REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add Mode of transportation column under paragraph 6.3. Update document paragraphs to current requirements. - ro	18-06-14	C. SAFFLE
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-11-20	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B	B	B	B			
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PMIC N/A

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Original date of drawing
YY-MM-DD

13-01-11

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APPROVED BY
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TITLE

MICROCIRCUIT, LINEAR, 2.5 V TO 3.3 V HIGH PERFORMANCE CLOCK BUFFER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**
A	**16236**

DWG NO.
V62/13603

REV **B**

PAGE 1 **OF** 14

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V014-24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a 2.5 V to 3.3 V high performance clock buffer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13603	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	CDCVF2310-EP	2.5 V to 3.3 V high performance clock buffer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{DD})	-0.5 V to 4.6 V
Input voltage range, (V_I)	-0.5 V to V_{DD} + 0.5 V 2/ 3/
Output voltage range, (V_O)	-0.5 V to V_{DD} + 0.5 V 2/ 3/
Input clamp current, (I_{IK}) (V_I < 0 or V_I > V_{DD})	±50 mA
Output clamp current, (I_{OK}) (V_O < 0 or V_O > V_{DD})	±50 mA
Continuous total output current, (I_O) (V_O = 0 to V_{DD})	±50 mA
Package thermal impedance, (θ_{JA})	91.7 °C/W 4/
Storage temperature range	-65°C to 150°C

1.4 Recommended operating conditions. 5/ 6/

Supply voltage, (V_{DD})	2.3 V to 2.5 V nominal
Supply voltage, (V_{DD})	3.3 V nominal to 3.6 V
Maximum low level input voltage, (V_{IL})	
V_{DD} = 3 V to 3.6 V	0.8 V
V_{DD} = 2.3 V to 2.7 V	0.7 V
Minimum high level input voltage, (V_{IH})	
V_{DD} = 3 V to 3.6 V	2 V
V_{DD} = 2.3 V to 2.7 V	1.7 V
Input voltage, (V_I)	0 V to V_{DD}
High level output current, (I_{OH})	
V_{DD} = 3 V to 3.6 V	12 mA
V_{DD} = 2.3 V to 2.7 V	6 mA
Low level output current, (I_{OL})	
V_{DD} = 3 V to 3.6 V	12 mA
V_{DD} = 2.3 V to 2.7 V	6 mA
Operating junction temperature, (T_J):	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output clamp-current rating are observed.
3/ This value is limited to 4.6 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ Unused inputs must be high or low to prevent them from floating.

1.5 Thermal characteristics.

Thermal metric 7/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 8/	91.7	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 9/	31.2	
Junction to board thermal resistance, θ_{JB} 10/	46.4	
Junction to top characterization parameter, Ψ_{JT} 11/	1.5	
Junction to board characterization parameter, Ψ_{JB} 12/	45.8	
Junction to case (bottom) thermal resistance, θ_{JCbot} 13/	N/A	

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at https://www.ansi.org)

JEDEC Solid State Technology Association

JEDEC JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
EIA/JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JESD51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

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7/ For more information about traditional and new thermal metrics, see manufacturer data.
8/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
9/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
10/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
11/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
12/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
13/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Test load circuit. The test load circuit shall be as shown in figure 6.

3.5.7 Voltage waveforms propagation delay times. The voltage waveforms propagation delay times shall be as shown in figure 7.

3.5.8 Output skew. The output skew shall be as shown in figure 8.

3.5.9 Pulse skew. The pulse skew shall be as shown in figure 9.

3.5.10 Supply current vs Frequency. The supply current vs Frequency shall be as shown in figure 10.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ 2/	Max	
Over recommended operating free air temperature range (unless otherwise noted)						
Input voltage	V_{IK}	V_{DD} = 3 V, I_I = -18 mA			-1.2	V
Input current	I_I	V_I = 0 V to V_{DD}			±5	µA
Static device current	I_{DD} 3/	CLK = 0 to V_{DD}, I_O = 0 mA			100	µA
Input capacitance	C_I	V_{DD} = 2.3 V to 3.6 V, V_I = 0 V or V_{DD}		2.5		pF
Output capacitance	C_O	V_{DD} = 2.3 V to 3.6 V, V_I = 0 V or V_{DD}		2.8		pF
V_{DD} = 3.3 V ±0.3 V						
High level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V, I_{OH} = -12 mA	2.1			
		V_{DD} = 3 V, I_{OH} = -6 mA	2.4			
Low level output voltage	V_{OL}	V_{DD} = min to max, I_{OL} = 100 µA			0.2	V
		V_{DD} = 3 V, I_{OL} = 12 mA			0.8	
		V_{DD} = 3 V, I_{OL} = 6 mA			0.55	
High level output current	I_{OH}	V_{DD} = 3 V, V_O = 1 V	-28			mA
		V_{DD} = 3.3 V, V_O = 1.65 V		-36		
		V_{DD} = 3.6 V, V_O = 3.135 V			-14	
Low level output current	I_{OL}	V_{DD} = 3 V, V_O = 1.95 V	28			mA
		V_{DD} = 3.3 V, V_O = 1.65 V		36		
		V_{DD} = 3.6 V, V_O = 0.4 V			14	
V_{DD} = 2.5 V ±0.2 V						
High level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V, I_{OH} = -6 mA	1.8			
Low level output voltage	V_{OL}	V_{DD} = min to max, I_{OL} = 100 µA			0.2	V
		V_{DD} = 3 V, I_{OL} = 6 mA			0.55	
High level output current	I_{OH}	V_{DD} = 2.3 V, V_O = 1 V	-15			mA
		V_{DD} = 2.5 V, V_O = 1.25 V		-25		
		V_{DD} = 2.7 V, V_O = 2.375 V			-10	
Low level output current	I_{OL}	V_{DD} = 2.3 V, V_O = 1.2 V	15			mA
		V_{DD} = 2.5 V, V_O = 1.25 V		25		
		V_{DD} = 2.7 V, V_O = 0.3 V			10	

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ 2/	Max	
Timing requirements Over recommended ranges of supply voltage and operating free air temperature						
Clock frequency	f_{clk}	V_{DD} = 3 V to 3.6 V	0		200	MHz
		V_{DD} = 2.3 V to 2.7 V	0		170	
Jitter characteristics Characterized using this device performance EVM when V_{DD} = 3.3 V. Outputs not under test are terminated to 50 Ω						
Additive phase jitter from input to output 1 YD	t_{jitter}	12 kHz to 5 MHz, f_{out} = 30.72 MHz		52		fs ms
		12 kHz to 20 MHz, f_{out} = 125 MHz		45		
Switching characteristics Over recommended operating free air temperature range (unless otherwise noted). V_{DD} = 3.3 V ±0.3 V (See FIGURE 6)						
CLK to Yn	t_{PLH} t_{PHL}	f = 0 MHz to 200 MHz, for circuit load, see FIGURE 6	1.3		3.3	ns
Output skew 4/ (Ym to Yn)	$t_{sk(0)}$	See FIGURE 8			100	ps
Pulse skew	$t_{sk(p)}$	See FIGURE 9			570	ps
Part to part skew	$t_{sk(pp)}$				500	ps
Rise time	t_r	V_O = 0.4 V to 2 V, see FIGURE 7	0.7		2	V/ns
Fall time	t_f	V_O = 2 V to 0.4 V, see FIGURE 7	0.7		2	V/ns
Enable setup time, G_high before CLK ↓	$t_{su(en)}$		0.1			ns
Disable setup time, G_low before CLK ↓	$t_{su(dis)}$		0.1			ns
Enable hold time, G_high after CLK ↓	$t_{h(en)}$		0.4			ns
Disable hold time, G_low after CLK ↓	$t_{h(dis)}$		0.4			ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Switching characteristics – continued. Over recommended operating free air temperature range (unless otherwise noted). V_{DD} = 2.5 V ±0.2 V (See FIGURE 6)						
CLK to Yn	t_{PLH} t_{PHL}	f = 0 MHz to 200 MHz, for circuit load, see FIGURE 6	1.5		4	ns
Output skew (Ym to Yn) 4/	$t_{sk(0)}$	See FIGURE 8			170	ps
Pulse skew	$t_{sk(p)}$	See FIGURE 9			680	ps
Part to part skew	$t_{sk(pp)}$				600	ps
Rise time	t_r	V_O = 0.4 V to 1.7 V, see FIGURE 7	0.5		1.4	V/ns
Fall time	t_f	V_O = 1.7 V to 0.4 V, see FIGURE 7	0.5		1.4	V/ns
Enable setup time, G_high before CLK ↓	$t_{su(en)}$		0.1			ns
Disable setup time, G_low before CLK ↓	$t_{su(dis)}$		0.1			ns
Enable hold time, G_high after CLK ↓	$t_{h(en)}$		0.4			ns
Disable hold time, G_low after CLK ↓	$t_{h(dis)}$		0.4			ns

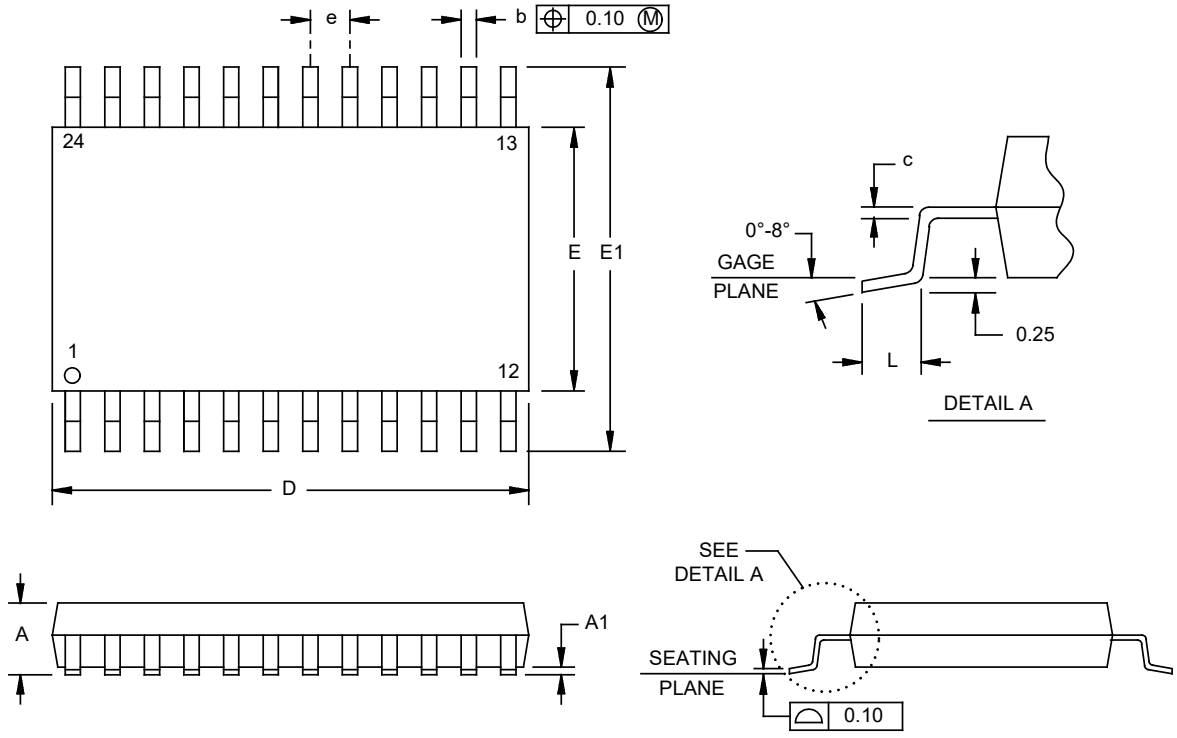
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All typical values are at respective nominal V_{DD}.

3/ For I_{CC} over frequency, see FIGURE 10.

4/ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	7.70	7.90			

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. This drawing is subject to change without notice.
3. For dimension D, body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
4. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
5. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	24	CLK
2	V_{DD}	23	V_{DD}
3	1Y0	22	V_{DD}
4	1Y1	21	2Y0
5	1Y2	20	2Y1
6	GND	19	GND
7	GND	18	GND
8	1Y3	17	2Y2
9	1Y4	16	2Y3
10	V_{DD}	15	V_{DD}
11	1G	14	V_{DD}
12	2Y4	13	2G

FIGURE 2. Terminal connections.

Terminal number	Terminal name	I/O	Description
11	1G	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high
13	2G	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high
3, 4, 5, 8, 9	1Y[0:4]	O	Buffered outputs clocks
21, 20, 17, 16, 12	2Y[0:4]	O	Buffered outputs clocks
24	CLK	I	Input reference frequency
1, 6, 7, 18, 19	GND		Ground
2, 10, 14, 15, 22, 23	V_{DD}		DC power supply, 2.3 V to 3.6 V

FIGURE 3. Terminal function.

Input			**Output**	
1G	2G	CLK	1Y[0:4]	2Y[0:4]
L	L	↓	L	L
H	L	↓	CLK SEE NOTE 1	L
L	H	↓	L	CLK SEE NOTE 1
H	H	↓	CLK SEE NOTE 1	CLK SEE NOTE 1

NOTE 1. After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

FIGURE 4. Function table.

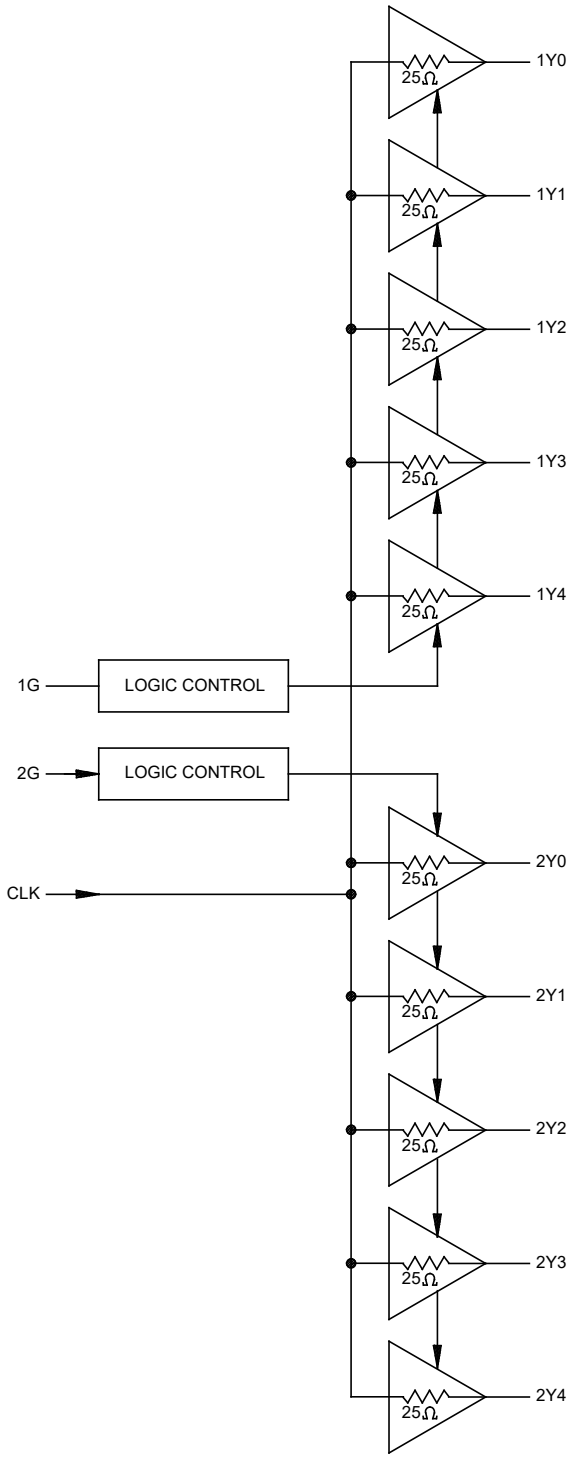
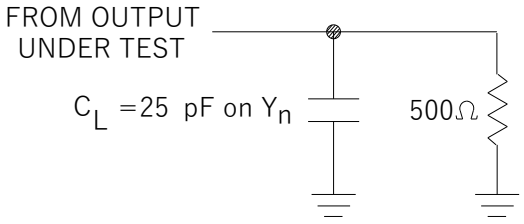


FIGURE 5. Functional block diagram.



NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.

FIGURE 6. Test load circuit.

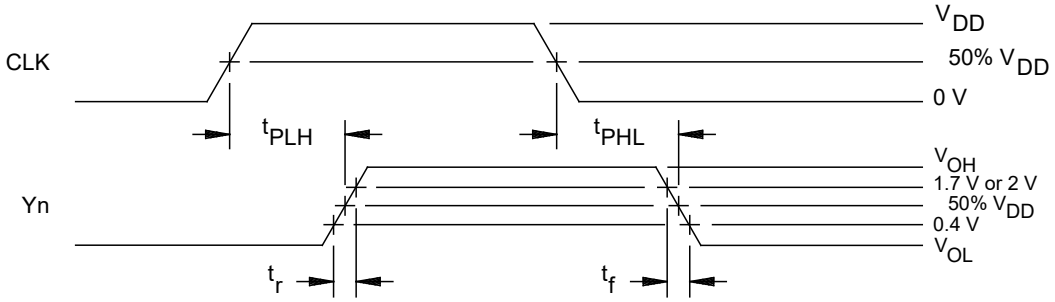


FIGURE 7. Voltage waveforms propagation delay times.

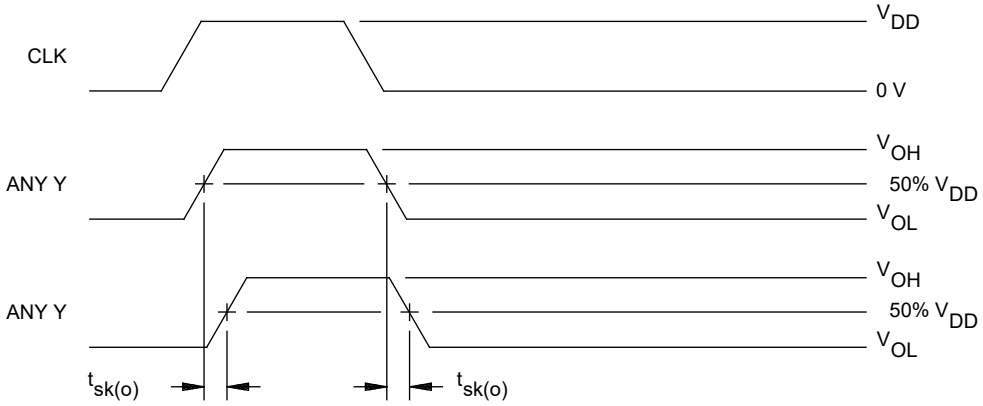
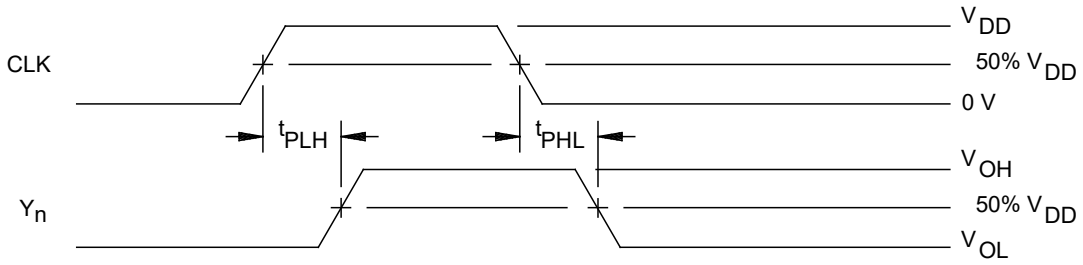


FIGURE 8. Output skew.



NOTE:
1. $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

FIGURE 9. Pulse skew.

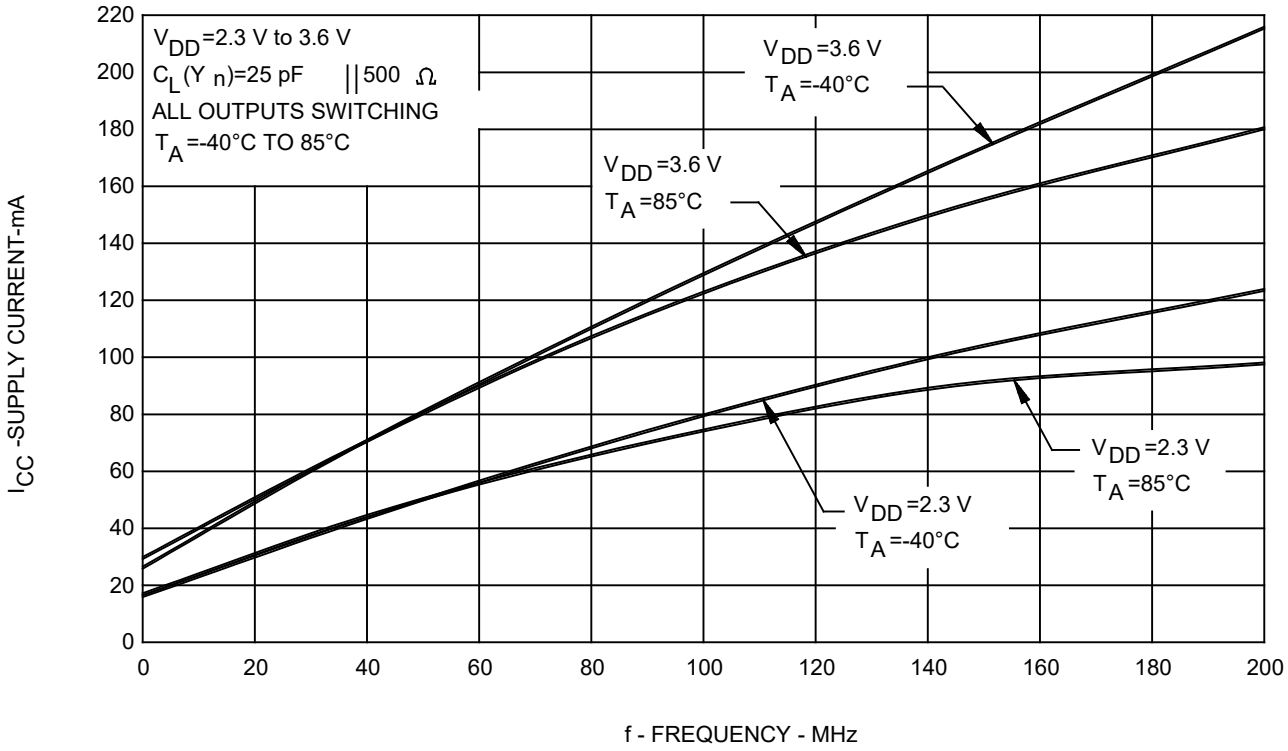


FIGURE 10. Supply current vs Frequency.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation	Top side marking	Vendor part number
V62/13603-01XE	01295	Tape and reel	CKV2310EP	CDCVF2310MPWREP
		Tube	CKV2310EP	CDCVF2310MPWEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243