REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-05-22	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-10-18	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV												
SHEET												
REV												
SHEET												
REV	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/landandmaritime
Original date of drawing YY MM DD 13-02-07	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, 16 BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE A / **CAGE CODE** 16236	**DWG NO.** **V62/12667**
	REV B	**PAGE 1 OF 12**

AMSC N/A

5962-V170-23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 bit dual supply bus transceiver with configurable voltage translation and 3-state outputs microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12667	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC16T245-EP	16 bit dual supply bus transceiver with configurable voltage translation and 3-state outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range: (V_{CCA}, V_{CCB}) .... -0.5 V to 6.5 V
Input voltage range (V_I): 2/
I/O ports (A port) .... -0.5 V to 6.5 V
I/O ports (B port) .... -0.5 V to 6.5 V
Control inputs .... -0.5 V to 6.5 V
Voltage range applied to any output in the high impedance or power off stated, (V_O): 2/
A port .... -0.5 V to 6.5 V
B port .... -0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, (V_O): 2/ 3/
A port .... -0.5 V to V_{CCA} + 0.5 V
B port .... -0.5 V to V_{CCB} + 0.5 V
Input clamp current, (I_{IK}) ($V_I < 0$) .... -50 mA
Output clamp current, (I_{OK}) ($V_O < 0$) .... -50 mA
Continuous output current, (I_O) .... ±50 mA
Continuous current through each V_{CCA}, V_{CCB} , and GND .... ±100 mA
Maximum junction temperature,(T_J) .... 150 °C
Storage temperature range .... -65°C to 150°C

1.4 Thermal characteristics.

Thermal metric 4/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 5/	59.9	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 6/	13.9	°C/W
Junction to board thermal resistance, θ_{JB} 7/	27.1	°C/W
Junction to top characterization parameter, Ψ_{JT} 8/	0.5	°C/W
Junction to board characterization parameter, Ψ_{JB} 9/	26.8	°C/W
Junction to case (bottom) thermal resistance, θ_{JCbot} 10/	N/A	°C/W

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The output positive-voltage may be exceeded up to 6.5 V maximum if the output current rating is observed.
4/ For more information about traditional and new thermal metric, see manufacturer “the IC package Thermal Metric application report, SPRA953”.
5/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-k-board, as specified in JESD51-7, in an environment described in JESD51-2a.
6/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
7/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
8/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
9/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
10/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

1.5 Recommended operating conditions. 11/ 12/ 13/ 14/ 15/

		V_{CCI}	V_{CCO}	Limits		Unit
				Min	Max	
Supply voltage	V_{CCA}			1.65	5.5	V
	V_{CCB}			1.65	5.5	V
High level input voltage, (V_{IH})	Data inputs 16/	1.65 V to 1.95 V		V_{CCI} x 0.65		V
		2.3 V to 2.7 V		1.7		V
		3 V to 3.6 V		2		V
		4.5 V to 5.5 V		V_{CCI} x 0.7		V
Low level input voltage, (V_{IL})	Data inputs 16/	1.65 V to 1.95 V			V_{CCI} x 0.35	V
		2.3 V to 2.7 V			0.7	V
		3 V to 3.6 V			0.8	V
		4.5 V to 5.5 V			V_{CCI} x 0.3	V
High level input voltage, (V_{IH})	Control inputs (referenced to V_{CCA}) 17/	1.65 V to 1.95 V		V_{CCA} x 0.65		V
		2.3 V to 2.7 V		1.7		V
		3 V to 3.6 V		2		V
		4.5 V to 5.5 V		V_{CCA} x 0.7		V
Low level input voltage, (V_{IL})	Control inputs (referenced to V_{CCA}) 17/	1.65 V to 1.95 V			V_{CCA} x 0.35	V
		2.3 V to 2.7 V			0.7	V
		3 V to 3.6 V			0.8	V
		4.5 V to 5.5 V			V_{CCA} x 0.3	V
Input voltage, (V_I)	Control inputs			0	5.5	V
Input/output voltage, ($V_{I/O}$)	Active state			0	V_{CCO}	V
	3-State			0	5.5	V
High level output current, (I_{OH})			1.65 V to 1.95 V		-4	mA
			2.3 V to 2.7 V		-8	mA
			3 V to 3.6 V		-24	mA
			4.5 V to 5.5 V		-32	mA
Low level output current, (I_{OL})			1.65 V to 1.95 V		4	mA
			2.3 V to 2.7 V		8	mA
			3 V to 3.6 V		24	mA
			4.5 V to 5.5 V		32	mA
Input transition rise or fall rate, ($\Delta t/\Delta v$)	Data inputs	1.65 V to 1.95 V			20	ns/V
		2.3 V to 2.7 V			20	ns/V
		3 V to 3.6 V			10	ns/V
		4.5 V to 5.5 V			5	ns/V
Operating free air temperature, (T_A)				-55	125	°C

11/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
12/ V_{CCI} is the V_{CC} associated with the input port.
13/ V_{CCO} is the V_{CC} associated with the output port.
14/ All unused or driven (floating) data inputs (I/Os) of the device must held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to manufacturer data, Implications of Slow or Floating CMOS inputs, literature number SCBA004.
15/ All unused data inputs of the device must be held at V_{CCA} or GND to ensure proper device operation.
16/ For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} x 0.7 V, V_{IL} max = V_{CCI} x 0.3 V.
17/ For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} x 0.7 V, V_{IL} max = V_{CCA} x 0.3 V

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board thermal resistance Theta-JB or $R\theta_{JB}$

(Copies of these documents are available online at https://www.jedec.org.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available from https://www.ansi.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.5, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The function table shall be as shown in figure 3.

3.5.4 Logic diagram (Positive Logic). The logic diagram (Positive Logic) shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and voltage waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test		Test conditions	V_{CCA}	V_{CCB}	Limits Min	Limits Max	Unit
Electrical characteristics 2/ 3/							
T_A = -55°C to 125°C, over recommended input voltage range (unless otherwise noted)							
V_{OH}		I_{OH} = -100 µA, $V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V	V_{CCO} – 0.1		V
		I_{OH} = -4 mA, $V_I = V_{IH}$	1.65 V	1.65 V	1.2		V
		I_{OH} = -8 mA, $V_I = V_{IH}$	2.3 V	2.3 V	1.9		V
		I_{OH} = -24 mA, $V_I = V_{IH}$	3 V	3 V	2.35		V
		I_{OH} = -32 mA, $V_I = V_{IH}$	4.5 V	4.5 V	3.75		V
V_{OL}		I_{OL} = 100 µA, $V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V		0.1	V
		I_{OL} = 4 mA, $V_I = V_{IL}$	1.65 V	1.65 V		0.45	V
		I_{OL} = 8 mA, $V_I = V_{IL}$	2.3 V	2.3 V		0.3	V
		I_{OL} = 24 mA, $V_I = V_{IL}$	3 V	3 V		0.65	V
		I_{OL} = 32 mA, $V_I = V_{IL}$	4.5 V	4.5 V		0.65	V
I_I	Control inputs	$V_I = V_{CCA}$ or GND	1.65 V to 5.5 V	1.65 V to 5.5 V		±2	µA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V	0 V	0 V to 5.5 V		±10	µA
			0 V to 5.5 V	0 V		±10	µA
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V		±10	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V		20	µA
			5 V	0 V		20	µA
			0 V	5 V		-2.5	µA
I_{CCB}		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V		20	µA
			5 V	0 V		-2.5	µA
			0 V	5 V		20	µA
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V		30	µA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open	3 V to 5.5 V	3 V to 5.5 V		50	µA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND				50	µA
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V		50	µA
C_I	Control inputs	$V_I = V_{CCA}$ or GND	3.3 V	3.3 V	4	TYP	pF
C_{IO}	A or B port	$V_O = V_{CCA/B}$ or GND	3.3 V	3.3 V	8.5	TYP	pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Parameter	Test conditions	From (Input)	To (Output)	V_{CCB} = 1.8 V ±0.15 V Min	Max	V_{CCB} = 2.5 V ±0.2 V Min	Max	V_{CCB} = 3.3 V ±0.3 V Min	Max	V_{CCB} =5 V ±0.5 V Min	Max	Unit
Switching characteristics												
T_A = -55°C to 125°C, V_{CCA} = 1.8 V ±0.15 V (unless otherwise noted) (See FIGURE 5).												
t_{PLH}		A	B	1.7	25.9	1.3	13.2	1	11.4	0.8	11.1	ns
t_{PHL}												ns
t_{PLH}		B	A	0.9	27.8	0.8	27.8	0.7	27.4	0.7	27.4	ns
t_{PHL}												ns
t_{PHZ}		$\overline{OE}$	A	1.6	33.6	1.5	33.4	1.5	33.3	1.4	33.2	ns
t_{PLZ}												ns
t_{PHZ}		$\overline{OE}$	B	2.4	36.2	1.9	17.1	1.7	16	1.3	14.3	ns
t_{PLZ}												ns
t_{PZH}		$\overline{OE}$	A	0.4	28	0.4	27.8	0.4	27.7	0.4	27.7	ns
t_{PZL}												ns
t_{PZH}		$\overline{OE}$	B	1.8	36	1.6	22	1.2	16.6	0.9	14.8	ns
t_{PZL}												ns
Switching characteristics – Continued												
T_A = -55°C to 125°C, V_{CCA} = 2.5 V ±0.2 V (unless otherwise noted) (See FIGURE 5).												
t_{PLH}		A	B	1.6	25.4	1.2	13	0.8	10.2	0.6	8.8	ns
t_{PHL}												ns
t_{PLH}		B	A	1.2	13.3	1	13.1	1	12.9	0.9	12.8	ns
t_{PHL}												ns
t_{PHZ}		$\overline{OE}$	A	1.4	13	1.4	13	1.4	13	1.4	13	ns
t_{PLZ}												ns
t_{PHZ}		$\overline{OE}$	B	2.3	33.6	1.8	14	1.7	14.3	0.9	10.9	ns
t_{PLZ}												ns
t_{PZH}		$\overline{OE}$	A	1	14.9	1	14.9	1	14.9	1	14.9	ns
t_{PZL}												ns
t_{PZH}		$\overline{OE}$	B	1.7	32.2	1.6	16.9	1.2	13.4	1	10.9	ns
t_{PZL}												ns
Switching characteristics - Continued												
T_A = -55°C to 125°C, V_{CCA} = 3.3 V ±0.3 V (unless otherwise noted) (See FIGURE 5).												
t_{PLH}		A	B	1.5	25.2	1.1	12.8	0.8	10.2	0.5	8.4	ns
t_{PHL}												ns
t_{PLH}		B	A	0.9	11.2	0.8	10.2	0.7	10.1	0.6	10	ns
t_{PHL}												ns
t_{PHZ}		$\overline{OE}$	A	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	ns
t_{PLZ}												ns
t_{PHZ}		$\overline{OE}$	B	2.1	33	1.7	14.3	1.5	12.8	0.8	10.3	ns
t_{PLZ}												ns
t_{PZH}		$\overline{OE}$	A	0.8	11.8	0.8	12.1	0.8	12.1	0.8	12.1	ns
t_{PZL}												ns
t_{PZH}		$\overline{OE}$	B	1.6	31.7	1.4	16.4	1.1	12.9	0.9	10.4	ns
t_{PZL}												ns

See footnote at the end of table.

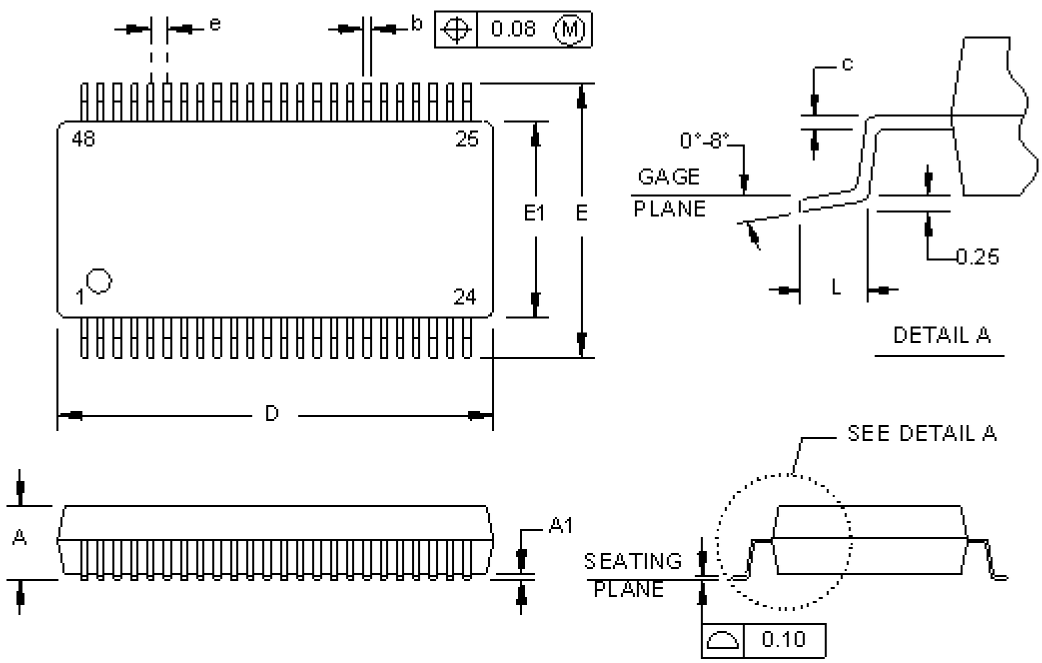
TABLE I. Electrical performance characteristics - Continued. 1/

Parameter	Test conditions	From (Input)	To (Output)	V_{CCB} = 1.8 V ±0.15 V Min	Max	V_{CCB} = 2.5 V ±0.2 V Min	Max	V_{CCB} = 3.3 V ±0.3 V Min	Max	V_{CCB} =5 V ±0.5 V Min	Max	Unit
Switching characteristics T_A = -55°C to 125°C, V_{CCA} = 5 V ±0.5 V (unless otherwise noted) (See FIGURE 5).												
t_{PLH}		A	B	1.6	25.4	1	14.3	0.7	10	0.4	8.2	ns
t_{PHL}												ns
t_{PLH}		B	A	0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	ns
t_{PHL}												ns
t_{PHZ}		$\overline{OE}$	A	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	ns
t_{PLZ}												ns
t_{PHZ}		$\overline{OE}$	B	2	32.7	1.6	13.7	1.4	12	0.7	9.7	ns
t_{PLZ}												ns
t_{PZH}		$\overline{OE}$	A	0.7	10.4	0.7	10.4	0.7	10.4	0.7	10.4	ns
t_{PZL}												ns
t_{PZH}		$\overline{OE}$	B	1.6	31.6	1.3	19.3	1	12.6	0.9	10	ns
t_{PZL}												ns

Test	Symbol	Test conditions	V_{CCA} = V_{CCB} = 1.8 V TYP	V_{CCA} = V_{CCB} = 2.5 V TYP	V_{CCA} = V_{CCB} = 3.3 V TYP	V_{CCA} = V_{CCB} = 5 V TYP	Unit
Operating characteristics T_A = 25°C							
A-port input, B-port output	C_{pdA} 4/	CL = 0, f = 10 MHz t_r = t_f = 1 ns	2	2	2	3	pF
B-port input, A-port output			18	19	19	22	pF
A-port input, B-port output	C_{pdB} 4/		18	19	20	22	pF
B-port input, A-port output			2	2	2	2	pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ V_{CCO} is the V_{CC} associated with the output port.
3/ V_{CCI} is the V_{CC} associated with the input port.
4/ Power dissipation capacitance per transceiver.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millim eters	
	Min	Max		Min	Max
A		1.20	E	7.90	8.30
A1	0.05	0.15	E1	6.00	6.20
b	0.17	0.27	e	0.50 BSC	
c	0.15 TYP		L	0.50	0.75
D	12.40	12.60			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold protrusion not to exceed 0.15.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symb1B1ol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	13	2B1	25	$2\overline{OE}$	37	1A8
2	1B1	14	2B2	26	2A8	38	1A7
3	1B2	15	GND	27	2A7	39	GND
4	GND	16	2B3	28	GND	40	1A6
5	1B3	17	2B4	29	2A6	41	1A5
6	1B4	18	V_{CCB}	30	2A5	42	V_{CCA}
7	V_{CCB}	19	2B5	31	V_{CCA}	43	1A4
8	1B5	20	2B6	32	2A4	44	1A3
9	1B6	21	GND	33	2A3	45	GND
10	GND	22	2B7	34	GND	46	1A2
11	1B7	23	2B8	35	2A2	47	1A1
12	1B8	24	2DIR	36	2A1	48	$1\overline{OE}$

FIGURE 2. Terminal connections.

(Each 8-bit Section) 1/

Control Inputs		Output Circuits		Operation
$\overline{OE}$	DIR	A Port	B Port	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

1. Input circuits of the data I/Os always are active.

FIGURE 3. Function table.

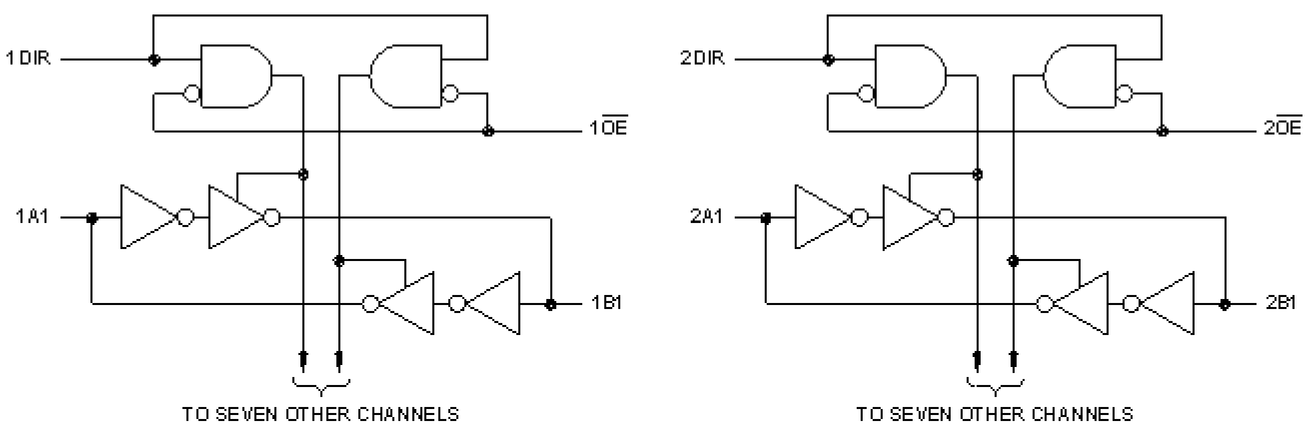
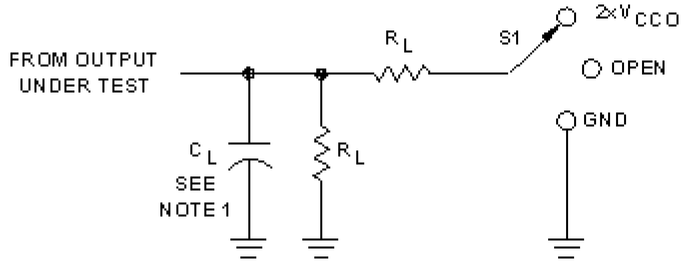


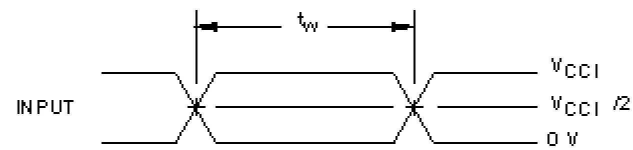
FIGURE 4. Logic diagram (Positive Logic).



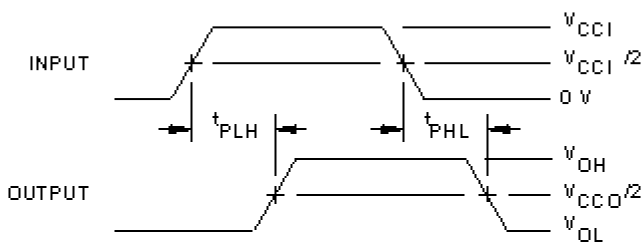
LOAD CIRCUIT

TEST	S1
t_{pd}	OPEN
t_{PLZ} / t_{PZL}	$2 \times V_{CCO}$
t_{PHZ} / t_{PZH}	GND

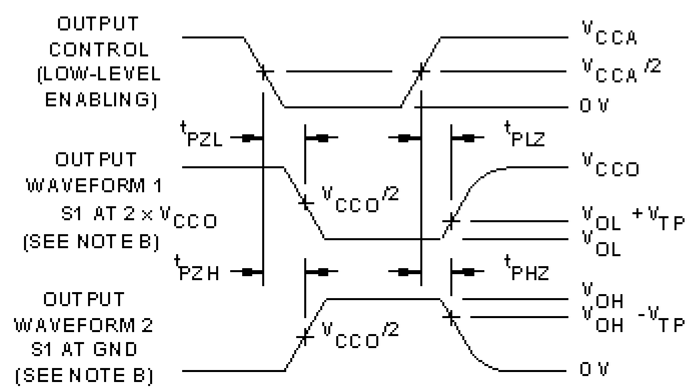
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ±0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ±0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ±0.3 V	15 pF	2 kΩ	0.3 V
5 V ±0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The output are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as tdis.
6. t_{PZL} and t_{PZH} are the same as ten.
7. t_{PLH} and t_{PHL} are the same as tpd.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.
10. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transport media	Vendor part number	Top side marking
V62/12667-01XE	01295	Tape and real	CLVC16T245MDGGREP	LVC16T245MEP
		Tube	CLVC16T245MDGGEP	LVC16T245MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243