

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete figure 5 and all Daisy chain mode references under footnote 13/ as specified under table I. Add typical limits to INE, DNE, FSE, ZSE, AE, ZIN, IDD, ISS, ICC, and IOICC as specified under table I. - ro	13-10-02	C. SAFFLE
B	Add lead finish E device. Add mode of transportation and quantity column under paragraph 6.3. - ro	18-03-07	C. SAFFLE
C	Update document paragraphs to current requirements. - ro	23-07-07	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

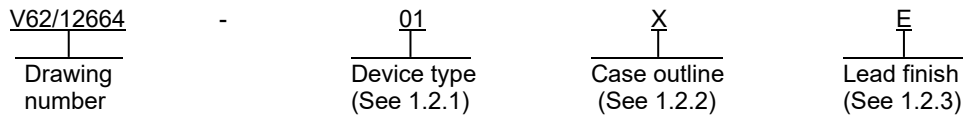
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

<b>PMIC N/A</b>  Original date of drawing 13-04-11	<b>PREPARED BY</b> RICK OFFICER		<b>DLA LAND AND MARITIME</b> COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/landandmaritime">https://www.dla.mil/landandmaritime</a>	
	<b>CHECKED BY</b> RAJESH PITHADIA		<b>TITLE</b> MICROCIRCUIT, DIGITAL-LINEAR, 20 BIT VOLTAGE OUTPUT DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON	
	<b>APPROVED BY</b> CHARLES F. SAFFLE		<b>DWG NO.</b> <b>V62/12664</b>	
	<b>SIZE</b> A	<b>CAGE CODE</b> 16236	<b>PAGE</b> 1 OF 20	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 20 bit, voltage output digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD5791	20 bit, voltage output digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-153-AC	Thin shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Positive analog supply voltage (VDD) to analog ground reference (AGND)	-0.3 V to +34 V
Negative analog supply (VSS) to AGND	-34 V to +0.3 V
VDD to VSS	-0.3 V to +34 V
Digital supply voltage (VCC) to digital ground reference (DGND)	-0.3 V to +7 V
Digital interface supply (IOVCC) to DGND	-0.3 V to VCC + 3 V or +7 V (whichever is less)
Digital inputs to DGND	-0.3 V to IOVCC + 0.3 V or +7 V (whichever is less)
Analog output voltage (VOUT) to AGND	-0.3 V to VDD + 0.3 V
Positive reference force voltage (VREFPF) to AGND	-0.3 V to VDD + 0.3 V
Positive reference sense voltage (VREFPS) to AGND	-0.3 V to VDD + 0.3 V
Negative reference force voltage (VREFNF) to AGND	VSS – 0.3 V to + 0.3 V
Negative reference sense voltage (VREFNS) to AGND	VSS – 0.3 V to +0.3 V
DGND to AGND	-0.3 V to +0.3 V
Storage temperature range (TSTG)	-65°C to +150°C
Maximum junction temperature range (TJ)	+150°C
Power dissipation (PD)	174.8 mW 2/
Electrostatic discharge (ESD):	
Human body model (HBM)	1.5 kV

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (TA)	-55°C to +125°C
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1.5 Thermal characteristics.

Thermal resistance, junction to case (θJC)	45°C/W
Thermal resistance, junction to ambient (θJA)	143°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Power dissipation (PD) = ( TJ max – TA ) / θJA = (150 – 125) / 143 = 0.1748 W.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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## 2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 3 and 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, TA	Device type	Limits		Unit				
					Min	Max					
Static performance <u>4/</u>											
Resolution			-55°C to +125°C	01	20		Bits				
Integral nonlinearity error (relative accuracy)	INE	VREFP = +10 V, VREFN = -10 V	0°C to +105°C	01	-1	+1	LSB				
			+25°C		±0.25 typical						
		VREFP = +10 V, VREFN = -10 V <u>5/</u>	-55°C to +125°C		-1.5	+1.5					
			+25°C		±0.5 typical						
		VREFP = +10 V, VREFN = 0 V <u>5/</u>	-55°C to +125°C		-1.5	+1.5					
			+25°C		±1 typical						
		VREFP = +5 V, VREFN = 0 V <u>5/</u>	-55°C to +125°C		-3	+3					
			+25°C		±0.25 typical						
Differential nonlinearity error	DNE	VREFP = +10 V, VREFN = -10 V	-55°C to +125°C	01	-1	+1	LSB				
			+25°C		±0.5 typical						
		VREFP = +10 V, VREFN = 0 V	-55°C to +125°C		-1.5	+1.5					
			+25°C		±0.75 typical						
		VREFP = +5 V, VREFN = 0 V	-55°C to +125°C		-2.5	+2.5					
			+25°C		±1 typical						
		Linearity error long <u>6/</u> term stability			After 500 hours	+125°C		01	0.16 typical		LSB
					After 1,000 hours				0.19 typical		
After 1,000 hours	+100°C			0.11 typical							
Full scale error	FSE	VREFP = +10 V, VREFN = -10 V <u>5/</u>	-55°C to +125°C	01	-7	+7	LSB				
			+25°C		±0.1 typical						
		VREFP = +10 V, VREFN = 0 V <u>5/</u>	-55°C to +125°C		-11	+11					
			+25°C		±0.25 typical						
		VREFP = +5 V, VREFN = 0 V <u>5/</u>	-55°C to +125°C		-21	+21					
			+25°C		±0.8 typical						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit				
					Min	Max					
Static performance – continued. <u>4/</u>											
Full scale error	FSE	V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = -10 V <u>5/</u>	0°C to +105°C	01	-4	+4	LSB				
			+25°C		±0.1 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = 0 V <u>5/</u>	0°C to +105°C		-4	+4					
			+25°C		±0.25 typical						
		V <sub>REFP</sub> = +5 V, V <sub>REFN</sub> = 0 V <u>5/</u>	0°C to +105°C		-6	+6					
			+25°C		±0.8 typical						
Full scale error temperature coefficient			+25°C	01	±0.02 typical		ppm FSR/ °C				
Zero scale error	ZSE	V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = -10 V <u>5/</u>	-55°C to +125°C	01	-7	+7	LSB				
			+25°C		±0.1 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = 0 V <u>5/</u>	-55°C to +125°C		-10	+10					
			+25°C		±0.15 typical						
		V <sub>REFP</sub> = +5 V, V <sub>REFN</sub> = 0 V <u>5/</u>	-55°C to +125°C		-21	+21					
			+25°C		±0.75 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = -10 V <u>5/</u>	0°C to +105°C		-4	+4					
			+25°C		±0.1 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = 0 V <u>5/</u>	0°C to +105°C		-4	+4					
			+25°C		±0.15 typical						
		V <sub>REFP</sub> = +5 V, V <sub>REFN</sub> = 0 V <u>5/</u>	0°C to +105°C		-6	+6					
			+25°C		±0.75 typical						
		Zero scale error <u>5/</u> temperature coefficient				+25°C		01	±0.04 typical		ppm FSR/ °C

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit				
					Min	Max					
Static performance – continued. 4/											
Gain error	AE	V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = -10 V 5/	-55°C to +125°C	01	-6	+6	ppm FSR				
			+25°C		±0.3 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = 0 V 5/	-55°C to +125°C		-10	+10					
			+25°C		±0.4 typical						
		V <sub>REFP</sub> = +5 V, V <sub>REFN</sub> = 0 V 5/	-55°C to +125°C		-20	+20					
			+25°C		±0.4 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = -10 V 5/	0°C to +105°C		-6	+6					
			+25°C		±0.3 typical						
		V <sub>REFP</sub> = +10 V, V <sub>REFN</sub> = 0 V 5/	0°C to +105°C		-6	+6					
			+25°C		±0.4 typical						
		V <sub>REFP</sub> = +5 V, V <sub>REFN</sub> = 0 V 5/	0°C to +105°C		-7	+7					
			+25°C		±0.4 typical						
		Gain error temperature coefficient 5/				+25°C		01	±0.04 typical		ppm FSR/ °C
		R1, RFB matching				+25°C		01	0.01 typical		%

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Output characteristics. <u>5/</u>							
Output voltage range			+25°C	01	VREFN	VREFP	V
Output slew rate			+25°C	01	50 typical		V/ $\mu$ s
Output voltage settling time		10 V step to 0.02%, using AD845 buffer in unity gain mode	+25°C	01	1 typical		$\mu$ s
		500 code step to $\pm 1$ LSB <u>7/</u>			1 typical		
Output noise spectral density		At 1 kHz, DAC code = midscale	+25°C	01	7.5 typical		nV / $\sqrt{\text{Hz}}$
		At 10 kHz, DAC code = midscale			7.5 typical		
		At 100 kHz, DAC code = midscale			7.5 typical		
Output voltage noise		DAC code = midscale, <u>8/</u> 0.1 Hz to 10 Hz bandwidth	+25°C	01	1.1 typical		$\mu$ V <sub>PP</sub>
Midscale glitch <u>9/</u> impulse		VREFP = +10 V, VREFN = -10 V	+25°C	01	3.1 typical		nV-sec
		VREFP = +10 V, VREFN = 0 V			1.7 typical		
		VREFP = +5 V, VREFN = 0 V			1.4 typical		
MSB segment <u>9/</u> glitch impulse		VREFP = +10 V, VREFN = -10 V	+25°C	01	9.1 typical		nV-sec
		VREFP = +10 V, VREFN = 0 V			3.6 typical		
		VREFP = +5 V, VREFN = 0 V			1.9 typical		
Output enabled glitch impulse		On removal of output ground clamp	+25°C	01	45 typical		nV-sec
Digital feedthrough			+25°C	01	0.4 typical		nV-sec
DC output impedance (normal mode)			+25°C	01	3.4 typical		k $\Omega$
DC output impedance (output clamped to ground)			+25°C	01	6 typical		k $\Omega$

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Output characteristics – continued. <u>5/</u>							
Spurious free dynamic range		1 kHz tone, 10 kHz sample rate	+25°C	01	100 typical		dB
Total harmonic distortion		1 kHz tone, 10 kHz sample rate	+25°C	01	97 typical		dB
Reference inputs. <u>5/</u>							
VREFP input range			-55°C to +125°C	01	5	V <sub>DD</sub> – 2.5	V
VREFN input range			-55°C to +125°C	01	V <sub>SS</sub> + 2.5 V	0	V
DC input impedance	Z <sub>IN</sub>	VREFP, VREFN, code dependent, typical mid-scale code	-55°C to +125°C	01	5		kΩ
			+25°C		6.6 typical		
Input capacitance	C <sub>IN</sub>	VREFP, VREFN	+25°C	01	15 typical		pF
Logic inputs. <u>5/</u>							
Input current <u>10/</u>	I <sub>IN</sub>		-55°C to +125°C	01	-1	+1	μA
Input low voltage	V <sub>IL</sub>	IOVCC = 1.71 V to 5.5 V	-55°C to +125°C	01		0.3 x IOVCC	V
Input high voltage	V <sub>IH</sub>	IOVCC = 1.71 V to 5.5 V	-55°C to +125°C	01	0.7 x IOVCC		V
Pin capacitance			+25°C	01	5 typical		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Logic output (SDO) <u>5/</u>							
Output low voltage	V <sub>OL</sub>	IOVCC = 1.71 V to 5.5 V, sinking 1 mA	-55°C to +125°C	01		0.4	V
Output high voltage	V <sub>OH</sub>	IOVCC = 1.71 V to 5.5 V, sourcing 1 mA	-55°C to +125°C	01	IOVCC – 0.5 V		V
High impedance leakage current			-55°C to +125°C	01		±1	μA
High impedance output capacitance			+25°C	01	3	typical	pF
Power requirements. All digital inputs at DGND or IOVCC							
Positive analog supply voltage	V <sub>DD</sub>		-55°C to +125°C	01	7.5	V <sub>SS</sub> + 33	V
Negative analog supply voltage	V <sub>SS</sub>		-55°C to +125°C	01	V <sub>DD</sub> – 33	-2.5	V
Digital supply voltage	V <sub>CC</sub>		-55°C to +125°C	01	2.7	5.5	V
Digital interface supply voltage	IOVCC	IOVCC ≤ V <sub>CC</sub>	-55°C to +125°C	01	1.71	5.5	V
Positive analog supply current	I <sub>DD</sub>		-55°C to +125°C	01		5.2	mA
			+25°C		4.2	typical	
Negative analog supply current	I <sub>SS</sub>		-55°C to +125°C	01		4.9	mA
			+25°C		4	typical	
Digital supply current	I <sub>CC</sub>		-55°C to +125°C	01		900	μA
			+25°C		600	typical	
Digital interface supply current	IOI <sub>CC</sub>	SDO disabled	-55°C to +125°C	01		140	μA
			+25°C		52	typical	
DC power <u>5/ 11/</u> supply rejection ratio		V <sub>DD</sub> ± 10%, V <sub>SS</sub> = 15 V	+25°C	01	±0.6 typical		μV/V
		V <sub>SS</sub> ± 10%, V <sub>DD</sub> = 15 V			±0.6 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Power requirements - continued.		All digital inputs at DGND or IOV <sub>CC</sub>					
AC power <u>5/</u> supply rejection ratio		V <sub>DD</sub> ± 200 mV, 50 Hz/60 Hz, V <sub>SS</sub> = -15 V	+25°C	01	95 typical		dB
		ΔV <sub>SS</sub> ± 200 mV, 50 Hz/60 Hz, V <sub>DD</sub> = 15 V			95 typical		
Timing requirements. <u>12/</u>							
SCLK cycle time <u>13/</u>	t <sub>1</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	40		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			28		
SCLK cycle time (readback) modes		IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	92		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			60		
SCLK high time	t <sub>2</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	15		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			10		
SCLK low time	t <sub>3</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	9		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			5		
$\overline{\text{SYNC}}$ to SCLK falling edge setup time	t <sub>4</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	5		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			5		
SCLK falling edge to $\overline{\text{SYNC}}$ rising edge hold time	t <sub>5</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	2		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			2		
Minimum $\overline{\text{SYNC}}$ high time	t <sub>6</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	48		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			40		
$\overline{\text{SYNC}}$ rising edge to next SCLK falling edge ignore	t <sub>7</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	8		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			6		
Data setup time	t <sub>8</sub>	IOV <sub>CC</sub> = 1.71 V to 3.3 V	-55°C to +125°C	01	9		ns
		IOV <sub>CC</sub> = 3.3 V to 5.5 V			7		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued. <u>12/</u>							
Data hold time	t <sub>9</sub>	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	12		ns
		IOVCC = 3.3 V to 5.5 V			7		
$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge	t <sub>10</sub>	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	13		ns
		IOVCC = 3.3 V to 5.5 V			10		
$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	t <sub>11</sub>	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	20		ns
		IOVCC = 3.3 V to 5.5 V			16		
$\overline{\text{LDAC}}$ pulse width low	t <sub>12</sub>	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	14		ns
		IOVCC = 3.3 V to 5.5 V			11		
$\overline{\text{LDAC}}$ falling edge to output response time	t <sub>13</sub>	IOVCC = 1.71 V to 3.3 V	+25°C	01	130 typical		ns
		IOVCC = 3.3 V to 5.5 V			130 typical		
$\overline{\text{SYNC}}$ rising edge to output response time ( $\overline{\text{LDAC}}$ tied low)	t <sub>14</sub>	IOVCC = 1.71 V to 3.3 V	+25°C	01	130 typical		ns
		IOVCC = 3.3 V to 5.5 V			130 typical		
$\overline{\text{CLR}}$ pulse width low	t <sub>15</sub>	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	50		ns
		IOVCC = 3.3 V to 5.5 V			50		
$\overline{\text{CLR}}$ pulse activation time	t <sub>16</sub>	IOVCC = 1.71 V to 3.3 V	+25°C	01	140 typical		ns
		IOVCC = 3.3 V to 5.5 V			140 typical		
$\overline{\text{SYNC}}$ falling edge to first SCLK rising edge	t <sub>17</sub>	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	0		ns
		IOVCC = 3.3 V to 5.5 V			0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> <u>3/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued. <u>12/</u>							
$\overline{\text{SYNC}}$ rising edge to SDO tristate	t18	IOVCC = 1.71 V to 3.3 V, CL = 50 pF	-55°C to +125°C	01		65	ns
		IOVCC = 3.3 V to 5.5 V, CL = 50 pF				60	
SCLK rising edge to SDO valid	t19	IOVCC = 1.71 V to 3.3 V, CL = 50 pF	-55°C to +125°C	01		62	ns
		IOVCC = 3.3 V to 5.5 V, CL = 50 pF				45	
$\overline{\text{SYNC}}$ rising edge to SCLK rising edge ignore	t20	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	0		ns
		IOVCC = 3.3 V to 5.5 V			0		
$\overline{\text{RESET}}$ pulse width low	t21	IOVCC = 1.71 V to 3.3 V	+25°C	01	35 typical		ns
		IOVCC = 3.3 V to 5.5 V			35 typical		
$\overline{\text{RESET}}$ pulse activation time	t22	IOVCC = 1.71 V to 3.3 V	+25°C	01	150 typical		ns
		IOVCC = 3.3 V to 5.5 V			150 typical		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, VDD = +12.5 V to +16.5 V, VSS = -16.5 V to -12.5 V, VREFP = +10 V, VREFN = -10 V, VCC = +2.7 V to +5.5 V, IOVCC = +1.71 V to +5.5 V, RL = unloaded, and CL = unloaded.
- 3/ Unless otherwise specified, for typical conditions, T<sub>A</sub> = +25°C, VDD = +15 V, VSS = -15 V, VREFP = +10 V, and VREFN = -10 V.
- 4/ Performance characterized with AD8676BRZ voltage reference buffers and AD8675ARZ output buffer.
- 5/ Guaranteed by design and characterization; not production tested.
- 6/ Linearity error refers to both INL error and DNL error; either parameter can be expected to drift by the amount specified after the length of time specified.
- 7/ The device configured in x2 gain mode, 25 pF compensation capacitor on AD797.
- 8/ Includes noise contribution from AD8676BRZ voltage reference buffers.
- 9/ The device is configured in the bias compensation mode with a low pass resistor-capacitor (RC) filter on the output. R = 300 Ω, C = 143 pF (total capacitance seen by the output buffer, lead capacitance).
- 10/ Current flowing in an individual logic pin.
- 11/ Includes PSRR of AD8676BRZ voltage reference buffers.
- 12/ All input signals are specified with t<sub>R</sub> = t<sub>F</sub> = 1 ns/V (10% to 90% of IOVCC) and timed from a voltage level of (V<sub>IL</sub> + V<sub>IH</sub>) / 2.
- 13/ Maximum SCLK frequency is 35 MHz for write mode and 16 MHz for readback mode.

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Case X

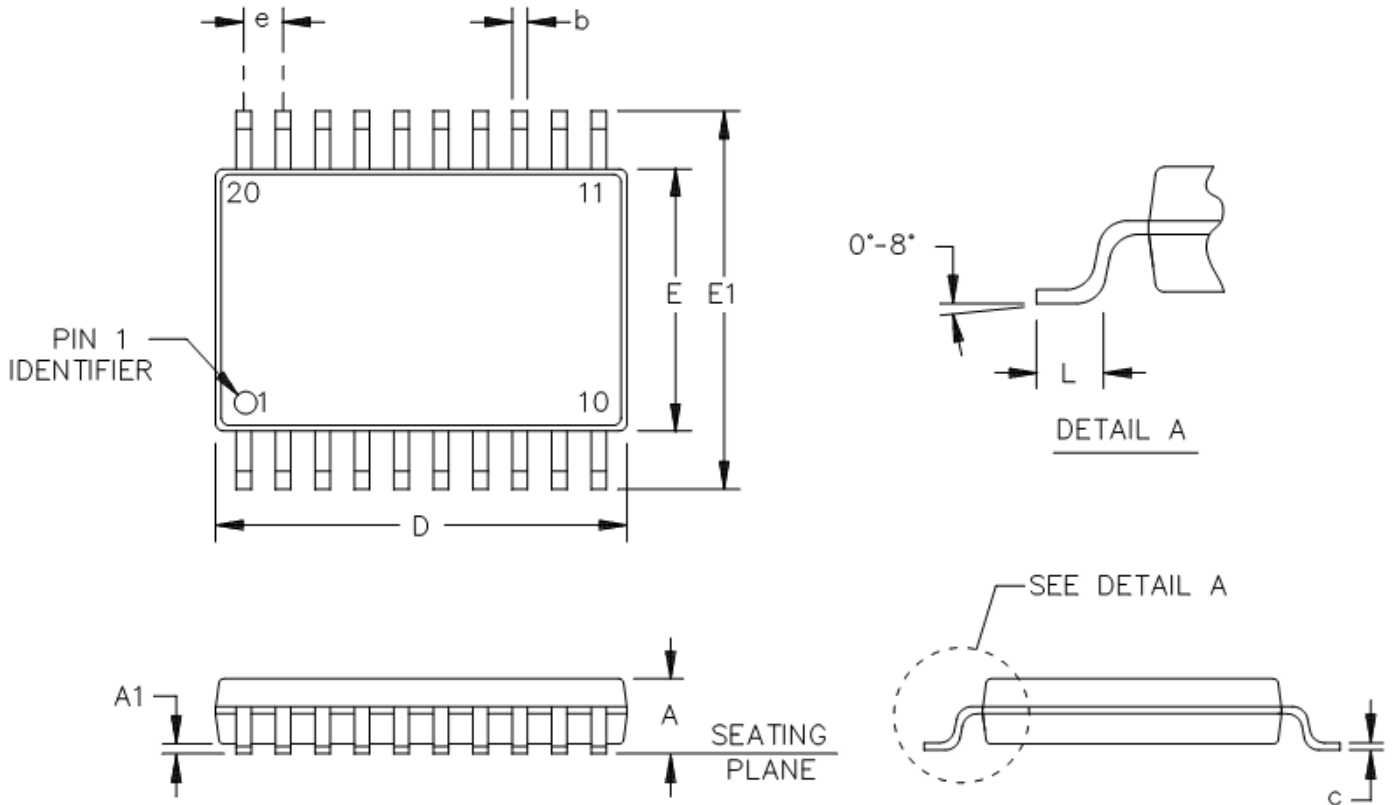


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Min	Nominal	Max	Min	Nominal	Max
A	---	---	.047	---	---	1.20
A1	.001	---	.005	0.05	---	0.15
b	.007	---	.011	0.19	---	0.30
c	.003	---	.007	0.09	---	0.20
D	.251	0.255	.259	6.40	6.50	6.60
E	.169	0.173	.177	4.30	4.40	4.50
E1	.251 BSC			6.40 BSC		
e	.025 BSC			0.65 BSC		
L	.017	.023	.029	0.45	0.60	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AC.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	INV	Connection to inverting input of external amplifier.
2	VOU	Analog output voltage.
3	VREFPS	Positive reference sense voltage input. A voltage range of 5 V to VDD – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFPF pin.
4	VREFPF	Positive reference force voltage input. A voltage range of 5 V to VDD – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFPS pin.
5	VDD	Positive analog supply connection. A voltage range of 7.5 V to 16.5 V can be connected. VDD should be decoupled to AGND.
6	$\overline{\text{RESET}}$	Active low reset logic input pin. Asserting this pin returns the device to its power on status.
7	$\overline{\text{CLR}}$	Active low clear logic input pin. Asserting this pin sets the DAC register to a user defined value and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
8	$\overline{\text{LDAC}}$	Active low load DAC input pin. This is used to update the DAC register and, consequently, the analog output. When tied permanently low, the output is updated on the rising edge of $\overline{\text{SYNC}}$ . If $\overline{\text{LDAC}}$ is held high during the write cycle, the input register is updated, but the output is held off until the falling edge of $\overline{\text{LDAC}}$ . The $\overline{\text{LDAC}}$ pin should not be left unconnected.
9	VCC	Digital supply connection. A voltage in the range of 2.7 V to 5.5 V can be connected. VCC should be decoupled to DGND.
10	IOVCC	Digital interface supply pin. Digital threshold levels are referenced to the voltage applied to this pin. A voltage range of 1.71 V to 5.5 V can be connected. IOVCC should not be allowed to exceed VCC.

FIGURE 2. Terminal connections.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
11	SDO	Serial data output pin. Data is clocked out on the rising edge of the serial clock input.
12	SDIN	Serial data input pin. This device has a 24 bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock rates of up to 35 MHz.
14	$\overline{\text{SYNC}}$	Active low digital interface synchronization input pin. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ is low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The input shift register is updated on the rising edge of $\overline{\text{SYNC}}$ .
15	DGND	Ground reference pin for digital circuitry.
16	VREFNF	Negative reference force voltage input. A voltage range of $V_{SS} + 2.5 \text{ V}$ to $0 \text{ V}$ can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFNS pin.
17	VREFNS	Negative reference sense voltage input. A voltage range of $V_{SS} + 2.5 \text{ V}$ to $0 \text{ V}$ can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFNF pin.
18	VSS	Negative analog supply connection. A voltage range of $-16.5 \text{ V}$ to $-2.5 \text{ V}$ can be connected. VSS should be decoupled to AGND.
19	AGND	Ground reference pin for analog circuitry.
20	RFB	Feedback connection for external amplifier.

FIGURE 2. Terminal connections - continued.

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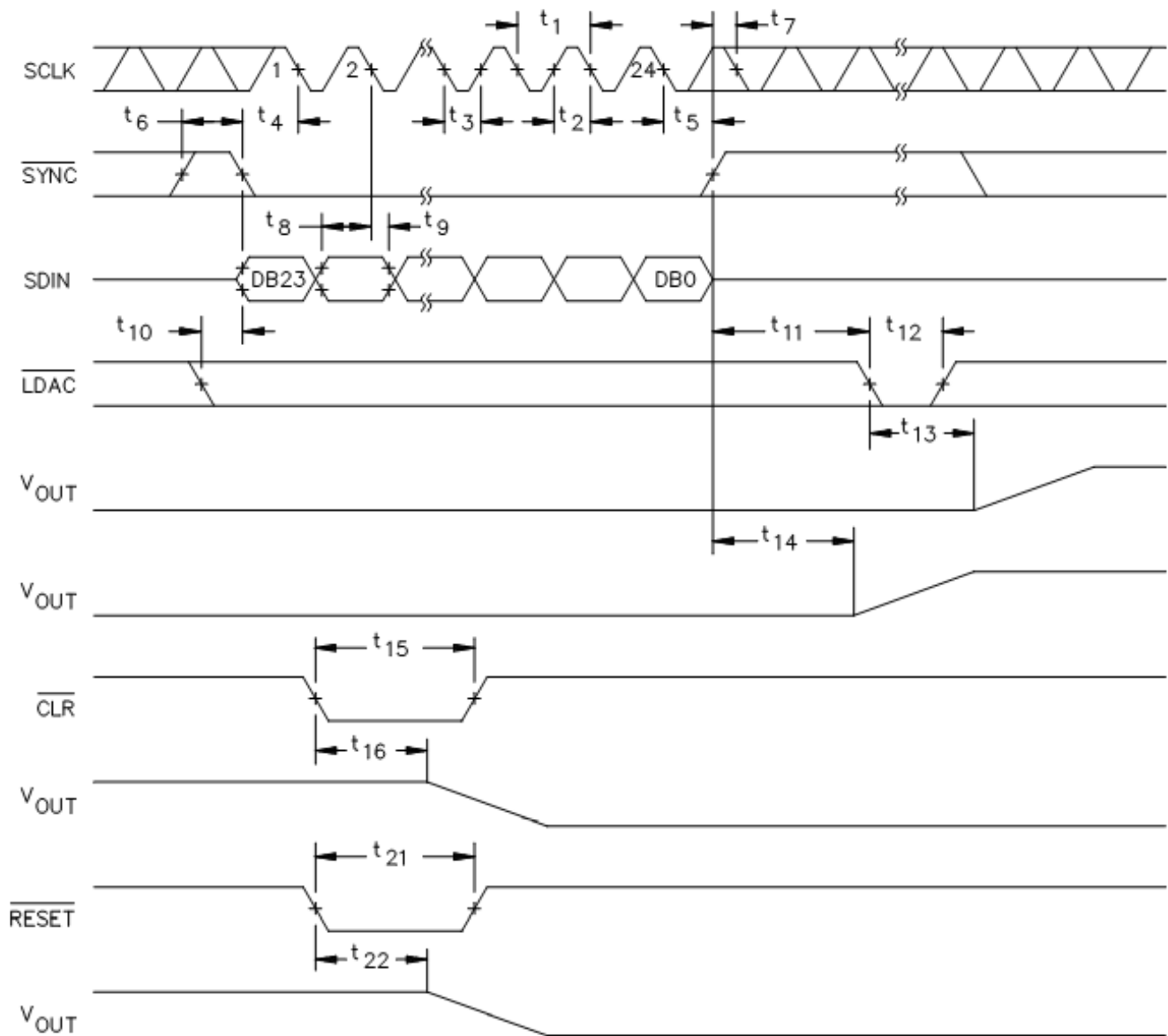


FIGURE 3. Write mode timing diagram.

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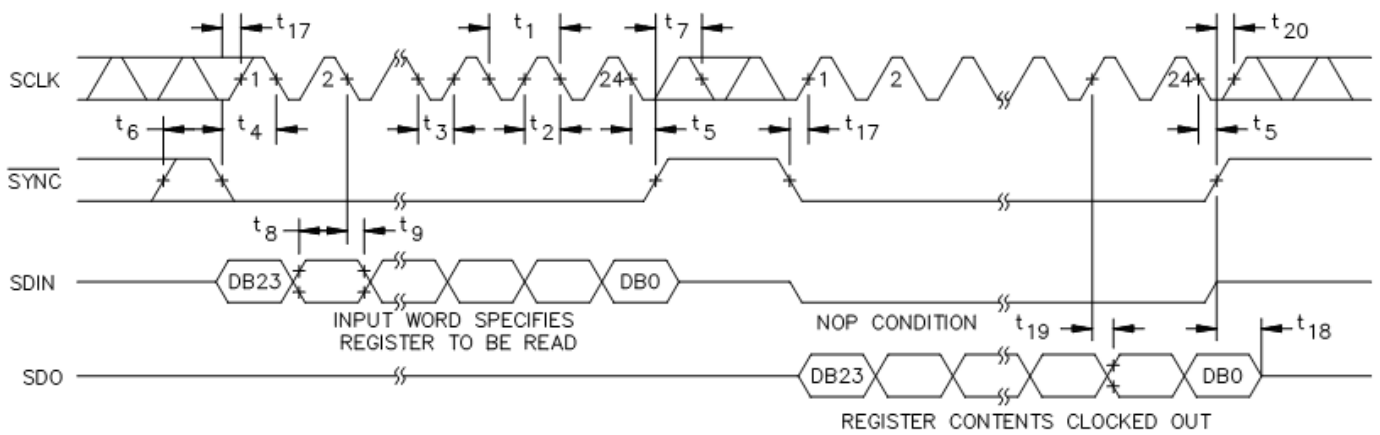


FIGURE 4. Readback mode timing diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <sup>1/</sup>	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/12664-01XB	24355	Tube, 75 units	AD5791SRU-EP
V62/12664-01XE	24355	Tube, 75 units	AD5791SRUZ-EP

<sup>1/</sup> The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices  
 Route 1 Industrial Park  
 P.O. Box 9106  
 Norwood, MA 02062  
 Point of contact: 20 Alpha Road  
 Chelmsford, MA 01824-4123

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