REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete all Daisy chain references under SCLK cycle time test and footnote 14/ as specified under Table I. Delete figure 5, Daisy chain mode timing diagram. - ro	13-10-03	C. SAFFLE
B	Add lead finish E device. Add Mode of transportation and quantity column under paragraph 6.3. - ro	18-03-02	C. SAFFLE
C	Update document paragraphs to current requirements. - ro	23-06-14	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

Original date of drawing
YY-MM-DD

13-06-18

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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, 18 BIT VOLTAGE OUTPUT DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. **V62/12661**

REV C

PAGE 1 OF 20

AMSC N/A

5962-V061-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 18 bit, voltage output digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12661	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5781	18 bit, voltage output digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-153-AC	Thin shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Positive analog supply voltage (V_{DD}) to analog ground reference (AGND)	-0.3 V to +34 V
Negative analog supply (V_{SS}) to AGND	-34 V to +0.3 V
V_{DD} to V_{SS}	-0.3 V to +34 V
Digital supply voltage (V_{CC}) to digital ground reference (DGND)	-0.3 V to +7 V
Digital interface supply (IOV_{CC}) to DGND	-0.3 V to V_{CC} + 3 V or +7 V (whichever is less)
Digital inputs to DGND	-0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
Analog output voltage (V_{OUT}) to AGND	-0.3 V to V_{DD} + 0.3 V
Positive reference force voltage (V_{REFPF}) to AGND	-0.3 V to V_{DD} + 0.3 V
Positive reference sense voltage (V_{REFPS}) to AGND	-0.3 V to V_{DD} + 0.3 V
Negative reference force voltage (V_{REFNF}) to AGND	V_{SS} – 0.3 V to + 0.3 V
Negative reference sense voltage (V_{REFNS}) to AGND	V_{SS} – 0.3 V to +0.3 V
DGND to AGND	-0.3 V to +0.3 V
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum junction temperature range (T_J)	+150°C
Power dissipation (P_D)	120 mW
Electrostatic discharge (ESD):	
Human body model (HBM)	1.5 kV

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (T_A)	-55°C to +125°C

1.5 Thermal characteristics.

Thermal resistance, junction to case (θ_{JC})	45°C/W
Thermal resistance, junction to ambient (θ_{JA})	143°C/W

_____

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Unless otherwise specified, T_A = +25°C. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 3 and 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance 4/							
Resolution			-55°C to +125°C	01	18		Bits
Integral nonlinearity error (relative accuracy)		V_{REFP} = +10 V, V_{REFN} = -10 V	-55°C to +125°C	01	-0.5	+0.5	LSB
					±0.25 typical		
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			-0.5	+0.5	
					±0.25 typical		
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			-1	+1	
					±0.5 typical		
Differential nonlinearity error		V_{REFP} = +10 V, V_{REFN} = -10 V	-55°C to +125°C	01	-0.5	+0.5	LSB
					±0.25 typical		
		V_{REFP} = +10 V, V_{REFN} = 0 V			-0.5	+0.5	
					±0.25 typical		
		V_{REFP} = +5 V, V_{REFN} = 0 V			-1	+1	
					±0.5 typical		
Linearity error long 6/ term stability		After 500 hours	+125°C	01	0.04 typical		LSB
		After 1,000 hours			0.05 typical		
		After 1,000 hours	+100°C		0.03 typical		
Full scale error	FSE	V_{REFP} = +10 V, V_{REFN} = -10 V 5/	-55°C to +125°C	01	-1.75	+1.75	LSB
					±0.25 typical		
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			-2.75	+2.75	
					±0.062 typical		
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			-5.25	+5.25	
					±0.2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance – continued.		4/					
Full scale error	FSE	V_{REFP} = +10 V, V_{REFN} = -10 V 5/	0°C to +105°C	01	-1	+1	LSB
					±0.25	typical	
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			-1	+1	
					±0.062	typical	
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			-1.5	+1.5	
					±0.2	typical	
Full scale error temperature coefficient			+25°C	01	±0.02	typical	ppm FSR/ °C
Zero scale error	ZSE	V_{REFP} = +10 V, V_{REFN} = -10 V 5/	-55°C to +125°C	01	-1.75	+1.75	LSB
					±0.025	typical	
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			-2.5	+2.5	
					±0.38	typical	
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			-5.25	+5.25	
					±0.19	typical	
		V_{REFP} = +10 V, V_{REFN} = -10 V 5/	0°C to +105°C		-1	+1	
					±0.025	typical	
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			-1	+1	
					±0.38	typical	
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			-1.5	+1.5	
					±0.19	typical	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance – continued. 4/							
Zero scale error 5/ temperature coefficient			+25°C	01	±0.04 typical		ppm FSR/ °C
Gain error	AE	V_{REFP} = +10 V, V_{REFN} = -10 V 5/	-55°C to +125°C	01	-6	+6	ppm
					±0.3 typical		FSR
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			-10	+10	
					±0.4 typical		
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			-20	+20	
					±0.4 typical		
Gain error 5/ temperature coefficient			+25°C	01	±0.04 typical		ppm FSR/ °C
R1, RFB matching			+25°C	01	0.01 typical		%
Output characteristics 5/							
Output voltage range			+25°C	01	V_{REFN}	V_{REFP}	V
Output slew rate		Unbuffered output, 10 MΩ||20 pF load 7/	+25°C	01	50 typical		V/μs
Output voltage settling time		10 V step to 0.02%, using AD845 buffer in unity gain mode	+25°C	01	1 typical		μs
		125 code step to ±1 LSB 8/			1 typical		
Output noise spectral density		At 1 kHz, DAC code = midscale	+25°C	01	7.5 typical		nV / $\sqrt{Hz}$
		At 10 kHz, DAC code = midscale			7.5 typical		
		At 100 kHz, DAC code = midscale			7.5 typical		
Output voltage noise		DAC code = midscale, 9/ 0.1 Hz to 10 Hz bandwidth	+25°C	01	1.1 typical		μVPP

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics - continued. 5/							
Midscale glitch impulse 10/		V_{REFP} = +10 V, V_{REFN} = -10 V 5/	+25°C	01	3.1 typical		nV-sec
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			1.7 typical		
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			1.4 typical		
MSB segment glitch impulse 10/		V_{REFP} = +10 V, V_{REFN} = -10 V 5/	+25°C	01	9.1 typical		nV-sec
		V_{REFP} = +10 V, V_{REFN} = 0 V 5/			3.6 typical		
		V_{REFP} = +5 V, V_{REFN} = 0 V 5/			1.9 typical		
Output enabled glitch impulse		On removal of output ground clamp	+25°C	01	45 typical		nV-sec
Digital feedthrough			+25°C	01	0.4 typical		nV-sec
DC output impedance (normal mode)			+25°C	01	3.4 typical		kΩ
DC output impedance (output clamped to ground)			+25°C	01	6 typical		kΩ
Spurious free dynamic range		1 kHz tone, 10 kHz sample rate	+25°C	01	100 typical		dB
Total harmonic distortion		1 kHz tone, 10 kHz sample rate	+25°C	01	97 typical		dB
Reference inputs 5/							
V_{REFP} input range			-55°C to +125°C	01	5	V_{DD} – 2.5	V
V_{REFN} input range			-55°C to +125°C	01	V_{SS} + 2.5 V	0	V
DC input impedance		V_{REFP}, V_{REFN}, code dependent, typical mid-scale code	-55°C to +125°C	01	5		kΩ
					6.6 typical		
Input capacitance	C_{IN}	V_{REFP}, V_{REFN}	+25°C	01	15 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic inputs 5/							
Input current 11/	I_{IN}		-55°C to +125°C	01	-1	+1	µA
Input low voltage	V_{IL}	IOV_{CC} = 1.71 V to 5.5 V	-55°C to +125°C	01		0.3 x IOV_{CC}	V
Input high voltage	V_{IH}	IOV_{CC} = 1.71 V to 5.5 V	-55°C to +125°C	01	0.7 x IOV_{CC}		V
Pin capacitance			+25°C	01	5 typical		pF
Logic output (SDO) 5/							
Output low voltage	V_{OL}	IOV_{CC} = 1.71 V to 5.5 V, sinking 1 mA	-55°C to +125°C	01		0.4	V
Output high voltage	V_{OH}	IOV_{CC} = 1.71 V to 5.5 V, sourcing 1 mA	-55°C to +125°C	01	IOV_{CC} – 0.5 V		V
High impedance leakage current			-55°C to +125°C	01		±1	µA
High impedance output capacitance			+25°C	01	3 typical		pF
Power requirements.		All digital inputs at DGND or IOV_{CC}					
Positive analog supply voltage	V_{DD}		-55°C to +125°C	01	7.5	V_{SS} + 33	V
Negative analog supply voltage	V_{SS}		-55°C to +125°C	01	V_{DD} - 33	-2.5	V
Digital supply voltage	V_{CC}		-55°C to +125°C	01	2.7	5.5	V
Digital interface supply voltage	IOV_{CC}	$IOV_{CC} \leq V_{CC}$	-55°C to +125°C	01	1.71	5.5	V
Positive analog supply current	I_{DD}		-55°C to +125°C	01		5.2	mA
					4.2 typical		
Negative analog supply current	I_{SS}		-55°C to +125°C	01		4.9	mA
					4 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power requirements - continued.		All digital inputs at DGND or IOV_{CC}					
Digital supply current	I_{CC}		-55°C to +125°C	01		900	µA
					600 typical		
Digital interface supply current	IOI_{CC}	SDO disabled	-55°C to +125°C	01		140	µA
					52 typical		
DC power supply rejection ratio 5/ 12/		V_{DD} ± 10%, V_{SS} = 15 V	+25°C	01	±0.6 typical		µV/V
		V_{SS} ± 10%, V_{DD} = 15 V			±0.6 typical		
AC power supply rejection ratio 5/ 12/		V_{DD} ± 200 mV, 50 Hz/60 Hz, V_{SS} = -15 V	+25°C	01	95 typical		dB
		V_{SS} ± 200 mV, 50 Hz/60 Hz, V_{DD} = 15 V			95 typical		
Timing requirements. 13/							
SCLK cycle time 14/	t_1	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	40		ns
		IOV_{CC} = 3.3 V to 5.5 V			28		
SCLK cycle time (readback mode)		IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	92		ns
		IOV_{CC} = 3.3 V to 5.5 V			60		
SCLK high time	t_2	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	15		ns
		IOV_{CC} = 3.3 V to 5.5 V			10		
SCLK low time	t_3	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	9		ns
		IOV_{CC} = 3.3 V to 5.5 V			5		
$\overline{SYNC}$ to SCLK falling edge setup time	t_4	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	5		ns
		IOV_{CC} = 3.3 V to 5.5 V			5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing requirements.	13/						
SCLK falling edge to $\overline{\text{SYNC}}$ rising edge hold time	t_5	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	2		ns
		IOV_{CC} = 3.3 V to 5.5 V			2		
Minimum $\overline{\text{SYNC}}$ high time	t_6	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	48		ns
		IOV_{CC} = 3.3 V to 5.5 V			40		
$\overline{\text{SYNC}}$ rising edge to next SCLK falling edge ignore	t_7	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	8		ns
		IOV_{CC} = 3.3 V to 5.5 V			6		
Data setup time	t_8	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	9		ns
		IOV_{CC} = 3.3 V to 5.5 V			7		
Data hold time	t_9	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	12		ns
		IOV_{CC} = 3.3 V to 5.5 V			7		
$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge	t_{10}	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	13		ns
		IOV_{CC} = 3.3 V to 5.5 V			10		
$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	t_{11}	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	20		ns
		IOV_{CC} = 3.3 V to 5.5 V			16		
$\overline{\text{LDAC}}$ pulse width low	t_{12}	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	14		ns
		IOV_{CC} = 3.3 V to 5.5 V			11		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued. 13/							
$\overline{LDAC}$ falling edge to output response time	t_{13}	IOV_{CC} = 1.71 V to 3.3 V	+25°C	01	130 typical		ns
		IOV_{CC} = 3.3 V to 5.5 V			130 typical		
$\overline{SYNC}$ rising edge to output response time ($\overline{LDAC}$ tied low)	t_{14}	IOV_{CC} = 1.71 V to 3.3 V	+25°C	01	130 typical		ns
		IOV_{CC} = 3.3 V to 5.5 V			130 typical		
$\overline{CLR}$ pulse width low	t_{15}	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	50		ns
		IOV_{CC} = 3.3 V to 5.5 V			50		
$\overline{CLR}$ pulse activation time	t_{16}	IOV_{CC} = 1.71 V to 3.3 V	+25°C	01	140 typical		ns
		IOV_{CC} = 3.3 V to 5.5 V			140 typical		
$\overline{SYNC}$ falling edge to first SCLK rising edge	t_{17}	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	0		ns
		IOV_{CC} = 3.3 V to 5.5 V			0		
$\overline{SYNC}$ rising edge to SDO tristate	t_{18}	IOV_{CC} = 1.71 V to 3.3 V, C_L = 50 pF	-55°C to +125°C	01		65	ns
		IOV_{CC} = 3.3 V to 5.5 V, C_L = 50 pF				60	
SCLK rising edge to SDO valid	t_{19}	IOV_{CC} = 1.71 V to 3.3 V, C_L = 50 pF	-55°C to +125°C	01		62	ns
		IOV_{CC} = 3.3 V to 5.5 V, C_L = 50 pF				45	
$\overline{SYNC}$ rising edge to SCLK rising edge ignore	t_{20}	IOV_{CC} = 1.71 V to 3.3 V	-55°C to +125°C	01	0		ns
		IOV_{CC} = 3.3 V to 5.5 V			0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued. 13/							
$\overline{\text{RESET}}$ pulse width low	t_{21}	IOV_{CC} = 1.71 V to 3.3 V	+25°C	01	35 typical		ns
		IOV_{CC} = 3.3 V to 5.5 V			35 typical		
$\overline{\text{RESET}}$ pulse activation time	t_{22}	IOV_{CC} = 1.71 V to 3.3 V	+25°C	01	150 typical		ns
		IOV_{CC} = 3.3 V to 5.5 V			150 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = +12.5 V to +16.5 V, V_{SS} = -16.5 V to -12.5 V, V_{REFP} = +10 V, V_{REFN} = -10 V, V_{CC} = +2.7 V to +5.5 V, IOV_{CC} = +1.71 V to +5.5 V, R_L = unloaded, and C_L = unloaded.

3/ Unless otherwise specified, for typical conditions, T_A = +25°C, V_{DD} = +15 V, V_{SS} = -15 V, V_{REFP} = +10 V, and V_{REFN} = -10 V.

4/ Performance characterized with AD8676BRZ voltage reference buffers and AD8675ARZ output buffer.

5/ Guaranteed by design and characterization; not production tested.

6/ Linearity error refers to both INL error and DNL error; either parameter can be expected to drift by the amount specified after the length of time specified.

7/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

8/ The device configured in x2 gain mode, 25 pF compensation capacitor on AD797.

9/ Includes noise contribution from AD8676BRZ voltage reference buffers.

10/ The device is configured in the bias compensation mode with a low pass RC filter on the output. R = 300 Ω, C = 143 pF (total capacitance seen by the output buffer, lead capacitance).

11/ Current flowing in an individual logic pin.

12/ Includes PSRR of AD8676BRZ voltage reference buffers.

13/ All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{CC}) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.

14/ Maximum SCLK frequency is 35 MHz for write mode and 16 MHz for readback mode.

Case X

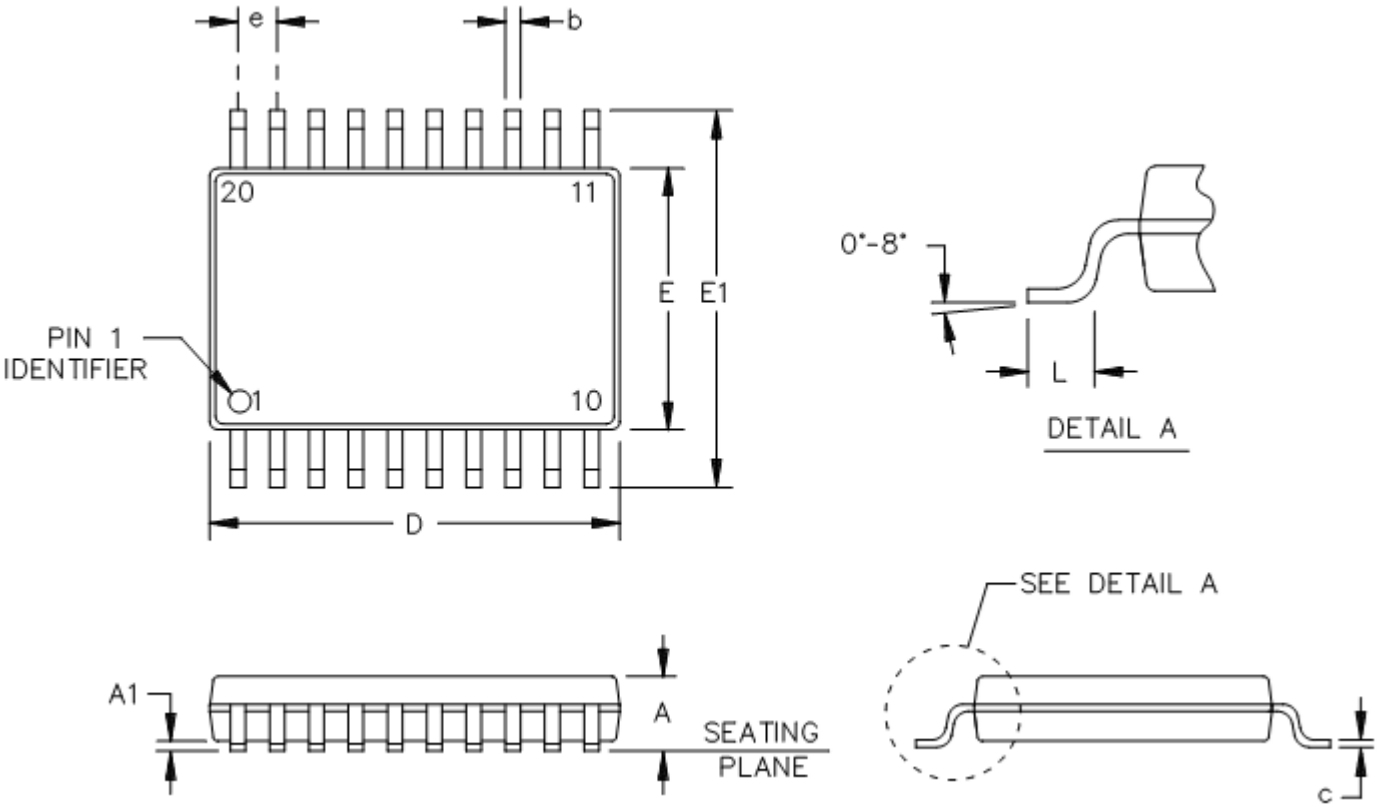

FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.003	.007	0.09	0.20
D	.251	.259	6.40	6.60
E	.169	.177	4.30	4.50
E1	.251 BSC		6.40 BSC	
e	.025 BSC		0.65 BSC	
L	.017	.029	0.45	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AC.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	INV	Connection to inverting input of external amplifier.
2	V_{OUT}	Analog output voltage.
3	V_{REFPS}	Positive reference sense voltage input. A voltage range of 5 V to V_{DD} – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V_{REFPF} pin.
4	V_{REFPF}	Positive reference force voltage input. A voltage range of 5 V to V_{DD} – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V_{REFPS} pin.
5	V_{DD}	Positive analog supply connection. A voltage range of 7.5 V to 16.5 V can be connected. V_{DD} should be decoupled to AGND.
6	$\overline{RESET}$	Active low reset logic input pin. Asserting this pin returns the device to its power on status.
7	$\overline{CLR}$	Active low clear logic input pin. Asserting this pin sets the DAC register to a user defined value and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
8	$\overline{LDAC}$	Active low load DAC input pin. This is used to update the DAC register and, consequently, the analog output. When tied permanently low, the output is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the input register is updated, but the output is held off until the falling edge of $\overline{LDAC}$. The $\overline{LDAC}$ pin should not be left unconnected.
9	V_{CC}	Digital supply connection. A voltage in the range of 2.7 V to 5.5 V can be connected. V_{CC} should be decoupled to DGND.
10	IOV_{CC}	Digital interface supply pin. Digital threshold levels are referenced to the voltage applied to this pin. A voltage range of 1.71 V to 5.5 V can be connected. IOV_{CC} should not be allowed to exceed V_{CC}.

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
11	SDO	Serial data output pin. Data is clocked out on the rising edge of the serial clock input.
12	SDIN	Serial data input pin. This device has a 24 bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock rates of up to 35 MHz.
14	$\overline{\text{SYNC}}$	Active low digital interface synchronization input pin. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ is low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The input shift register is updated on the rising edge of $\overline{\text{SYNC}}$.
15	DGND	Ground reference pin for digital circuitry.
16	V_{REFNF}	Negative reference force voltage input. A voltage range of V_{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V_{REFNS} pin.
17	V_{REFNS}	Negative reference sense voltage input. A voltage range of V_{SS} + 2.5 V to 0 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the V_{REFNF} pin.
18	V_{SS}	Negative analog supply connection. A voltage range of -16.5 V to -2.5 V can be connected. V_{SS} should be decoupled to AGND.
19	AGND	Ground reference pin for analog circuitry.
20	R_{FB}	Feedback connection for external amplifier.

FIGURE 2. Terminal connections - continued.

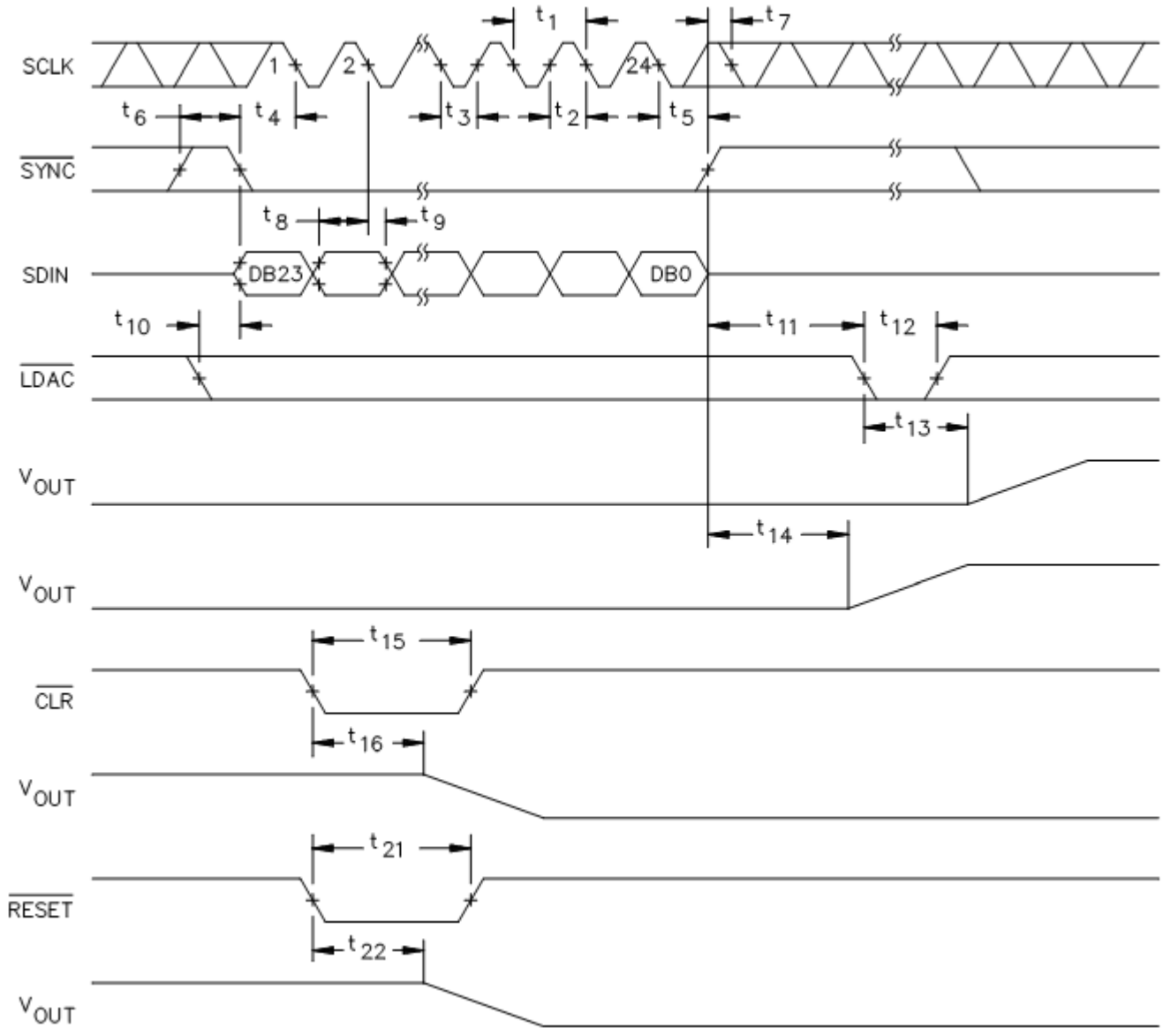

FIGURE 3. Write mode timing diagram.

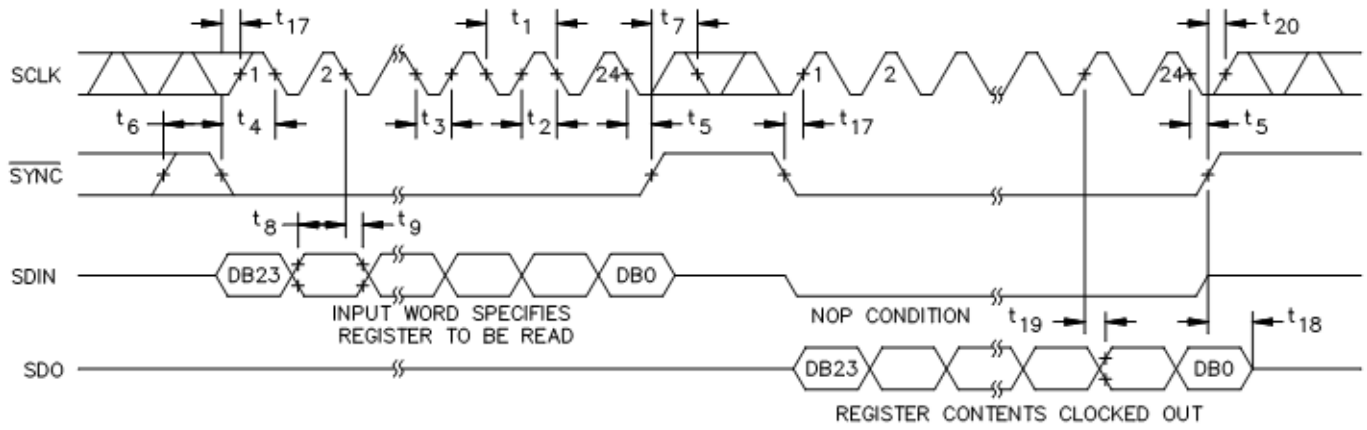

FIGURE 4. Readback mode timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/12661-01XB	24355	Tube, 75 units	AD5781SRU-EP
V62/12661-01XE	24355	Tube, 75 units	AD5781SRUZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123