

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Delete all Daisy chain references under SCLK cycle time test and footnote 14/ as specified under Table I. Delete figure 5, Daisy chain mode timing diagram. - ro	13-10-03	C. SAFFLE
B	Add lead finish E device. Add Mode of transportation and quantity column under paragraph 6.3. - ro	18-03-02	C. SAFFLE



Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B																		
PAGE	18	19	20																		
REV STATUS OF PAGES	REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.dla.mil/landandmaritime
Original date of drawing YY-MM-DD 13-06-18	CHECKED BY RAJESH PITHADIA	MICROCIRCUIT, DIGITAL-LINEAR, 18 BIT, VOLTAGE OUTPUT DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE A	CODE IDENT. NO. 16236
	REV B	PAGE 1 OF 20

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 18 bit, voltage output digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/12661</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>B</u> Lead finish (See 1.2.3)
--	---	--	--	---

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD5781	18 bit, voltage output digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-153-AC	Thin shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 2

1.3 Absolute maximum ratings. 1/ 2/

Positive analog supply voltage (VDD) to analog ground reference (AGND)	-0.3 V to +34 V
Negative analog supply (VSS) to AGND	-34 V to +0.3 V
VDD to VSS	-0.3 V to +34 V
Digital supply voltage (VCC) to digital ground reference (DGND)	-0.3 V to +7 V
Digital interface supply (IOVCC) to DGND	-0.3 V to VCC + 3 V or +7 V (whichever is less)
Digital inputs to DGND	-0.3 V to IOVCC + 0.3 V or +7 V (whichever is less)
Analog output voltage (VOUT) to AGND	-0.3 V to VDD + 0.3 V
Positive reference force voltage (VREFPF) to AGND	-0.3 V to VDD + 0.3 V
Positive reference sense voltage (VREFPS) to AGND	-0.3 V to VDD + 0.3 V
Negative reference force voltage (VREFNF) to AGND	VSS – 0.3 V to + 0.3 V
Negative reference sense voltage (VREFNS) to AGND	VSS – 0.3 V to +0.3 V
DGND to AGND	-0.3 V to +0.3 V
Storage temperature range (TSTG)	-65°C to +150°C
Maximum junction temperature range (TJ)	+150°C
Power dissipation (PD)	120 mW
Electrostatic discharge (ESD):	
Human body model (HBM)	1.5 kV

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (TA)	-55°C to +125°C
---	-----------------

1.5 Thermal characteristics.

Thermal resistance, junction to case (θJC)	45°C/W
Thermal resistance, junction to ambient (θJA)	143°C/W

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - 2/ Unless otherwise specified, TA = +25°C. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.
 - 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at <https://www.jedec.org>).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figures 3 and 4.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u> <u>3/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Static performance <u>4/</u>							
Resolution			-55°C to +125°C	01	18		Bits
Integral nonlinearity error (relative accuracy)		V _{REFP} = +10 V, V _{REFN} = -10 V	-55°C to +125°C	01	-0.5	+0.5	LSB
					±0.25 typical		
		V _{REFP} = +10 V, V _{REFN} = 0 V <u>5/</u>			-0.5	+0.5	
					±0.25 typical		
		V _{REFP} = +5 V, V _{REFN} = 0 V <u>5/</u>			-1	+1	
		±0.5 typical					
Differential nonlinearity error		V _{REFP} = +10 V, V _{REFN} = -10 V	-55°C to +125°C	01	-0.5	+0.5	LSB
					±0.25 typical		
		V _{REFP} = +10 V, V _{REFN} = 0 V			-0.5	+0.5	
					±0.25 typical		
		V _{REFP} = +5 V, V _{REFN} = 0 V			-1	+1	
		±0.5 typical					
Linearity error long <u>6/</u> term stability		After 500 hours	+125°C	01	0.04 typical		LSB
		After 1,000 hours			0.05 typical		
		After 1,000 hours	+100°C		0.03 typical		
Full scale error	FSE	V _{REFP} = +10 V, V _{REFN} = -10 V <u>5/</u>	-55°C to +125°C	01	-1.75	+1.75	LSB
					±0.25 typical		
		V _{REFP} = +10 V, V _{REFN} = 0 V <u>5/</u>			-2.75	+2.75	
					±0.062 typical		
		V _{REFP} = +5 V, V _{REFN} = 0 V <u>5/</u>			-5.25	+5.25	
		±0.2 typical					

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Static performance – continued. <u>4/</u>							
Full scale error	FSE	V _{REFP} = +10 V, V _{REFN} = -10 V <u>5/</u>	0°C to +105°C	01	-1	+1	LSB
					±0.25 typical		
		V _{REFP} = +10 V, V _{REFN} = 0 V <u>5/</u>			-1	+1	
					±0.062 typical		
		V _{REFP} = +5 V, V _{REFN} = 0 V <u>5/</u>			-1.5	+1.5	
	±0.2 typical						
Full scale error temperature coefficient			+25°C	01	±0.02 typical		ppm FSR/ °C
Zero scale error	ZSE	V _{REFP} = +10 V, V _{REFN} = -10 V <u>5/</u>	-55°C to +125°C	01	-1.75	+1.75	LSB
					±0.025 typical		
		V _{REFP} = +10 V, V _{REFN} = 0 V <u>5/</u>			-2.5	+2.5	
					±0.38 typical		
		V _{REFP} = +5 V, V _{REFN} = 0 V <u>5/</u>			-5.25	+5.25	
			±0.19 typical				
		V _{REFP} = +10 V, V _{REFN} = -10 V <u>5/</u>	0°C to +105°C		-1	+1	
					±0.025 typical		
		V _{REFP} = +10 V, V _{REFN} = 0 V <u>5/</u>			-1	+1	
					±0.38 typical		
V _{REFP} = +5 V, V _{REFN} = 0 V <u>5/</u>	-1.5	+1.5					
	±0.19 typical						

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 6

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Static performance – continued. <u>4/</u>							
Zero scale error <u>5/</u> temperature coefficient			+25°C	01	±0.04 typical		ppm FSR/ °C
Gain error	AE	V _{REFP} = +10 V, V _{REFN} = -10 V <u>5/</u>	-55°C to +125°C	01	-6	+6	ppm FSR
					±0.3 typical		
		-10			+10		
		±0.4 typical					
		-20			+20		
±0.4 typical							
V _{REFP} = +10 V, V _{REFN} = 0 V <u>5/</u>							
V _{REFP} = +5 V, V _{REFN} = 0 V <u>5/</u>							
Gain error <u>5/</u> temperature coefficient			+25°C	01	±0.04 typical		ppm FSR/ °C
R1, RFB matching			+25°C	01	0.01 typical		%
Output characteristics <u>5/</u>							
Output voltage range			+25°C	01	V _{REFN}	V _{REFP}	V
Output slew rate		Unbuffered output, 10 MΩ 20 pF load <u>7/</u>	+25°C	01	50 typical		V/μs
Output voltage settling time		10 V step to 0.02%, using AD845 buffer in unity gain mode	+25°C	01	1 typical		μs
		125 code step to ±1 LSB <u>8/</u>			1 typical		
Output noise spectral density		At 1 kHz, DAC code = midscale	+25°C	01	7.5 typical		nV / √Hz
		At 10 kHz, DAC code = midscale			7.5 typical		
		At 100 kHz, DAC code = midscale			7.5 typical		
Output voltage noise		DAC code = midscale, 0.1 Hz to 10 Hz bandwidth <u>9/</u>	+25°C	01	1.1 typical		μV _{PP}

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 7

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Output characteristics - continued. <u>5/</u>							
Midscale glitch impulse <u>10/</u>		VREFP = +10 V, VREFN = -10 V <u>5/</u>	+25°C	01	3.1 typical		nV-sec
		VREFP = +10 V, VREFN = 0 V <u>5/</u>			1.7 typical		
		VREFP = +5 V, VREFN = 0 V <u>5/</u>			1.4 typical		
MSB segment glitch impulse <u>10/</u>		VREFP = +10 V, VREFN = -10 V <u>5/</u>	+25°C	01	9.1 typical		nV-sec
		VREFP = +10 V, VREFN = 0 V <u>5/</u>			3.6 typical		
		VREFP = +5 V, VREFN = 0 V <u>5/</u>			1.9 typical		
Output enabled glitch impulse		On removal of output ground clamp	+25°C	01	45 typical		nV-sec
Digital feedthrough			+25°C	01	0.4 typical		nV-sec
DC output impedance (normal mode)			+25°C	01	3.4 typical		kΩ
DC output impedance (output clamped to ground)			+25°C	01	6 typical		kΩ
Spurious free dynamic range		1 kHz tone, 10 kHz sample rate	+25°C	01	100 typical		dB
Total harmonic distortion		1 kHz tone, 10 kHz sample rate	+25°C	01	97 typical		dB
Reference inputs <u>5/</u>							
VREFP input range			-55°C to +125°C	01	5	V _{DD} - 2.5	V
VREFN input range			-55°C to +125°C	01	V _{SS} + 2.5 V	0	V
DC input impedance		VREFP, VREFN, code dependent, typical mid-scale code	-55°C to +125°C	01	5		kΩ
					6.6 typical		
Input capacitance	C _{IN}	VREFP, VREFN	+25°C	01	15 typical		pF

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 8

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Logic inputs <u>5/</u>							
Input current <u>11/</u>	I _{IN}		-55°C to +125°C	01	-1	+1	μA
Input low voltage	V _{IL}	IOVCC = 1.71 V to 5.5 V	-55°C to +125°C	01		0.3 x IOVCC	V
Input high voltage	V _{IH}	IOVCC = 1.71 V to 5.5 V	-55°C to +125°C	01	0.7 x IOVCC		V
Pin capacitance			+25°C	01	5 typical		pF
Logic output (SDO) <u>5/</u>							
Output low voltage	V _{OL}	IOVCC = 1.71 V to 5.5 V, sinking 1 mA	-55°C to +125°C	01		0.4	V
Output high voltage	V _{OH}	IOVCC = 1.71 V to 5.5 V, sourcing 1 mA	-55°C to +125°C	01	IOVCC – 0.5 V		V
High impedance leakage current			-55°C to +125°C	01		±1	μA
High impedance output capacitance			+25°C	01	3 typical		pF
Power requirements. All digital inputs at DGND or IOVCC							
Positive analog supply voltage	V _{DD}		-55°C to +125°C	01	7.5	V _{SS} + 33	V
Negative analog supply voltage	V _{SS}		-55°C to +125°C	01	V _{DD} - 33	-2.5	V
Digital supply voltage	V _{CC}		-55°C to +125°C	01	2.7	5.5	V
Digital interface supply voltage	IOVCC	IOVCC ≤ V _{CC}	-55°C to +125°C	01	1.71	5.5	V
Positive analog supply current	I _{DD}		-55°C to +125°C	01		5.2	mA
					4.2 typical		
Negative analog supply current	I _{SS}		-55°C to +125°C	01		4.9	mA
					4 typical		

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 9

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Power requirements - continued. All digital inputs at DGND or IOVCC							
Digital supply current	I _{CC}		-55°C to +125°C	01		900	μA
					600 typical		
Digital interface supply current	IO _{CC}	SDO disabled	-55°C to +125°C	01		140	μA
					52 typical		
DC power <u>5/ 12/</u> supply rejection ratio		VDD ± 10%, VSS = 15 V	+25°C	01	±0.6 typical		μV/V
		VSS ± 10%, VDD = 15 V			±0.6 typical		
AC power <u>5/ 12/</u> supply rejection ratio		VDD ± 200 mV, 50 Hz/60 Hz, VSS = -15 V	+25°C	01	95 typical		dB
		VSS ± 200 mV, 50 Hz/60 Hz, VDD = 15 V			95 typical		
Timing requirements. <u>13/</u>							
SCLK cycle time <u>14/</u>	t ₁	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	40		ns
		IOVCC = 3.3 V to 5.5 V			28		
SCLK cycle time (readback mode)		IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	92		ns
		IOVCC = 3.3 V to 5.5 V			60		
SCLK high time	t ₂	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	15		ns
		IOVCC = 3.3 V to 5.5 V			10		
SCLK low time	t ₃	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	9		ns
		IOVCC = 3.3 V to 5.5 V			5		
$\overline{\text{SYNC}}$ to SCLK falling edge setup time	t ₄	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	5		ns
		IOVCC = 3.3 V to 5.5 V			5		

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 10

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Timing requirements. <u>13/</u>							
SCLK falling edge to $\overline{\text{SYNC}}$ rising edge hold time	t5	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	2		ns
		IOVCC = 3.3 V to 5.5 V			2		
Minimum $\overline{\text{SYNC}}$ high time	t6	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	48		ns
		IOVCC = 3.3 V to 5.5 V			40		
$\overline{\text{SYNC}}$ rising edge to next SCLK falling edge ignore	t7	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	8		ns
		IOVCC = 3.3 V to 5.5 V			6		
Data setup time	t8	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	9		ns
		IOVCC = 3.3 V to 5.5 V			7		
Data hold time	t9	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	12		ns
		IOVCC = 3.3 V to 5.5 V			7		
$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ falling edge	t10	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	13		ns
		IOVCC = 3.3 V to 5.5 V			10		
$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	t11	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	20		ns
		IOVCC = 3.3 V to 5.5 V			16		
$\overline{\text{LDAC}}$ pulse width low	t12	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	14		ns
		IOVCC = 3.3 V to 5.5 V			11		

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 11

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued. <u>13/</u>							
$\overline{\text{LDAC}}$ falling edge to output response time	t13	IOVCC = 1.71 V to 3.3 V	+25°C	01	130 typical		ns
		IOVCC = 3.3 V to 5.5 V			130 typical		
$\overline{\text{SYNC}}$ rising edge to output response time ($\overline{\text{LDAC}}$ tied low)	t14	IOVCC = 1.71 V to 3.3 V	+25°C	01	130 typical		ns
		IOVCC = 3.3 V to 5.5 V			130 typical		
$\overline{\text{CLR}}$ pulse width low	t15	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	50		ns
		IOVCC = 3.3 V to 5.5 V			50		
$\overline{\text{CLR}}$ pulse activation time	t16	IOVCC = 1.71 V to 3.3 V	+25°C	01	140 typical		ns
		IOVCC = 3.3 V to 5.5 V			140 typical		
$\overline{\text{SYNC}}$ falling edge to first SCLK rising edge	t17	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	0		ns
		IOVCC = 3.3 V to 5.5 V			0		
$\overline{\text{SYNC}}$ rising edge to SDO tristate	t18	IOVCC = 1.71 V to 3.3 V, CL = 50 pF	-55°C to +125°C	01		65	ns
		IOVCC = 3.3 V to 5.5 V, CL = 50 pF				60	
SCLK rising edge to SDO valid	t19	IOVCC = 1.71 V to 3.3 V, CL = 50 pF	-55°C to +125°C	01		62	ns
		IOVCC = 3.3 V to 5.5 V, CL = 50 pF				45	
$\overline{\text{SYNC}}$ rising edge to SCLK rising edge ignore	t20	IOVCC = 1.71 V to 3.3 V	-55°C to +125°C	01	0		ns
		IOVCC = 3.3 V to 5.5 V			0		

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 12

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Timing requirements – continued. <u>13/</u>							
$\overline{\text{RESET}}$ pulse width low	t21	IOVCC = 1.71 V to 3.3 V	+25°C	01	35 typical		ns
		IOVCC = 3.3 V to 5.5 V			35 typical		
$\overline{\text{RESET}}$ pulse activation time	t22	IOVCC = 1.71 V to 3.3 V	+25°C	01	150 typical		ns
		IOVCC = 3.3 V to 5.5 V			150 typical		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, V_{DD} = +12.5 V to +16.5 V, V_{SS} = -16.5 V to -12.5 V, V_{REFP} = +10 V, V_{REFN} = -10 V, V_{CC} = +2.7 V to +5.5 V, IOVCC = +1.71 V to +5.5 V, R_L = unloaded, and C_L = unloaded.
- 3/ Unless otherwise specified, for typical conditions, T_A = +25°C, V_{DD} = +15 V, V_{SS} = -15 V, V_{REFP} = +10 V, and V_{REFN} = -10 V.
- 4/ Performance characterized with AD8676BRZ voltage reference buffers and AD8675ARZ output buffer.
- 5/ Guaranteed by design and characterization; not production tested.
- 6/ Linearity error refers to both INL error and DNL error; either parameter can be expected to drift by the amount specified after the length of time specified.
- 7/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.
- 8/ The device configured in x2 gain mode, 25 pF compensation capacitor on AD797.
- 9/ Includes noise contribution from AD8676BRZ voltage reference buffers.
- 10/ The device is configured in the bias compensation mode with a low pass RC filter on the output.
R = 300 Ω, C = 143 pF (total capacitance seen by the output buffer, lead capacitance).
- 11/ Current flowing in an individual logic pin.
- 12/ Includes PSRR of AD8676BRZ voltage reference buffers.
- 13/ All input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOVCC) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
- 14/ Maximum SCLK frequency is 35 MHz for write mode and 16 MHz for readback mode.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 13

Case X

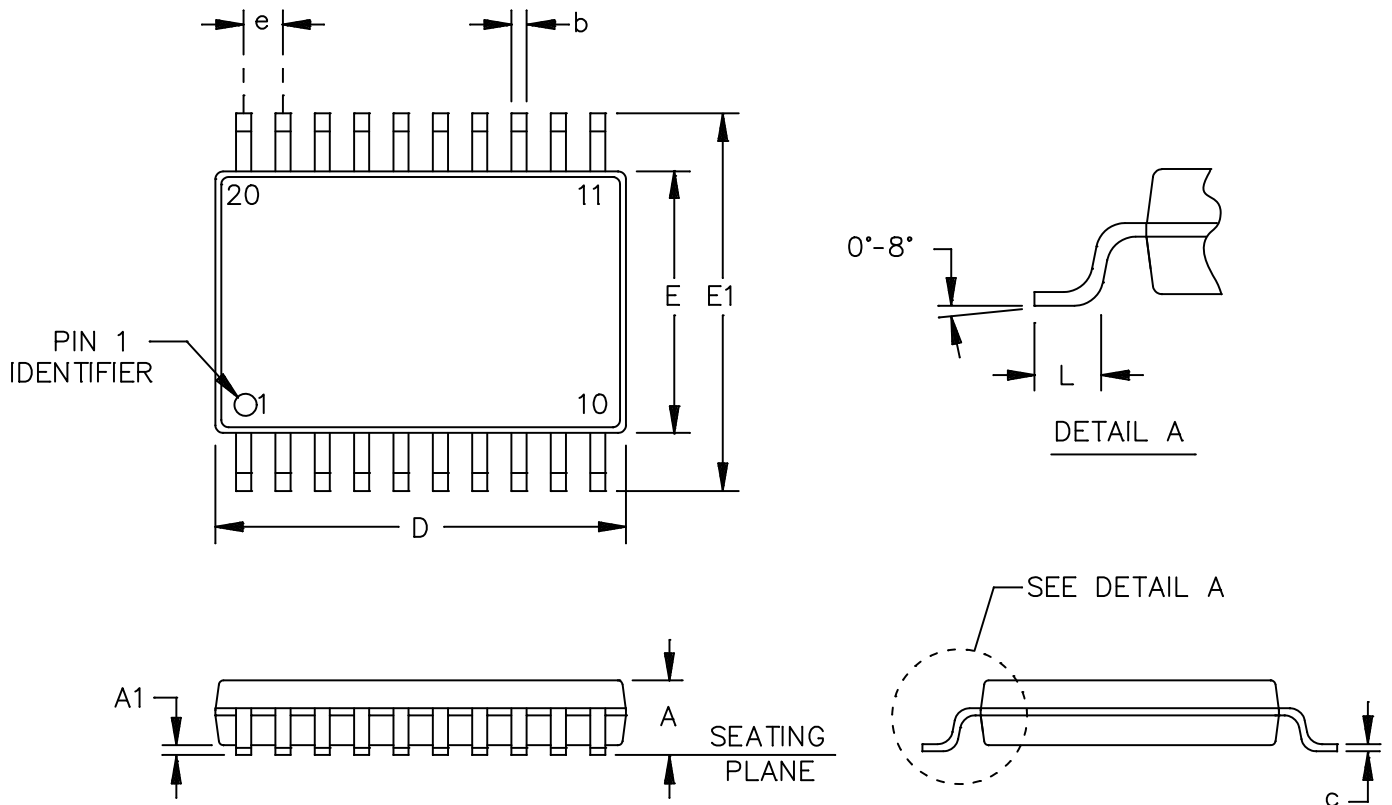


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/12661</p>
		<p>REV B</p>	<p>PAGE 14</p>

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.003	.007	0.09	0.20
D	.251	.259	6.40	6.60
E	.169	.177	4.30	4.50
E1	.251 BSC		6.40 BSC	
e	.025 BSC		0.65 BSC	
L	.017	.029	0.45	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AC.

FIGURE 1. Case outline - Continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 15

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	INV	Connection to inverting input of external amplifier.
2	VOUT	Analog output voltage.
3	VREFPS	Positive reference sense voltage input. A voltage range of 5 V to VDD – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFPF pin.
4	VREFPF	Positive reference force voltage input. A voltage range of 5 V to VDD – 2.5 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFPS pin.
5	VDD	Positive analog supply connection. A voltage range of 7.5 V to 16.5 V can be connected. VDD should be decoupled to AGND.
6	$\overline{\text{RESET}}$	Active low reset logic input pin. Asserting this pin returns the device to its power on status.
7	$\overline{\text{CLR}}$	Active low clear logic input pin. Asserting this pin sets the DAC register to a user defined value and updates the DAC output. The output value depends on the DAC register coding that is being used, either binary or twos complement.
8	$\overline{\text{LDAC}}$	Active low load DAC input pin. This is used to update the DAC register and, consequently, the analog output. When tied permanently low, the output is updated on the rising edge of $\overline{\text{SYNC}}$. If $\overline{\text{LDAC}}$ is held high during the write cycle, the input register is updated, but the output is held off until the falling edge of $\overline{\text{LDAC}}$. The $\overline{\text{LDAC}}$ pin should not be left unconnected.
9	VCC	Digital supply connection. A voltage in the range of 2.7 V to 5.5 V can be connected. VCC should be decoupled to DGND.
10	IOVCC	Digital interface supply pin. Digital threshold levels are referenced to the voltage applied to this pin. A voltage range of 1.71 V to 5.5 V can be connected. IOVCC should not be allowed to exceed VCC.

FIGURE 2. Terminal connections.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 16

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
11	SDO	Serial data output pin. Data is clocked out on the rising edge of the serial clock input.
12	SDIN	Serial data input pin. This device has a 24 bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock rates of up to 35 MHz.
14	$\overline{\text{SYNC}}$	Active low digital interface synchronization input pin. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ is low, it enables the input shift register, and data is then transferred in on the falling edges of the following clocks. The input shift register is updated on the rising edge of $\overline{\text{SYNC}}$.
15	DGND	Ground reference pin for digital circuitry.
16	VREFNF	Negative reference force voltage input. A voltage range of $V_{SS} + 2.5 \text{ V}$ to 0 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFNS pin.
17	VREFNS	Negative reference sense voltage input. A voltage range of $V_{SS} + 2.5 \text{ V}$ to 0 V can be connected. A unity gain amplifier must be connected at this pin, in conjunction with the VREFNF pin.
18	VSS	Negative analog supply connection. A voltage range of -16.5 V to -2.5 V can be connected. VSS should be decoupled to AGND.
19	AGND	Ground reference pin for analog circuitry.
20	RFB	Feedback connection for external amplifier.

FIGURE 2. Terminal connections - continued.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 17

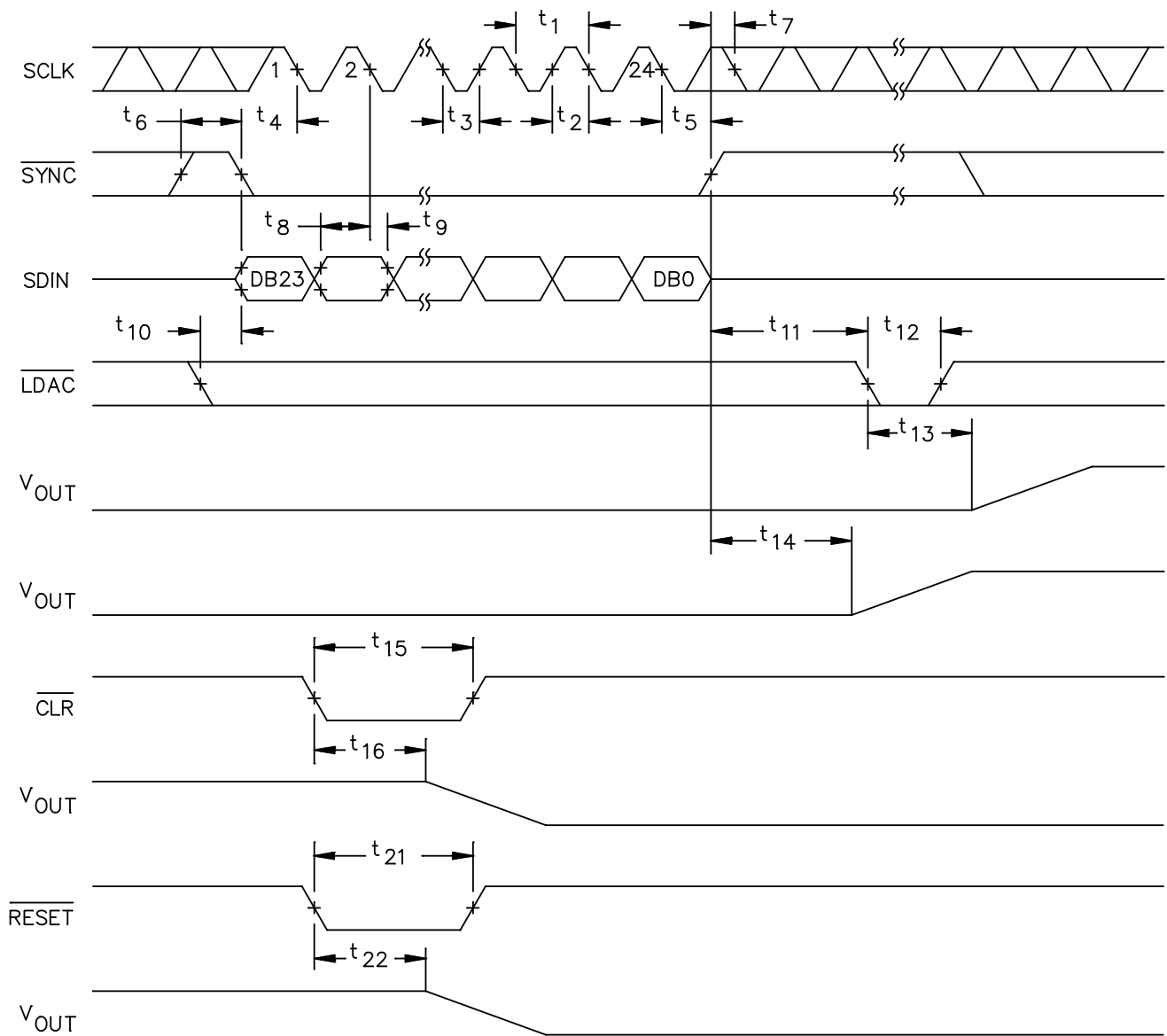


FIGURE 3. Write mode timing diagram.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/12661</p>
		<p align="center">REV B</p>	<p align="center">PAGE 18</p>

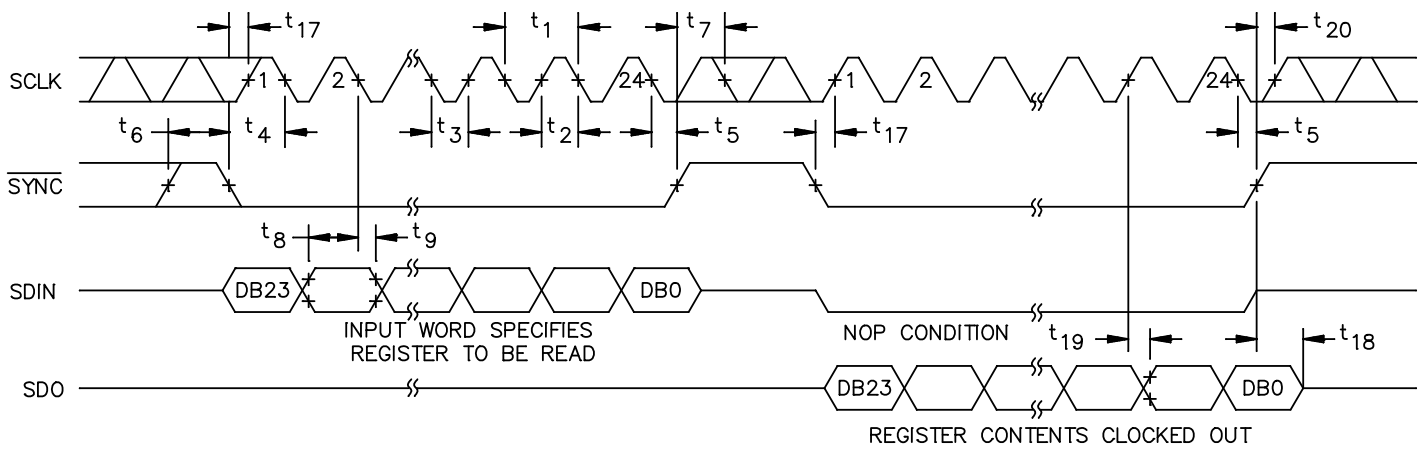


FIGURE 4. Readback mode timing diagram.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/12661</p>
		<p align="center">REV B</p>	<p align="center">PAGE 19</p>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/12661-01XB	24355	Tube, 75 units	AD5781SRU-EP
V62/12661-01XE	24355	Tube, 75 units	AD5781SRUZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: Raheen Business Park
 Limerick, Ireland

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12661
		REV B	PAGE 20