| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
| | | | |

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | |
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| **REV STATUS OF PAGES** | **REV** | | | | | | | | | | | | | | | | | | | | |
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|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>RICK OFFICER | **DLA LAND AND MARITIME**<br>**COLUMBUS, OHIO 43218-3990**<br>**http://www.landandmaritime.dla.mil/** |
| Original date of drawing<br>YY-MM-DD<br>13-01-10 | **CHECKED BY**<br>RAJESH PITHADIA | **TITLE**<br>MICROCIRCUIT, DIGITAL-LINEAR, 16 BIT, 65 MSPS, 1.8 V ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON |
| | **APPROVED BY**<br>CHARLES F. SAFFLE | |
| | **SIZE**<br>**A**<br>**CODE IDENT. NO.**<br>**16236** | **DWG NO.**<br>**V62/12660** |
| | **REV** | **PAGE** 1 **OF** 17 |

AMSC N/A

5962-V001-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 bit, 65 million samples per second (MSPS), 1.8 V analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/12660 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | AD9266 | 16 bit, 65 MSPS, 1.8 V analog to digital converter |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 32 | MO-220-WHHD-5 | Thin quad chip carrier |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Analog voltage 1.8 V ($AV_{DD}$) to analog ground (AGND) ..... -0.3 V to +2.0 V
Voltage supply for driver domain ($DRV_{DD}$) to AGND ..... -0.3 V to +3.9 V
Positive analog input ($+V_{IN}$), negative analog input ($-V_{IN}$) to AGND ..... -0.3 V to $AV_{DD}$ + 0.2 V
Clock input (+CLK), clock input (-CLK) to AGND ..... -0.3 V to $AV_{DD}$ + 0.2 V
Reference voltage ($V_{REF}$) to AGND ..... -0.3 V to $AV_{DD}$ + 0.2 V
Reference selection (SENSE) to AGND ..... -0.3 V to $AV_{DD}$ + 0.2 V
Analog output voltage ($V_{CM}$) to AGND ..... -0.3 V to $AV_{DD}$ + 0.2 V
Set analog current bias (RBIAS) to AGND ..... -0.3 V to $AV_{DD}$ + 0.2 V
Serial port interface (SPI) chip select (CSB) to AGND ..... -0.3 V to $DRV_{DD}$ + 0.3 V
SPI clock input (SCLK) / data format selection (DFS) to AGND ..... -0.3 V to $DRV_{DD}$ + 0.3 V
SPI data input/output (SDIO) / non-SPI mode power down (PDWN) to AGND ..... -0.3 V to $DRV_{DD}$ + o.3 V
Chip mode select input (MODE) / out of range digital output in SPI mode (OR) to AGND ..... -0.3 V to $DRV_{DD}$ + 0.3 V
ADC digital outputs (D1_D0 through D15_D14) to AGND ..... -0.3 V to $DRV_{DD}$ + 0.3 V
Data clock digital output (DCO) to AGND ..... -0.3 V to $DRV_{DD}$ + 0.3 V
Maximum junction temperature under bias ($T_J$) ..... 150°C
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range ($T_A$) ..... -55°C to +125°C

1.5 Thermal characteristics.

| Thermal metric | Symbol | Case X | | | Unit |
|---|---|---|---|---|---|
| Airflow velocity | | 0 | 1.0 | 2.5 | m/sec |
| Thermal resistance, junction-to-ambient 3/ 4/ | $\theta_{JA}$ | 37.1 | 32.4 | 29.1 | °C/W |
| Thermal resistance, junction-to-case 3/ 5/ | $\theta_{JC}$ | 3.1 | --- | --- | °C/W |
| Thermal resistance, junction-to-board 3/ 6/ | $\theta_{JB}$ | 20.7 | --- | --- | °C/W |
| Characterization parameter, junction-to-top 3/ 4/ | $\psi_{JT}$ | 0.3 | 0.5 | 0.8 | °C/W |

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
3/ Per JEDEC JESD51-7 plus JEDEC JESD 51-5 test board.
4/ Per JEDEC JESD51-2 (still air) or JEDEC JESD 51-6 (moving air).
5/ Per MIL-STD-883, method 1021, thermal characteristics.
6/ Per JEDEC JESD 51-8 (still air).

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices
EIA/JEDEC 51-5 - Extension of Thermal Conductivity Test Board Standards for Packages with Direct Thermal Attachment Mechanisms
EIA/JEDEC 51-6 - Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)
EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JEDEC 51-8 - Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 CMOS output data timing waveforms. The CMOS output data timing waveforms shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| DC specifications. | | | | | | | |
| Resolution | | | -55°C to +125°C | 01 | 16 | | Bits |
| Accuracy. | | | | | | | |
| No missing codes | | | -55°C to +125°C | 01 | Guaranteed | | |
| Offset error | | | -55°C to +125°C | 01 | | ±0.30 | %FSR |
| Gain error 3/ | | | +25°C | 01 | -1.3 typical | | %FSR |
| Differential 4/ nonlinearity error | DNL | | +25°C | 01 | -0.5/+1.0 typical | | LSB |
| | | | -55°C to +125°C | | | -0.9/ +1.7 | |
| Integral nonlinearity 4/ error | INL | | +25°C | 01 | ±2.6 typical | | LSB |
| | | | -55°C to +125°C | | | ±6.5 | |
| Offset error temperature drift | | | -55°C to +125°C | 01 | ±2 typical | | ppm/ °C |
| Internal voltage reference. | | | | | | | |
| Output voltage | | 1 V mode | -55°C to +125°C | 01 | 0.983 | 1.007 | V |
| Load regulation error at 1.0 mA | | | +25°C | 01 | 2 typical | | mV |
| Input referred noise | | | | | | | |
| Input referred noise | | VREF = 1.0 V | +25°C | 01 | 2.8 typical | | LSB rms |
| Analog input. | | | | | | | |
| Input span, VREF = 1.0 V | | | +25°C | 01 | 2 typical | | VPP |
| Input capacitance 5/ | $C_{IN}$ | | +25°C | 01 | 6.5 typical | | pF |
| Input common mode voltage | | | +25°C | 01 | 0.9 typical | | V |
| Input common mode range | | | -55°C to +125°C | 01 | 0.5 | 1.3 | V |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Reference input resistance | | | -55°C to +125°C | 01 | 7.5 typical | | kΩ |
| Power supplies. | | | | | | | |
| Supply voltage for ADC core domain | $AV_{DD}$ | | -55°C to +125°C | 01 | 1.7 | 1.9 | V |
| Supply voltage for output driver domain | $DRV_{DD}$ | | -55°C to +125°C | 01 | 1.7 | 3.6 | V |
| Supply current for 4/ ADC core domain | $IAV_{DD}$ | | -55°C to +125°C | 01 | | 62.2 | mA |
| Supply current for 4/ for output driver domain | $IDRV_{DD}$ | At 1.8 V | +25°C | 01 | 5.2 typical | | mA |
| Supply current for 4/ for output driver domain | $IDRV_{DD}$ | At 3.3 V | +25°C | 01 | 9.3 typical | | mA |
| Power consumption. | | | | | | | |
| DC input | | | +25°C | 01 | 107 typical | | mW |
| Sine wave input 4/ | | $DRV_{DD}$ = 1.8 V | -55°C to +125°C | 01 | | 122 | mW |
| | | $DRV_{DD}$ = 3.3 V | +25°C | | 132 typical | | |
| Standby power 6/ | | | +25°C | 01 | 44 typical | | mW |
| Power down power. | | | +25°C | 01 | 0.5 typical | | mW |
| AC specification | | | | | | | |
| Signal to noise ratio | SNR | $f_{IN}$ = 9.7 MHz | +25°C | 01 | 77.6 typical | | dBFS |
| | | $f_{IN}$ = 30.5 MHz | +25°C | | 77.4 typical | | |
| | | | -55°C to +125°C | | 76.5 | | |
| | | $f_{IN}$ = 70 MHz | +25°C | | 76.4 typical | | |
| Signal to noise and distortion | SINAD | $f_{IN}$ = 9.7 MHz | +25°C | 01 | 77.4 typical | | dBFS |
| | | $f_{IN}$ = 30.5 MHz | +25°C | | 77.2 typical | | |
| | | | -55°C to +125°C | | 76.0 | | |
| | | $f_{IN}$ = 70 MHz | +25°C | | 76.3 typical | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| AC specification – continued. | | | | | | | |
| Effective number of bits | ENOB | $f_{IN}$ = 9.7 MHz | +25°C | 01 | 12.6 typical | | Bits |
| | | $f_{IN}$ = 30.5 MHz | +25°C | | 12.5 typical | | |
| | | | -55°C to +125°C | | 12.3 | | |
| | | $f_{IN}$ = 70 MHz | +25°C | | 12.4 typical | | |
| Worst second or third harmonic | | $f_{IN}$ = 9.7 MHz | +25°C | 01 | -94 typical | | dBc |
| | | $f_{IN}$ = 30.5 MHz | +25°C | | -93 typical | | |
| | | | -55°C to +125°C | | | -80 | |
| | | $f_{IN}$ = 70 MHz | +25°C | | -93 typical | | |
| Spurious free dynamic range | SFDR | $f_{IN}$ = 9.7 MHz | +25°C | 01 | 94 typical | | dBc |
| | | $f_{IN}$ = 30.5 MHz | +25°C | | 93 typical | | |
| | | | -55°C to +125°C | | 80 | | |
| | | $f_{IN}$ = 70 MHz | +25°C | | 93 typical | | |
| Worst other (harmonic or spur) | | $f_{IN}$ = 9.7 MHz | +25°C | 01 | -92 typical | | dBFS |
| | | $f_{IN}$ = 30.5 MHz | +25°C | | -101 typical | | |
| | | | -55°C to +125°C | | | -88 | |
| | | $f_{IN}$ = 70 MHz | +25°C | | -98 typical | | |
| Two tone SFDR | | $f_{IN}$ = 30.5 MHz (-7 dBFS) | +25°C | 01 | 90 typical | | dBc |
| | | $f_{IN}$ = 32.5 MHz (-7 dBFS) | | | 90 typical | | |
| Analog input bandwidth | | | +25°C | 01 | 700 typical | | MHz |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Digital specifications. | | | | | | | |
| Differential clock inputs (+CLK, -CLK) | | | | | | | |
| Logic compliance | | CMOS / LVDS / LVPECL | | | | | |
| Internal common mode bias | | | -55°C to +125°C | 01 | 0.9 typical | | V |
| Differential input voltage | | | -55°C to +125°C | 01 | 0.2 | 3.6 | $V_{PP}$ |
| Input voltage range | | | -55°C to +125°C | 01 | GND – 0.3 | $AV_{DD}$ + 0.2 | V |
| High level input current | $I_{IL}$ | | -55°C to +125°C | 01 | -10 | +10 | μA |
| Low level input current | $I_{IH}$ | | -55°C to +125°C | 01 | -10 | +10 | μA |
| Input resistance | $R_{IN}$ | | -55°C to +125°C | 01 | 8 | 12 | kΩ |
| Input capacitance | $C_{IN}$ | | +25°C | 01 | 4 typical | | pF |
| Logic inputs (SCLK/DFS, MODE, SDIO/PDWN). 7/ | | | | | | | |
| High level input voltage | $V_{IH}$ | | -55°C to +125°C | 01 | 1.2 | $DRV_{DD}$ + 0.3 | V |
| Low level input voltage | $V_{IL}$ | | -55°C to +125°C | 01 | 0 | 0.8 | V |
| High level input current | $I_{IH}$ | | -55°C to +125°C | 01 | -50 | -75 | μA |
| Low level input current | $I_{IL}$ | | -55°C to +125°C | 01 | -10 | +10 | μA |
| Input resistance | $R_{IN}$ | | -55°C to +125°C | 01 | 30 typical | | kΩ |
| Input capacitance | $C_{IN}$ | | -55°C to +125°C | 01 | 2 typical | | pF |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Digital specifications – continued. | | | | | | | |
| Logic inputs (CSB) 8/ | | | | | | | |
| High level input voltage | $V_{IH}$ | | -55°C to +125°C | 01 | 1.2 | $DRV_{DD}$ + 0.3 | V |
| Low level input voltage | $V_{IL}$ | | -55°C to +125°C | 01 | 0 | 0.8 | V |
| High level input current | $I_{IH}$ | | -55°C to +125°C | 01 | -10 | +10 | µA |
| Low level input current | $I_{IL}$ | | -55°C to +125°C | 01 | 40 | 135 | µA |
| Input resistance | $R_{IN}$ | | -55°C to +125°C | 01 | 26 typical | | kΩ |
| Input capacitance | $C_{IN}$ | | -55°C to +125°C | 01 | 2 typical | | pF |
| Digital outputs | | | | | | | |
| High level output voltage | $V_{OH}$ | $DRV_{DD}$ = 3.3 V, $I_{OH}$ = 50 µA | -55°C to +125°C | 01 | 3.29 | | V |
| | | $DRV_{DD}$ = 3.3 V, $I_{OH}$ = 0.5 mA | | | 3.25 | | |
| Low level output voltage | $V_{OL}$ | $DRV_{DD}$ = 3.3 V, $I_{OL}$ = 1.6 mA | -55°C to +125°C | 01 | | 0.2 | V |
| | | $DRV_{DD}$ = 3.3 V, $I_{OL}$ = 50 µA | | | | 0.05 | |
| High level output voltage | $V_{OH}$ | $DRV_{DD}$ = 1.8 V, $I_{OH}$ = 50 µA | -55°C to +125°C | 01 | 1.79 | | V |
| | | $DRV_{DD}$ = 1.8 V, $I_{OH}$ = 0.5 mA | | | 1.75 | | |
| Low level output voltage | $V_{OL}$ | $DRV_{DD}$ = 1.8 V, $I_{OL}$ = 1.6 mA | -55°C to +125°C | 01 | | 0.2 | V |
| | | $DRV_{DD}$ = 1.8 V, $I_{OL}$ = 50 µA | | | | 0.05 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Switching specifications. | | | | | | | |
| Clock input parameters. | | | | | | | |
| Input clock rate | | | -55°C to +125°C | 01 | | 520 | MHz |
| Conversion rate 9/ | | | -55°C to +125°C | 01 | 3 | 65 | MSPS |
| CLK period divide by 1 mode | $t_{CLK}$ | | -55°C to +125°C | 01 | 15.38 | | ns |
| CLK pulse width high | $t_{CH}$ | | +25°C | 01 | 7.69 typical | | ns |
| Aperture delay | $t_A$ | | -55°C to +125°C | 01 | 1.0 typical | | ns |
| Aperture uncertainty jitter | $t_J$ | | -55°C to +125°C | 01 | 0.1 typical | | ps rms |
| Data output parameters | | | | | | | |
| Data propagation delay | $t_{PD}$ | | -55°C to +125°C | 01 | 3 typical | | ns |
| DCO propagation delay | $t_{DCO}$ | | -55°C to +125°C | 01 | 3 typical | | ns |
| DCO to data skew | $t_{SKEW}$ | | -55°C to +125°C | 01 | 0.1 typical | | ns |
| Pipeline delay | Latency | | -55°C to +125°C | 01 | 9 typical | | Cycles |
| Wake up time 10/ | | | -55°C to +125°C | 01 | 350 typical | | μs |
| Standby | | | -55°C to +125°C | 01 | 300 typical | | ns |
| Out of range recovery time | | | -55°C to +125°C | 01 | 2 typical | | Cycles |
| Timing specifications. | | | | | | | |
| SPI timing requirements. | | | | | | | |
| Setup time between the data and the rising edge of SCLK | $t_{DS}$ | | -55°C to +125°C | 01 | 2 | | ns |
| Hold time between the data and the rising edge of SCLK | $t_{DH}$ | | -55°C to +125°C | 01 | 2 | | ns |
| Period of the SCLK | $t_{CLK}$ | | -55°C to +125°C | 01 | 40 | | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions 2/ | Temperature, $T_A$ | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Timing specifications - continued. | | | | | | | |
| SPI timing requirements - continued. | | | | | | | |
| Setup time between CSB and SCLK | $t_S$ | | -55°C to +125°C | 01 | 2 | | ns |
| Hold time between CSB and SCLK | $t_H$ | | -55°C to +125°C | 01 | 2 | | ns |
| SCLK pulse width high | $t_{HIGH}$ | | -55°C to +125°C | 01 | 10 | | ns |
| SCLK pulse width low | $t_{LOW}$ | | -55°C to +125°C | 01 | 10 | | ns |
| Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge | $t_{EN\_SDIO}$ | | -55°C to +125°C | 01 | 10 | | ns |
| Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge | $t_{DIS\_SDIO}$ | | -55°C to +125°C | 01 | 10 | | ns |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, $AV_{DD}$ = 1.8 V, $DRV_{DD}$ = 1.8 V, maximum sample rate, 2 $V_{PP}$ differential input, 1.0 V internal reference, AIN = -1.0 dBFS, 50 % duty cycle clock, and DCS disabled.

3/ Measured with 1.0 V external reference.

4/ Measured with a 10 MHz input frequency at rated sample rate, full scale sine wave, with approximately 5 pF loading on each output bit.

5/ Input capacitance refers to the effective capacitance between the differential inputs.

6/ Standby power is measured with a dc input and the CLK active.

7/ Internal 30 kΩ pull down.

8/ Internal 30 kΩ pull up.

9/ Conversion rate is the clock rate after the CLK divider.

10/ Wake up time is dependent on the value of the decoupling capacitors.

Case X

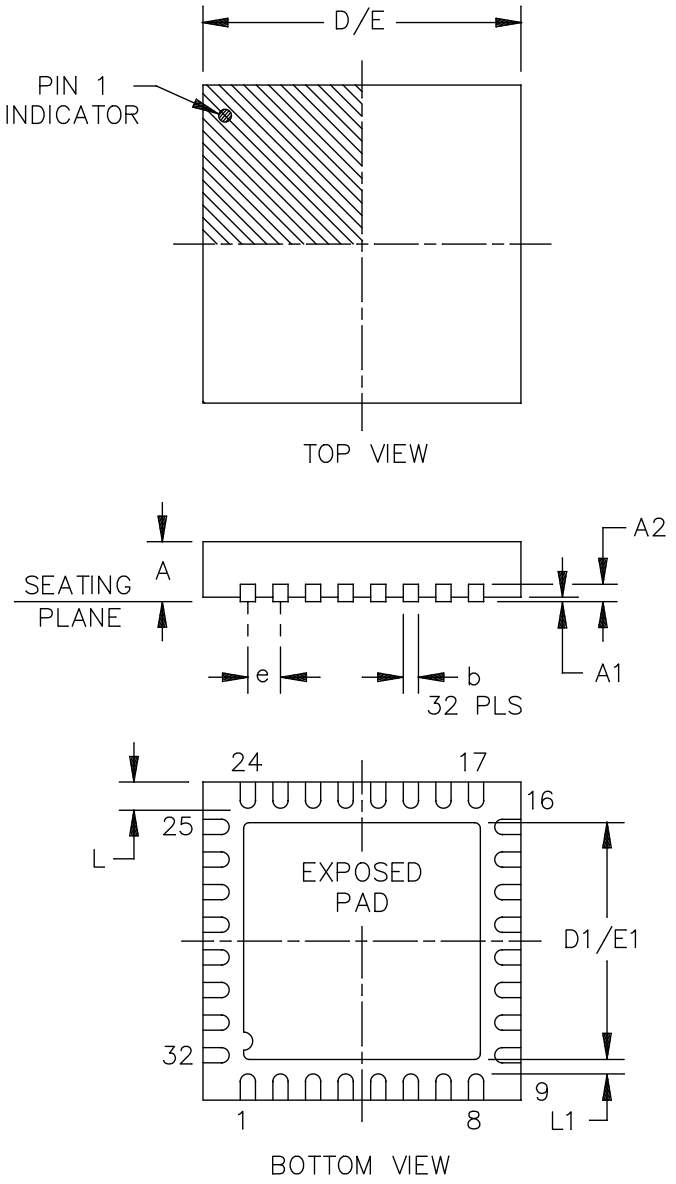


FIGURE 1. Case outline.

| DLA LAND AND MARITIME<br>COLUMBUS, OHIO | SIZE<br>A | CODE IDENT NO.<br>16236 | DWG NO.<br>V62/12660 |
|---|---|---|---|
| | | REV | PAGE 12 |

Case X

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | .027 | .031 | 0.70 | 0.80 |
| A1 | .0007 | .001 | 0.02 | 0.05 |
| A2 | .007 REF | | 0.20 REF | |
| b | .007 | .011 | 0.18 | 0.30 |
| D/E | .192 | .200 | 4.90 | 5.10 |
| D1/E1 | .139 | .147 | 3.55 | 3.75 |
| L | .011 | .019 | 0.30 | 0.50 |
| L1 | .009 | --- | 0.25 | --- |

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WHHD-5.

FIGURE 1. Case outline - Continued.

| Device type | 01 | | |
|---|---|---|---|
| Case outline | X | | |
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | +CLK | 17 | D7_D6 |
| 2 | -CLK | 18 | D9_D8 |
| 3 | $AV_{DD}$ | 19 | D11_D10 |
| 4 | CSB | 20 | D13_D12 |
| 5 | SCLK/DFS | 21 | (MSB) D15_D14 |
| 6 | SDIO/PDWN | 22 | DCO |
| 7 | NC | 23 | MODE/OR |
| 8 | NC | 24 | $AV_{DD}$ |
| 9 | NC | 25 | $V_{REF}$ |
| 10 | NC | 26 | SENSE |
| 11 | NC | 27 | $V_{CM}$ |
| 12 | NC | 28 | RBIAS |
| 13 | $DRV_{DD}$ | 29 | $AV_{DD}$ |
| 14 | D1_D0 (LSB) | 30 | $-V_{IN}$ |
| 15 | D3_D2 | 31 | $+V_{IN}$ |
| 16 | D5_D4 | 32 | $AV_{DD}$ |

NOTES:
1. NC = no connect. Do not connect to this pin.
2. The exposed paddle (pin 0) is the only GND connection on the chip and must be connected to the PCB AGND.

FIGURE 2. Terminal connections.

| Terminal symbol | Description |
|---|---|
| Exposed pad | AGND. The exposed paddle is the only ground connection on the chip. It must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits. |
| +CLK, -CLK | Differential encode clock for PECL, LVDS, or 1.8 V CMOS inputs. |
| $AV_{DD}$ | 1.8 V supply pin for ADC core domain. |
| CSB | SPI chip select. Active low enable, 30 kΩ internal pull up. |
| SCLK/DFS | SPI clock input in SPI mode (SCLK). 30 kΩ internal pull down.<br>Data format select in non-SPI mode (DFS).<br>Static control of data output format. 30 kΩ internal pull down.<br>DFS high = twos complement output; DFS low = offset binary output. |
| SDIO/PDWN | SPI data input/output (SDIO). Bidirectional SPI data I/O with 30 kΩ internal pull down.<br>Non-SPI mode power down (PDWN).<br>Static control chip power down with 30 kΩ internal pull down. |
| NC | No connect. Do not connect to this pin. |
| D1_D0 (LSB) to (MSB) D15_D14 | ADC digital outputs. |
| $DRV_{DD}$ | 1.8 V to 3.3 V supply pin for output driver domain. |
| DCO | Data clock digital output. |
| MODE/OR | Chip mode select input (MODE)/out of range digital output in SPI mode (OR).<br>Default = out of range (OR) digital output (SPI register 0x2A, bit 0 = 1).<br>Option = chip mode select input (SPI register 0x2A, bit 0 = 0).<br>Chip power down (SPI register 0x08, bits[7:5] = 100b).<br>Chip standby (SPI register 0x08, bits[7:5] = 101b).<br>Normal operation, output disabled (SPI register 0x08, bits[7:5] = 110b).<br>Normal operation, output enabled (SPI register 0x08, bits[7:5} = 111b).<br>Out of range (OR) digital output only in non-SPI mode. |
| $V_{REF}$ | 1.0 V voltage reference input/output. |
| SENSE | Reference mode selection. |
| $V_{CM}$ | Analog output voltage at mid AVDD supply. Sets common mode of the analog inputs. |
| RBIAS | Set analog current bias. Connect to 10 kΩ (1% tolerance) resistor to ground. |
| $-V_{IN}$, $+V_{IN}$ | ADC analog inputs. |

FIGURE 2. Terminal connections - continued.

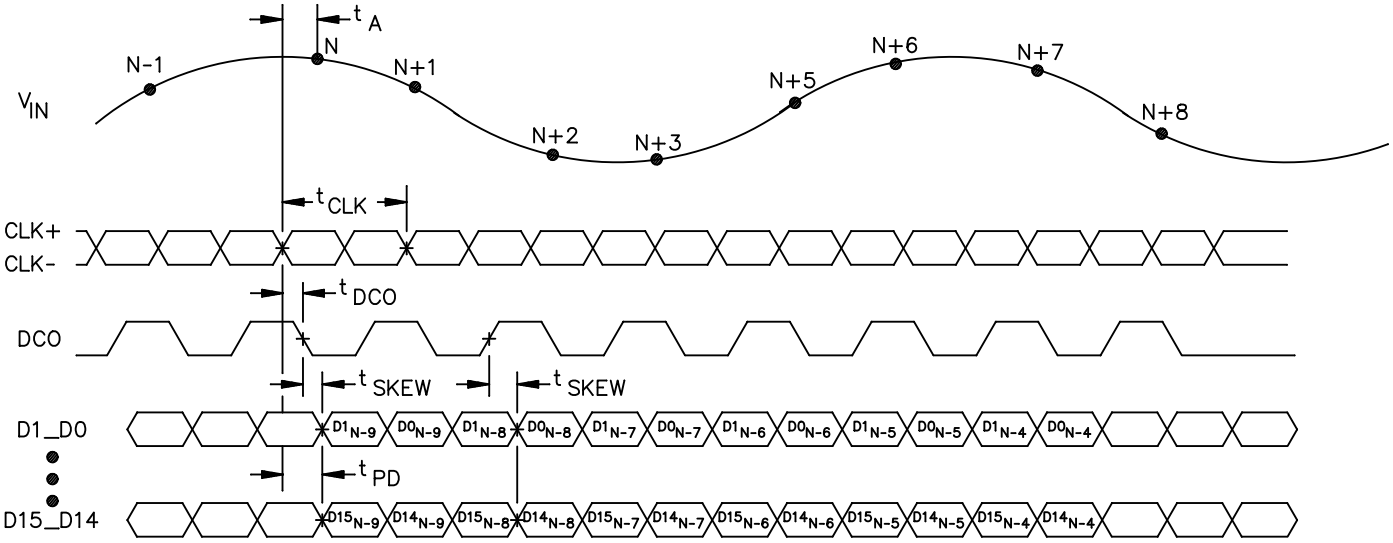


FIGURE 3. CMOS output data timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Vendor part number |
|---|---|---|
| V62/12660-01XE | 24355 | AD9266TCPZ-65-EP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 24355 | Analog Devices<br>Route 1 Industrial Park<br>P.O. Box 9106<br>Norwood, MA 02062<br>Point of contact: Raheen Business Park<br>Limerick, Ireland |