REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under paragraph 6.3, make correction to lead finish B vendor part number by deleting AD7524SRZ-EP-RL7 and replacing with AD7524SR-EP-RL7. Under paragraph 6.3, add lead finish E and vendor part numbers AD7524SRZ-EP and AD7524SRZ-EP-RL7. Add transportation mode data and quantity column under paragraph 6.3. - ro	18-02-14	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 13-06-17	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, DIGITAL-LINEAR, CMOS, 8-BIT, BUFFERED MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12659**
	REV **A**	**PAGE** 1 **OF** 15

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS, 8 bit, buffered multiplying digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12659	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7524	CMOS, 8 bit, buffered multiplying digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012-AC	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) to ground (GND) ..... -0.3 V to +17 V
DAC feedback resistor ($V_{RFEEDBACK}$) to GND ..... ±25 V
DAC reference voltage input (V_{REF}) to GND ..... ±25 V
Digital input voltage to GND ..... -0.3 V to V_{DD} + 0.3 V
DAC current output (OUT1), DAC analog ground (OUT2) to GND ..... -0.3 V to V_{DD} + 0.3 V
Power dissipation (PD) :
To 75°C ..... 450 mW
Derates above 75°C by ..... 6 mW/°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... 300°C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal resistance, junction to case (θ_{JC}) ..... 43°C/W (Non-standard 4 layer board)
Thermal resistance, junction to ambient (θ_{JA}) ..... 81°C/W (Non-standard 4 layer board)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{REF} = 10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance.							
Resolution		V_{DD} = 5 V and 15 V	25°C	01	8		Bits
			-55°C to +125°C		8		
Relative accuracy		V_{DD} = 5 V and 15 V	25°C	01		±1/2	LSB
			-55°C to +125°C			±1/2	
Monotonicity				01	Guaranteed		
Gain error 2/	AE	V_{DD} = 5 V	25°C	01		±2 1/2	LSB
		V_{DD} = 15 V				±1 1/4	
		V_{DD} = 5 V	-55°C to +125°C			±3 1/2	
		V_{DD} = 15 V				±1 1/2	
Average gain 3/ temperature coefficient (Measured from 25°C to -55°C or from 25°C to +125°C)		V_{DD} = 5 V	25°C	01	±40		ppm/°C
		V_{DD} = 15 V			±10		
		V_{DD} = 5 V	-55°C to +125°C		±40		
		V_{DD} = 15 V			±10		
DC supply rejection 3/	ΔGain/ ΔV_{DD}	V_{DD} = 5 V, ΔV_{DD} = ±10%	25°C	01		0.08	%FSR/ %max
					0.002 typical		
		V_{DD} = 15 V, ΔV_{DD} = ±10%				0.02	
					0.001 typical		
		V_{DD} = 5 V, ΔV_{DD} = ±10%	-55°C to +125°C			0.16	
					0.01 typical		
		V_{DD} = 15 V, ΔV_{DD} = ±10%				0.04	
					0.005 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{REF} = 10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise specified		Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Static performance – continued.								
Output leakage current, pin 1	I_{OUT1}	DB0 to DB7 = 0 V,	V_{DD} = 5 V	25°C	01		±50	nA
		$\overline{WR}$, $\overline{CS}$ = 0 V,	V_{DD} = 15 V				±50	
		V_{REF} = ±10 V	V_{DD} = 5 V	-55°C to +125°C			±400	
			V_{DD} = 15 V				±200	
Output leakage current, pin 2	I_{OUT2}	DB0 to DB7 = V_{DD},	V_{DD} = 5 V	25°C	01		±50	nA
		$\overline{WR}$, $\overline{CS}$ = 0 V,	V_{DD} = 15 V				±50	
		V_{REF} = ±10 V	V_{DD} = 5 V	-55°C to +125°C			±400	
			V_{DD} = 15 V				±200	
Dynamic performance.								
Output current 3/ settling time (to 1/2 LSB)		OUT1 load = 100 Ω,	V_{DD} = 5 V	25°C	01		400	ns
		C_{EXT} = 13 pF,	V_{DD} = 15 V				250	
		$\overline{WR}$, $\overline{CS}$ = 0 V,	V_{DD} = 5 V	-55°C to +125°C			500	
		DB0 to DB7 = 0 V to V_{DD} to 0 V,	V_{DD} = 15 V				350	
AC feedthrough at 3/ at OUT1		V_{REF} = ±10 V,	V_{DD} = 5 V	25°C	01		0.25	%FSR
		100 kHz sine wave,	V_{DD} = 15 V				0.25	
		DB0 to DB7 = 0 V,	V_{DD} = 5 V	-55°C to +125°C			0.5	
		$\overline{WR}$, $\overline{CS}$ = 0 V,	V_{DD} = 15 V				0.5	
AC feedthrough at 3/ at OUT2		V_{REF} = ±10 V,	V_{DD} = 5 V	25°C	01		0.25	%FSR
		100 kHz sine wave,	V_{DD} = 15 V				0.25	
		DB0 to DB7 = 0 V,	V_{DD} = 5 V	-55°C to +125°C			0.5	
		$\overline{WR}$, $\overline{CS}$ = 0 V,	V_{DD} = 15 V				0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{REF} = 10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Reference input.							
Reference input 4/ (V_{REF} pin to GND)	R_{IN}	V_{DD} = 5 V and 15 V	25°C	01	5	20	kΩ
			-55°C to +125°C		5	20	
Analog outputs.							
Output capacitance 3/	COUT1 (pin 1)	V_{DD} = 5 V and 15 V, DB0 to DB7 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0 V,	25°C	01		120	pF
			-55°C to +125°C			120	
	COUT2 (pin 2)		25°C			30	
			-55°C to +125°C			30	
	COUT1 (pin 1)	V_{DD} = 5 V and 15 V, DB0 to DB7 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0 V,	25°C			30	
			-55°C to +125°C			30	
	COUT2 (pin 2)		25°C			120	
			-55°C to +125°C			120	
Digital inputs.							
Input high voltage requirement	V_{IH}	V_{DD} = 5 V	25°C	01	2.4		V
		V_{DD} = 15 V			13.5		
		V_{DD} = 5 V	-55°C to +125°C		2.4		
		V_{DD} = 15 V			13.5		
Input low voltage requirement	V_{IL}	V_{DD} = 5 V	25°C	01		0.8	V
		V_{DD} = 15 V				1.5	
		V_{DD} = 5 V	-55°C to +125°C			0.5	
		V_{DD} = 15 V				1.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{REF} = 10 V, $V_{OUT1} = V_{OUT2}$ = 0 V, unless otherwise specified		Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Digital inputs - continued.								
Input current	I_{IN}	V_{DD} = 5 V, V_{IN} = 0 V or V_{DD}		25°C	01		±1	µA
		V_{DD} = 15 V, V_{IN} = 0 V or V_{DD}					±1	
		V_{DD} = 5 V, V_{IN} = 0 V or V_{DD}		-55°C to +125°C			±10	
		V_{DD} = 15 V, V_{IN} = 0 V or V_{DD}					±10	
Input capacitance 3/	C_{IN}	V_{DD} = 5 V and 15 V, V_{IN} = 0 V, DB0 to DB7		25°C	01		5	pF
				-55°C to +125°C			5	
		V_{DD} = 5 V and 15 V, V_{IN} = 0 V, $\overline{WR}$, $\overline{CS}$		25°C			20	
				-55°C to +125°C			20	
Switching characteristics.		See figure 3.						
Chip select to write setup time 5/	t_{CS}	$t_{WR} = t_{CS}$	V_{DD} = 5 V	25°C	01	170		ns
			V_{DD} = 15 V			100		
			V_{DD} = 5 V	-55°C to +125°C		240		
			V_{DD} = 15 V			150		
Chip select to write hold time	t_{CH}	V_{DD} = 5 V and 15 V		25°C	01	0		ns
				-55°C to +125°C		0		
Write pulse width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	V_{DD} = 5 V	25°C	01	170		ns
			V_{DD} = 15 V			100		
			V_{DD} = 5 V	-55°C to +125°C		240		
			V_{DD} = 15 V			150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{REF} = 10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise specified		Temperature, T_A	Device type	Limits		Unit
						Min	Max	
Switching characteristics - continued. See figure 3								
Data setup time	t_{DS}	V_{DD} = 5 V		25°C	01	135		ns
		V_{DD} = 15 V				60		
		V_{DD} = 5 V		-55°C to +125°C		170		
		V_{DD} = 15 V				100		
Data hold time	t_{DH}	V_{DD} = 5 V and 15 V		25°C	01	10		ns
				-55°C to +125°C		10		
Power supply								
Power supply current	I_{DD}	All digital inputs V_{IL} or V_{IH}	V_{DD} = 5 V	25°C	01		1	mA
			V_{DD} = 15 V				2	
			V_{DD} = 5 V	-55°C to +125°C			2	
			V_{DD} = 15 V				2	
		All digital inputs 0 V or V_{DD}	V_{DD} = 5 V	25°C			100	µA
			V_{DD} = 15 V				100	
			V_{DD} = 5 V	-55°C to +125°C			500	
			V_{DD} = 15 V				500	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Gain error is measured using internal feedback resistor. Full scale range (FSR) = V_{REF}.

3/ Guaranteed not tested.

4/ DAC thin film resistor temperature coefficient is approximately – 300 ppm/°C.

5/ AC parameter, sample tested at 25°C to ensure conformance to specification.

Case X

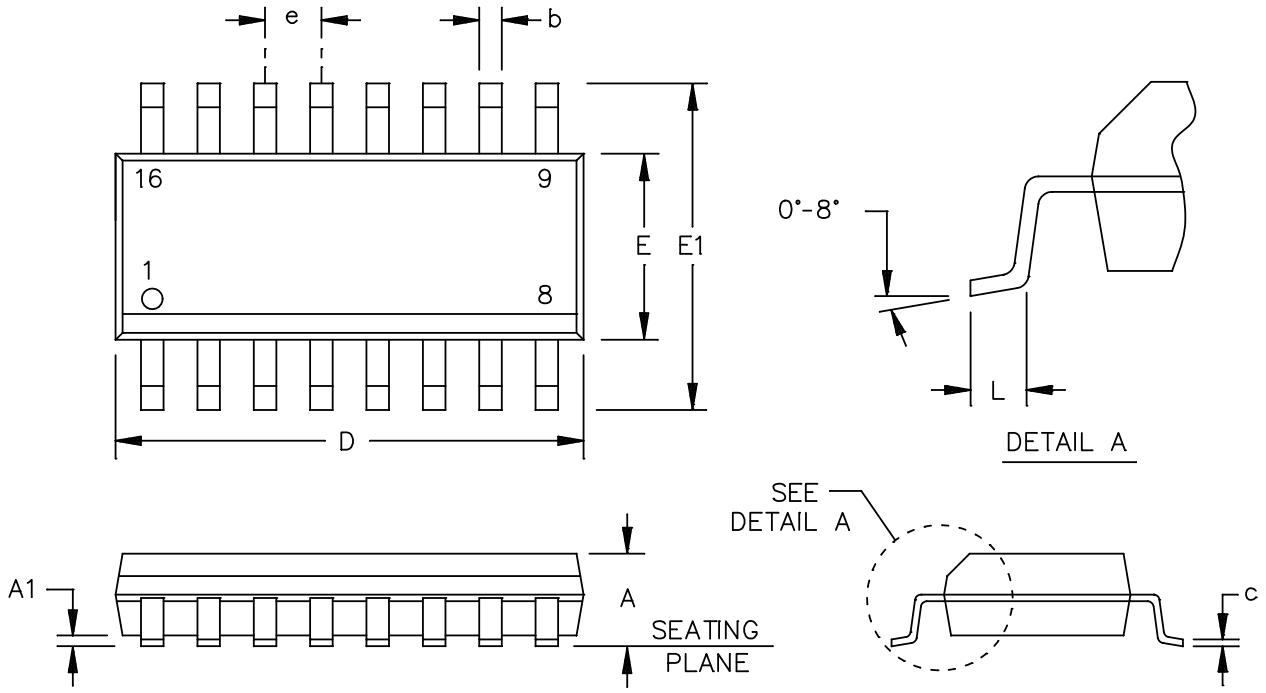


FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12659
		REV A	PAGE 10

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0531	0.0689	1.35	1.75
A1	0.0039	0.0098	0.10	0.25
b	0.0122	0.0201	0.31	0.51
c	0.0067	0.0098	0.17	0.25
D	0.3858	0.3937	9.80	10.00
E	0.1496	0.1575	3.80	4.00
E1	0.2283	0.2441	5.80	6.20
e	0.0500 BSC		1.27 BSC	
L	0.0157	0.0500	0.40	1.27

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AC.

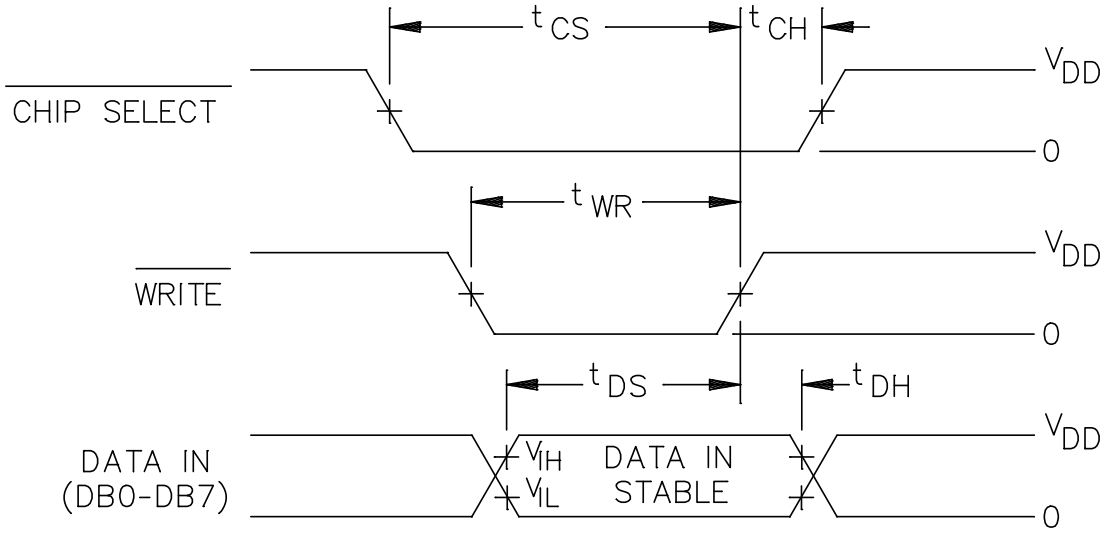
FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT1
2	OUT2
3	GND
4	DB7 (MSB)
5	DB6
6	DB5
7	DB4
8	DB3
9	DB2
10	DB1
11	DB0 (LSB)
12	$\overline{CS}$
13	$\overline{WR}$
14	V_{DD}
15	V_{REF}
16	$R_{FEEDBACK}$

FIGURE 2. Terminal connections.

Terminal symbol	Description
OUT1	DAC current output.
OUT2	DAC analog ground. This pin should normally be tied to the analog ground of the system.
GND	Ground.
DB7 (MSB) to DB0 (LSB)	Parallel data bit 7 to data bit 0.
$\overline{CS}$	Chip select input. Active low. Used in conjunction with $\overline{WR}$ to load parallel data to the input latch.
$\overline{WR}$	Write. When low, use in conjunction with $\overline{CS}$ to load parallel data.
V_{DD}	Positive power supply input. These parts can be operated with a supply of 5 V.
V_{REF}	DAC reference voltage input terminal.
$R_{FEEDBACK}$	DAC feedback resistor pin. Establish voltage output of the DAC by connecting to external amplifier output.

FIGURE 2. Terminal connections - continued.



NOTES:

1. All input signal rise and fall times measured from 10% to 90% of V_{DD}.
   V_{DD} = 5 V, $t_R = t_F$ = 20 ns; V_{DD} = 15 V, $t_R = t_F$ = 40 ns.

2. Timing measurement reference level is $(V_{IH} + V_{IL}) / 2$.

3. $t_{DS} + t_{DH}$ is approximately constant at 145 ns minimum at 25°C, V_{DD} = 5 V and t_{WR} = 170 ns minimum. The device is specified for a minimum t_{DH} of 10 ns. However, in applications where $t_{DH} > 10$ ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65 ns, t_{DH} = 80 ns.

FIGURE 3. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/12659-01XB	24355	Tube, 48 units	AD7524SR-EP
V62/12659-01XB	24355	Reel, 1000 units	AD7524SR-EP-RL7
V62/12659-01XE	24355	Tube, 48 units	AD7524SRZ-EP
V62/12659-01XE	24355	Reel, 1000 units	AD7524SRZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland