

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add mode of transportation and quantity column under paragraph 6.3. Update document paragraphs to current requirements. - ro	18-09-19	C. SAFFLE



Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A						
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PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="http://www.dla.mil/landandmaritime">http://www.dla.mil/landandmaritime</a>	
Original date of drawing YY-MM-DD  13-04-09	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL-LINEAR, QUAD UV/OV POSITIVE/NEGATIVE VOLTAGE SUPERVISOR, MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. <b>V62/12655</b>
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad under voltage (UV) / over voltage (OV) positive/negative voltage supervisor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/12655</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADM2914-EP	Quad UV/OV positive/negative voltage supervisor

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MO-137-AB	Shrink small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

VCC .....	-0.3 V to +6.0 V
$\overline{UV}$ , $\overline{OV}$ .....	-0.3 V to +16.0 V
Timer .....	-0.3 V to (VCC + 0.3 V)
VLx, VHx, $\overline{LATCH}$ , SEL .....	-0.3 V to +7.5 V
ICC .....	10 mA
Reference load current (IREF) .....	±1 mA
$I_{\overline{UV}}$ , $I_{\overline{OV}}$ .....	10 mA
Operating temperature range: .....	-55°C to +125°C
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 second) .....	+300°C

1.4 Thermal characteristics.

Thermal resistance

Case outline	$\theta_{JA}$	Unit
Case X	104	°C/W

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at <https://www.jedec.org>).

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 UV/OV Timeout period versus Capacitance. The UV/OV Timeout period versus Capacitance shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
<b>Shunt regulator</b>						
VCC shunt regulator voltage	VSHUNT	ICC = 5 mA	6.2	6.6	6.9	V
		TA = -55°C to +125°C	6.2	6.6	7.0	V
VCC shunt regulator load regulation	ΔVSHUNT	ICC = 2 mA to 10 mA		200	300	mV
<b>Supply</b>						
Supply voltage 3/	VCC		2.3		VSHUNT	V
Minimum VCC output valid	VCCR(MIN)				1	V
Supply under voltage lockout	VCC(UVLO)	VCC rising	1.9	2	2.1	V
Supply under voltage lockout hysteresis	ΔVCC(HYST)		5	25	50	mV
Supply current	ICC	VCC = 2.3 V to 6 V		62	100	μA
<b>Reference output</b>						
Reference output voltage	VREF	IVREF = ±1 mA	0.985	1	1.015	V
		TA = -55°C to +125°C	0.985	1	1.020	
<b>Undervoltage/Overvoltage characteristics</b>						
Undervoltage/Overvoltage threshold	VUOT		492.5	500	507.5	mV
Undervoltage/Overvoltage threshold to output delay	tUOD	VHx = VUOT – 5 mV or VLx = VUOT + 5 mV	50	125	500	μs
VHx, VLx input current	IVHL				±15	nA
		TA = -55°C to +125°C			±30	
UV/OV timeout period	tUOTO	CTIMER = 1 nF	6	8.5	12.5	ms
		TA = -55°C to +125°C	6	8.5	14	
<b>OV Latch clear input</b>						
OV Latch clear threshold input high	V <sub>LATCH(IH)</sub>		1.2			V
OV Latch clear threshold input low	V <sub>LATCH(IL)</sub>				0.8	V
LATCH input current	ILATCH	V <sub>LATCH</sub> > 0.5 V			±1	μA
<b>Timer characteristics</b>						
Timer pull up current	ITIMER(UP)	VTIMER = 0 V	-1.3	-2.1	-2.8	μA
		TA = -55°C to +125°C	-1.2	-2.1	-2.8	
Timer pull down current	ITIMER(DOWN)	VTIMER = 1.6 V	1.3	2.1	2.8	μA
		TA = -55°C to +125°C	1.2	2.1	2.8	
Timer disable voltage	VTIMER(DIS)	Reference to VCC	-180	-270		mV
<b>Output voltage</b>						
Output voltage high	UV/OV, VOH	VCC = 2.3 V; I <sub>UV/OV</sub> = -1 μA	1			V
Output voltage low	UV/OV, VOL	VCC = 2.3 V; I <sub>UV/OV</sub> = -2.5 mA		0.1	0.3	V
		VCC = 1 V; I <sub>UV</sub> = -100 μA		0.01	0.15	
		TA = -55°C to +125°C	0.6	0.9	1.2	

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions <u>2/</u>	Limits			Unit
			Min	Typ	Max	
Three state input SEL						
Low level input voltage	V <sub>IL</sub>				0.4	V
High level input voltage	V <sub>IH</sub>		1.4			V
Pin voltage when left in high-Z state	V <sub>Z</sub>	I <sub>SEL</sub> = ±10 µA	0.7	0.9	1.1	V
		TA = -55°C to +125°C	0.6	0.9	1.2	
SEL high, low input current	I <sub>SEL</sub>				±25	µA
Maximum SEL input current	I <sub>SEL(MAX)</sub>	SEL tied to VCC or GND			±30	µA

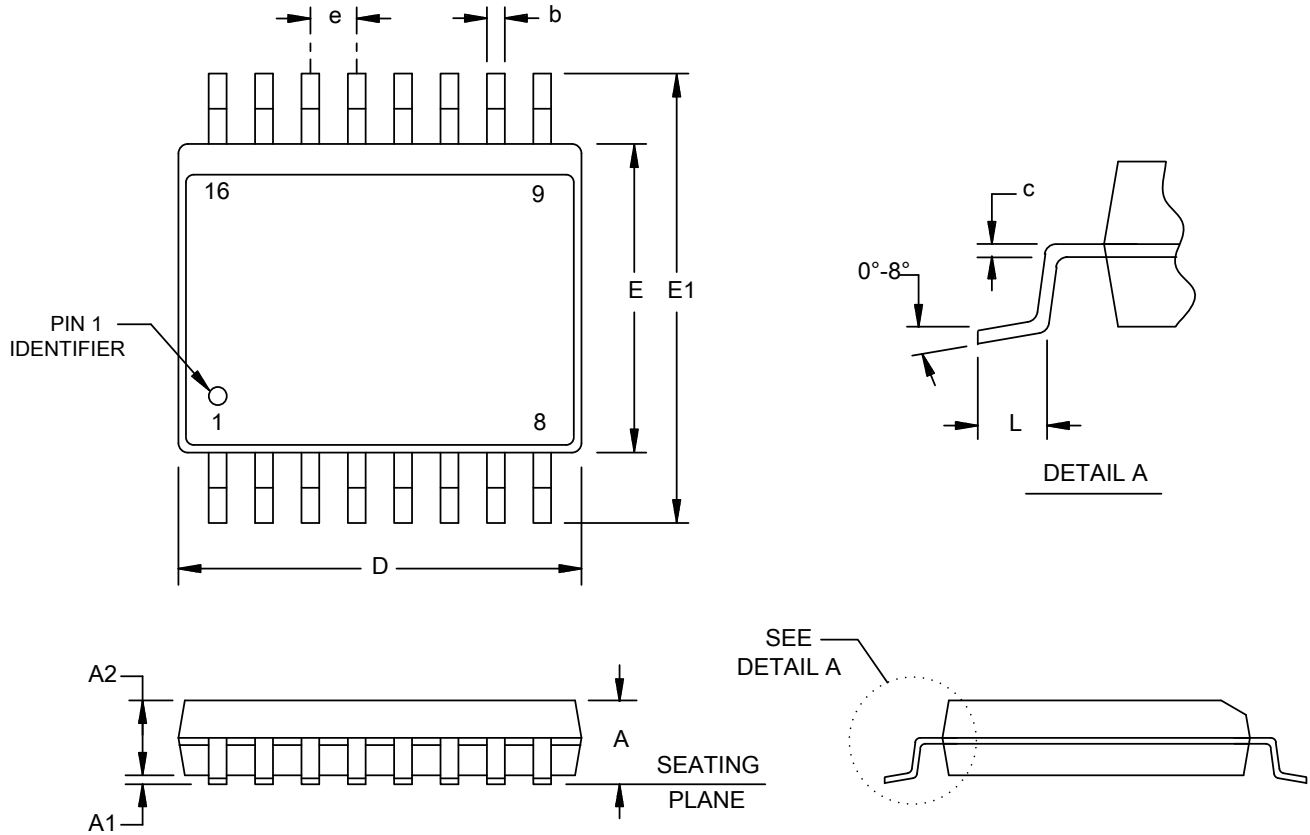
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ -55°C ≤ TA ≤ +125°C. Typical values at TA = 25°C, unless otherwise noted. VCC = 3.3 V, VLX = 0.45 V, VHx = 0.55 V, LATCH = VCC, SEL = VCC, unless otherwise noted.

3/ The maximum voltage on the VCC pin is limited by the input current. The VCC pin has an internal 6.5 V shunt regulator and, therefore, a low impedance supply greater than 6 V may exceed the maximum allowed input current. When operating from a higher supply than 6 V, always use a dropper resistor.

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Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.053	.069	1.35	1.75	D	.189	.197	4.80	5.00
A1	.049	.065	1.25	1.65	E	.150	.158	3.81	4.01
A2	.004	.010	0.10	0.25	E1	.228	.244	5.79	6.20
b	.008	.012	0.20	0.30	e	.025 BSC		0.64 BSC	
c	.006	.010	0.15	0.25	L	.041 REF		1.04 REF	

NOTES:

- Controlling dimensions are in inches; millimeters dimensions are rounded off inch; equivalents for reference only and are not appropriate for use in design..
- Falls within JEDEC MO-137-AB.

FIGURE 1. Case outline.

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Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VH1	16	V <sub>CC</sub>
2	VL1	15	TIMER
3	VH2	14	SEL
4	VL2	13	$\overline{\text{LATCH}}$
5	VH3	12	$\overline{\text{UV}}$
6	VL3	11	$\overline{\text{OV}}$
7	VH4	10	REF
8	VL4	9	GND

FIGURE 2. Terminal connections.

Case outline X		
Terminal number	Terminal symbol	Description
1	VH1	Voltage High Input 1 and Voltage High Input 2. If the voltage monitored by VH1 or VH2 drops below 0.5 V, an undervoltage condition is detected. Connect to V <sub>CC</sub> when not in use.
3	VH2	
2	VL1	Voltage Low Input 1 and Voltage Low Input 2. If the voltage monitored by VL1 or VL2 rises above 0.5 V, an overvoltage condition is detected. Tie to GND when not in use.
4	VL2	
5	VH3	Voltage High Input 3 and Voltage High Input 4. The polarity of these inputs is determined by the state of the SEL pin. When the monitored input is configured as a positive voltage and the voltage monitored by VH3 and VH4 drops below 0.5 V, an undervoltage condition is detected. Conversely, when the input is configured as a negative voltage and the inputs drops below 0.5 V, an overvoltage condition is detected. Connect to V <sub>CC</sub> when not in use.
7	VH4	
6	VL3	Voltage Low Input 3 and Voltage Low Input 4. The polarity of these inputs is determined by the state of the SEL pin. When the monitored input is configured as a positive voltage and the voltage monitored by VL3 and VL4 rises above 0.5 V, an overvoltage condition is detected. Conversely, when the input is configured as a negative voltage and the inputs rises above 0.5 V, an undervoltage condition is detected. Tie to GND when not in use.
8	VL4	
9	GND	Device Ground.
10	REF	Buffered Reference Output. This pin is a 1 V reference that is used as an offset when monitoring negative voltages. This pin can source or sink 1 mA and drive loads up to 1 nF. Larger capacitive loads may lead to instability. Leave unconnected when not in use.
11	$\overline{\text{OV}}$	Overvoltage Reset output. $\overline{\text{OV}}$ is asserted low if a negative polarity input voltage drops below its associated threshold or if a positive polarity input voltage exceeds its threshold. This device allows $\overline{\text{OV}}$ to be latched low. This pin has a weak pull up to V <sub>CC</sub> and can be pulled up to 16 V externally. Leave this pin unconnected when not in use.
12	$\overline{\text{UV}}$	Undervoltage Reset Output. $\overline{\text{UV}}$ is asserted low if a negative polarity input voltage exceeds its associated threshold or if a positive polarity input voltage drops below its threshold. $\overline{\text{UV}}$ is held low for an adjustable time out period set by the external capacitor tied to the TIMER pin. The $\overline{\text{UV}}$ pin has a weak pull up to V <sub>CC</sub> and can be pulled up to 16 V externally via an external pull up resistor. Leave this pin unconnected when not in use.

FIGURE 3. Terminal function.

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Case outline X – Continued.		
Terminal number	Terminal symbol	Description
13	$\overline{\text{LATCH}}$	$\overline{\text{OV}}$ Latch Bypass Input/Clear Pin. When pulled high, the $\overline{\text{OV}}$ latch is cleared. When held high, the $\overline{\text{OV}}$ output has the same delay and output characteristics as the $\overline{\text{UV}}$ output. When pulled low, the $\overline{\text{OV}}$ output is latched when asserted.
14	SEL	Input Polarity Select. This three state input pin allows the polarity of VH3, VL3, VH4 and VL4 to be configured. Connect to VCC or GND, or leave open to select one of three possible input polarity configurations.
15	TIMER	Adjustable Reset Delay Timer. Connect an external capacitor to the TIMER pin to program the reset timeout delay. Refer to FIGURE 5. Connect this pin to VCC to bypass the timer.
16	VCC	Supply Voltage. VCC operates as a direct supply for voltages up to 6 V. For voltages greater than 6 V, it operates as a shunt regulator. A dropper resistor must be used in this configuration to limit the current to less than 10 mA. When used without the resistor, the voltage at this pin must not exceed 6 V. A 0.1 $\mu\text{F}$ bypass capacitor or greater should be used.

FIGURE 3. Terminal function - Continued.

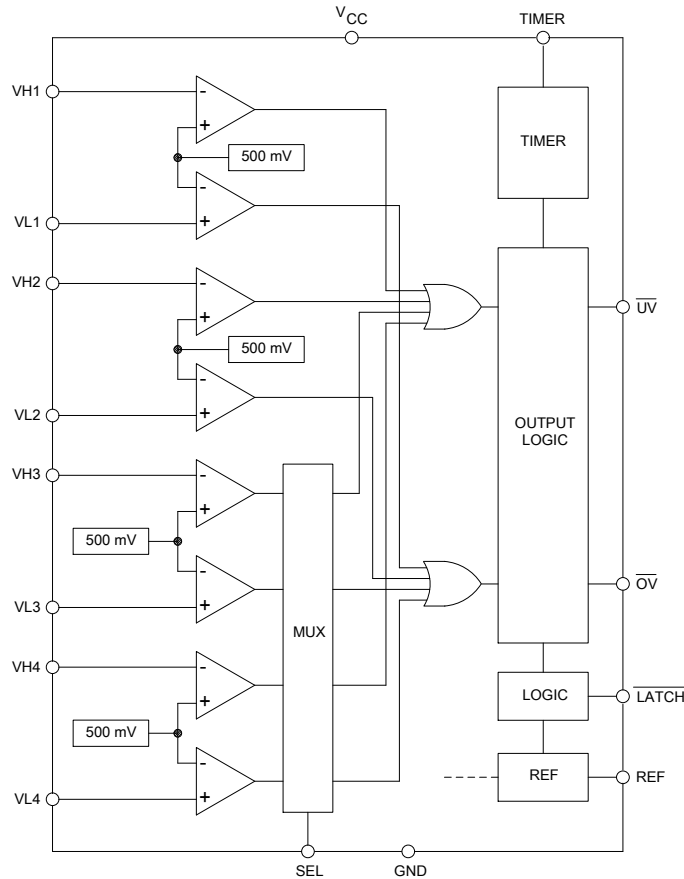


FIGURE 4. Functional block diagram

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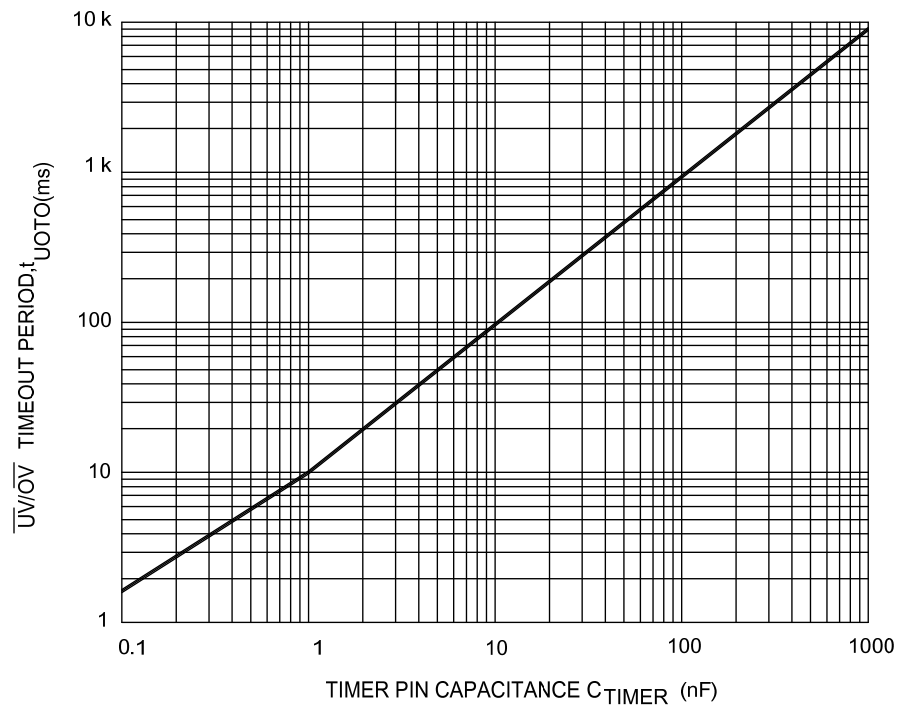


FIGURE 5.  $\overline{UV/OV}$  Timeout period vs Capacitance.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/12655-01XE	24355	Reel, 1,000 units	ADM2914-1SRQZEP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices  
 Route 1 Industrial Park  
 P.O. Box 9106  
 Norwood, MA 02062  
 Point of contact: Raheen Business Park  
 Limerick, Ireland

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