REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. - ro	18-06-12	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 13-01-11	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	TITLE MICROCIRCUIT, DIGITAL-LINEAR, DUAL, 16-BIT, 1130 MSPS, TxDAC+ DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12654**
	REV **A**	**PAGE** 1 **OF** 15

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AMSC N/A

5962-V057-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual, 16-bit, 1130 million samples per second (MSPS), TxDAC+ digital to analog converter microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12654	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9122-EP	Dual, 16-bit, 1130 MSPS, TxDAC+ digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	72	JEDEC MO-220-VNND-4	Lead Frame Chip Scale Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

AVDD33 to AVSS, EPAD, CVSS, DVSS ..... -0.3 V to +3.6 V
IOVDD to AVSS, EPAD, CVSS, DVSS ..... -0.3 V to +3.6 V
DVDD18, CVDD18 to AVSS, EPAD, CVSS, DVSS ..... -0.3 V to +2.1 V
AVSS to EPAD, CVSS, DVSS ..... -0.3 V to +0.3 V
EPAD to AVSS, CVSS, DVSS ..... -0.3 V to +0.3 V
CVSS to AVSS, EPAD, DVSS ..... -0.3 V to +0.3 V
DVSS to AVSS, EPAD, CVSS ..... -0.3 V to +0.3 V
FSADJ, REFIO, IOUT1P, IOUT1N, IOUT2P, IOUT2N to AVSS ..... -0.3 V to AVDD33 + 0.3 V
D[15:0]P, D[15:0]N, FRAMEP, FRAMEN, DCIP, DCIN to EPAD, DVSS ..... -0.3 V to DVDD18 + 0.3 V
DACCLKP, DACCLKN, REFCLKP, REFCLKN to CVSS ..... -0.3 V to CVDD18 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO to EPAD, DVSS ..... -0.3 V to IOVDD + 0.3 V
Junction temperature ..... 125°C
Storage temperature range ..... -65°C to +150°C

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JB}	θ_{JC}	Unit	Conditions
Case X	20.7	10.9	1.1	°C/W	EPAD soldered to ground plane

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1596 - IEEE Standard for low-voltage differential signals (LVDS) for scalable coherent.

(Copies of these documents are available online at https://www.ieee.org or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Timing diagram for input data port. The timing diagram for input data port shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
DC SPECIFICATIONS						
Resolution				16		Bits
Accuracy						
Differential Nonlinearity	DNL			±2.1		LSB
Integral Nonlinearity	INL			±3.7		LSB
Main DAC outputs						
Offset error			-0.001	0	+0.001	%FSR
Gain error (with internal reference)			-4.6	±2	+4.6	
Full scale output current 3/			8.66	19.6	31.66	mA
Output compliance range			-1.0		+1.0	V
Power Supply Rejection Ratio, AVD33			-0.3		+0.3	%FSR/V
output resistance				10		MΩ
Gain ADC monotonicity				4/		
Settling time to within ±0.5 LSB				20		ns
Main DAC temperature drift						
Offset				0.04		ppm/°C
Gain				100		
Reference voltage				30		
Reference						
Internal reference voltage				1.2		V
Output resistance				5		kΩ
Analog supply voltages						
AVD33			3.13	3.3	3.47	V
CVD18			1.71	1.8	1.89	
Digital supply voltages						
DVDD18			1.71	1.8	1.89	V
IOVDD			1.71	1.8/3.3	3.47	
Power consumption						
2 x Mode		f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL Off		834		mW
2 x Mode		f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL On		913		
8 x Mode		f_{DAC} = 800 MSPS, IF = 10 MHz, PLL Off		1135	1259	
AVDD33				55	57	mA
CVDD18				85	90	
DVDD18				444	505	
Power down mode (Register 0x01 = 0xF0)				6.5	18.8	mW
Power up time				260		ms
Operating range			-55	+25	+105	°C

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 5/	Limits			Unit
			Min	Typ	Max	
DIGITAL SPECIFICATIONS						
CMOS input logic level						
Input V_{IN} logic high		IOVDD = 1.8 V	1.2			V
		IOVDD = 2.5 V	1.6			
		IOVDD = 3.3 V	2.0			
Input V_{IN} logic low		IOVDD = 1.8 V			0.6	
		IOVDD = 2.5 V, 3.3 V			0.8	
CMOS output logic level						
Input V_{IN} logic high		IOVDD = 1.8 V	1.4			V
		IOVDD = 2.5 V	1.8			
		IOVDD = 3.3 V	2.4			
Input V_{IN} logic low		IOVDD = 1.8 V, 2.5 V, 3.3 V			0.4	
LVDS receiver inputs 6/ (Applies to data, DCI, and FRAME inputs)						
Input voltage range,	V_{IA} or V_{IB}		825		1675	mV
Input differential threshold	V_{IDTH}		-100		+100	
Input differential hysteresis,	V_{IDTHH} to V_{IDTHL}			20		
Receiver differential input impedance	R_{IN}		80		120	Ω
LVDS input rate		7/				
DAC clock input (DACCLKP, DACCLKN)						
Differential peak-to-peak voltage			100	500	2000	mV
Common mode voltage		Self-biased input, ac-coupled		1.25		V
Maximum clock rate			1230			MHz
REFCLK input (REFCLKP, REFCLKN)						
Differential peak-to-peak voltage			100	500	2000	mV
Common mode voltage				1.25		V
REFCLK frequency (PLL mode)		1 GHz ≤ f_{VCO} ≤ 2.1 GHz	15.625		600	MHz
REFCLK frequency (SYNC mode)		See Multichip synchronization section of the manufacturer data for more conditions	0		600	
Serial port interface						
Maximum clock rate	SCLK		40			MHz
Maximum pulse width high	t_{PWH}				12.5	ns
Minimum pulse width low	t_{PWL}				12.5	
Setup time, SDIO to SCLK	t_{DS}		2.1			
Hold time, SDIO to SCLK	t_{DH}		0.75			
Data valid, SDO to SCLK	t_{DV}		2.85			
Setup time, $\overline{CS}$ to SCLK	t_{DCSB}			1.4		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 5/	Limits			Unit
			Min	Typ	Max	
DIGITAL INPUT DATA TIMING SPECIFICATIONS						
Latency (DACCLK cycles)						
1 x Interpolation (With or without modulation)				64		Cycles
1 x Interpolation (With or without modulation)				135		
1 x Interpolation (With or without modulation)				292		
1 x Interpolation (With or without modulation)				608		
Inverse Sinc				20		
Fire modulation				8		

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
AC SPECIFICATIONS						
Spurious-Free Dynamic Range (SFDR)		f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		78		dBc
		f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		80		
		f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		69		
		f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		72		
Two tone Intermodulation Distortion (IMD)		f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		84		dBc
		f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		86		
		f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		84		
		f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		81		
Noise Spectral Density (NSD), Eight-tone, 500 kHz tone spacing		f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		-162		dBm/Hz
		f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		-163		
		f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		-164		
W-CDMA Adjacent Channel Leakage Ratio (ACLR), Single carrier		f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		84		dBc
		f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		82		
		f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		83		
W-CDMA second ACLR, single carrier		f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		88		dBc
		f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		86		
		f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		88		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.
3/ Based on a 10 kΩ external resistor between FSADJ and AVSS.
4/ Guaranteed.
5/ T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.
6/ LVDS receiver is compliant with the IEEE 1596 reduced range link, unless otherwise noted.
7/ Maximum rate (MSPS) with DVDD and CVDD supply regulation

Bus Width	Interpolation factor	$f_{INTERFACE}$ (MSPS) DVDD18, CVDD18 =			f_{DAC} (MSPS) DVDD18, CVDD18 =		
		1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%	1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%
Nibble (4 Bits)	1 x	1000	1100	1130	125	137.5	141.25
	2 x	1000	1100	1130	250	275	282.5
	4 x	1000	1100	1130	500	550	565
	8 x	1000	1100	1130	1000	1100	1130
Byte (8 Bits)	1 x	1000	1100	1130	250	275	282.5
	2 x	1000	1100	1130	500	550	565
	4 x	1000	1100	1130	1000	1100	1130
	8 x	500	550	565	1000	1100	1130
Word (16 Bits)	1 x	1000	1100	1130	500	550	565
	2 x (HB1)	800	900	900	800	900	900
	2 x (HB2)	1000	1100	1130	1000	1100	1130
	4 x	500	550	565	1000	1100	1130
	8 x	250	275	282.5	1000	1100	1130

Case X

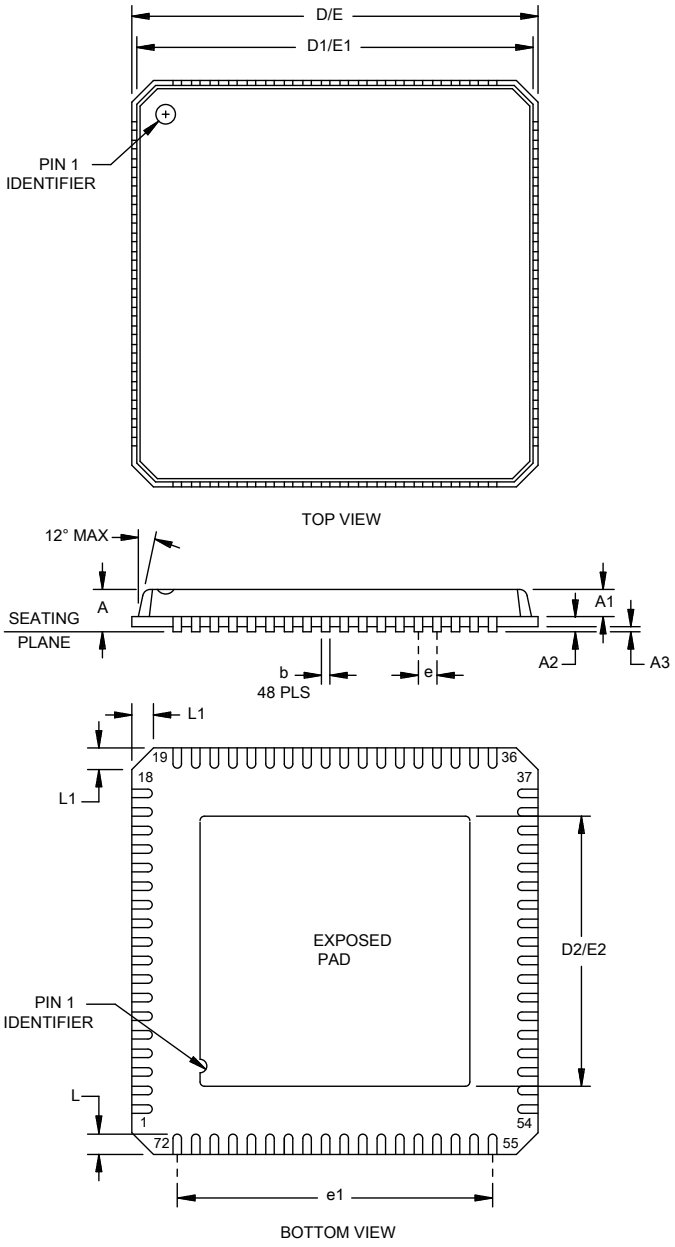

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12654
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Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D1/E1	9.75 BSC	
A1		0.80	D2/E2	5.85	6.15
A2	0.20 REF		e	0.50 BSC	
A3		0.05	e1	8.50 REF	
b	0.18	0.30	L	0.30	0.50
D/E	10.00 BSC		L1	0.24	0.60

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-VNND-4.

FIGURE 1. Case outline - Continued.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CVDD18	19	D11P	37	D4P	55	NC
2	DACCLKP	20	D11N	38	D4N	56	AVSS
3	DACCLKN	21	D10P	39	D3P	57	AVDD33
4	CVSS	22	D10N	40	D3N	58	IOUT2P
5	FRAMEP	23	D9P	41	D2P	59	IOUT2N
6	FRAMEN	24	D9N	42	D2N	60	AVDD33
7	$\overline{\text{IRQ}}$	25	D8P	43	DVDD18	61	AVSS
8	D15P	26	D8N	44	DVSS	62	REFIO
9	D15N	27	DCIP	45	D1P	63	FSADJ
10	NC	28	DCIN	46	D1N	64	AVSS
11	IOVDD	29	DVDD18	47	D0P	65	AVDD33
12	DVDD18	30	DVSS	48	D0N	66	IOUT1N
13	D14P	31	D7P	49	DVDD18	67	IOUT1P
14	D14N	32	D7N	50	SDO	68	AVDD33
15	D13P	33	D6P	51	SDIO	69	REFCLKN
16	D13N	34	D6N	52	SCLK	70	REFCLKP
17	D12P	35	D5P	53	$\overline{\text{CS}}$	71	CVDD18
18	D12N	36	D5N	54	$\overline{\text{RESET}}$	72	CVDD18

NOTES:
1. Exposed PAD (EPAD) must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.
2. NC = No Connect. Do not connect to this pin.

FIGURE 2. Terminal connections.

Case outline X		
Terminal number	Mnemonic	**Description**
1	CVDD18	1.8 V clock supply. Supplies clock receivers, clock distribution, and PLL circuitry
2	DACCLKP	DAC clock input, positive.
3	DACCLKN	DAC clock input, negative.
4	CVSS	Clock supply common.
5	FRAMEP	Frame input, Positive. This pin must be tied to DVSS if not used.
6	FRAMEN	Frame input, Negative. This pin must be tied to DVDD18 if not used.
7	$\overline{\text{IRQ}}$	Interrupt request. Open rain, active low output. Connect an external pull-up to IOVDD through a 10 kΩ resistor.
8	D15P	Data bit 15 (MSB), Positive.
9	D15N	Data bit 15 (MSB), Negative.
10	NC	No connect. Do not connect to this pin.
11	IOVDD	Supply pin for Serial port I/O pins, $\overline{\text{RESERT}}$, and $\overline{\text{IRQ}}$. 1.8 V to 3.3 V can be supplied to this pin.
12	DVDD18	1.8 V digital supply. Supplies power to digital core and digital data ports.
13	D14P	Data bit 14, Positive.
14	D14N	Data bit 14, Negative.
15	D13P	Data bit 13, Positive.
16	D13N	Data bit 13, Negative.
17	D12P	Data bit 12, Positive.
18	D12N	Data bit 12, Negative.
19	D11P	Data bit 11, Positive.
20	D11N	Data bit 11, Negative.
21	D10P	Data bit 10, Positive.
22	D10N	Data bit 10, Negative.
23	D9P	Data bit 9, Positive.
24	D9N	Data bit 9, Negative.
25	D8P	Data bit 8, Positive.
26	D8N	Data bit 8, Negative.
27	DCIP	Data clock input, Positive.
28	DCIN	Data clock input, Negative.
29	DVDD18	1.8 V Digital supply. Supplies power to digital core and digital data ports.
30	DVSS	Digital common.
31	D7P	Data bit 7, Positive.
32	D7N	Data bit 7, Negative.
33	D6P	Data bit 6, Positive.
34	D6N	Data bit 6, Negative.
35	D5P	Data bit 5, Positive.
36	D5N	Data bit 5, Negative.

FIGURE 3. Terminal function.

Case outline X - Continued		
Terminal number	Mnemonic	**Description**
37	D4P	Data bit 4, Positive.
38	D4N	Data bit 4, Negative.
39	D3P	Data bit 3, Positive.
40	D3N	Data bit 3, Negative.
41	D2P	Data bit 2, Positive.
42	D2N	Data bit 2, Negative.
43	DVDD18	1.8 V Digital supply. Supplies power to digital core and digital data ports.
44	DVSS	Digital common.
45	D1P	Data bit 1, Positive.
46	D1N	Data bit 1, Negative.
47	D0P	Data bit 0, Positive.
48	D0N	Data bit 0, Negative.
49	DVDD18	1.8 V Digital supply. Supplies power to digital core and digital data ports.
50	SDO	Serial port data Output (CMOS levels with respect to IOVDD)
51	SDIO	Serial port data Input/Output (CMOS levels with respect to IOVDD)
52	SCLK	Serial port clock Input (CMOS levels with respect to IOVDD)
53	$\overline{CS}$	Serial port chip select, Active low (CMOS levels with respect to IOVDD)
54	$\overline{RESET}$	Reset, Active low (CMOS levels with respect to IOVDD)
55	NC	No Connect. Do not connect to this pin.
56	AVSS	Analog supply common.
57	AVDD33	3.3 V Analog supply.
58	IOUT2P	Q DAC Positive current output.
59	IOUT2N	Q DAC Negative current output.
60	AVDD33	3.3 V Analog supply.
61	AVSS	Analog supply common.
62	REFIO	Voltage reference. Nominally 1.2 V output. Should be decoupled to AVSS.
63	FSADJ	Full Scale current output adjust. Place a 10 kΩ resistor from this pin to AVSS.
64	AVSS	Analog supply common.
65	AVDD33	3.3 V Analog supply.
66	IOUT1N	I DAC Negative current output.
67	IOUT1P	I DAC Positive current output.
68	AVDD33	3.3 V Analog supply.
69	REFCLKN	PLL reference clock input, Negative. This pin has s secondary function as a synchronization input.
70	REFCLKP	PLL reference clock input, Positive. This pin has s secondary function as a synchronization input.
71	CVDD18	1.8 V Clock supply. Supplies clock receivers, clock distribution, and PLL circuitry
72	CVDD18	1.8 V Clock supply. Supplies clock receivers, clock distribution, and PLL circuitry
	EPAD	The exposed pad (EPAD) must be soldered to the ground plane (AVSS). The EPAD provides an electrical thermal, and mechanical connection to the board.

FIGURE 3. Terminal function - Continued.

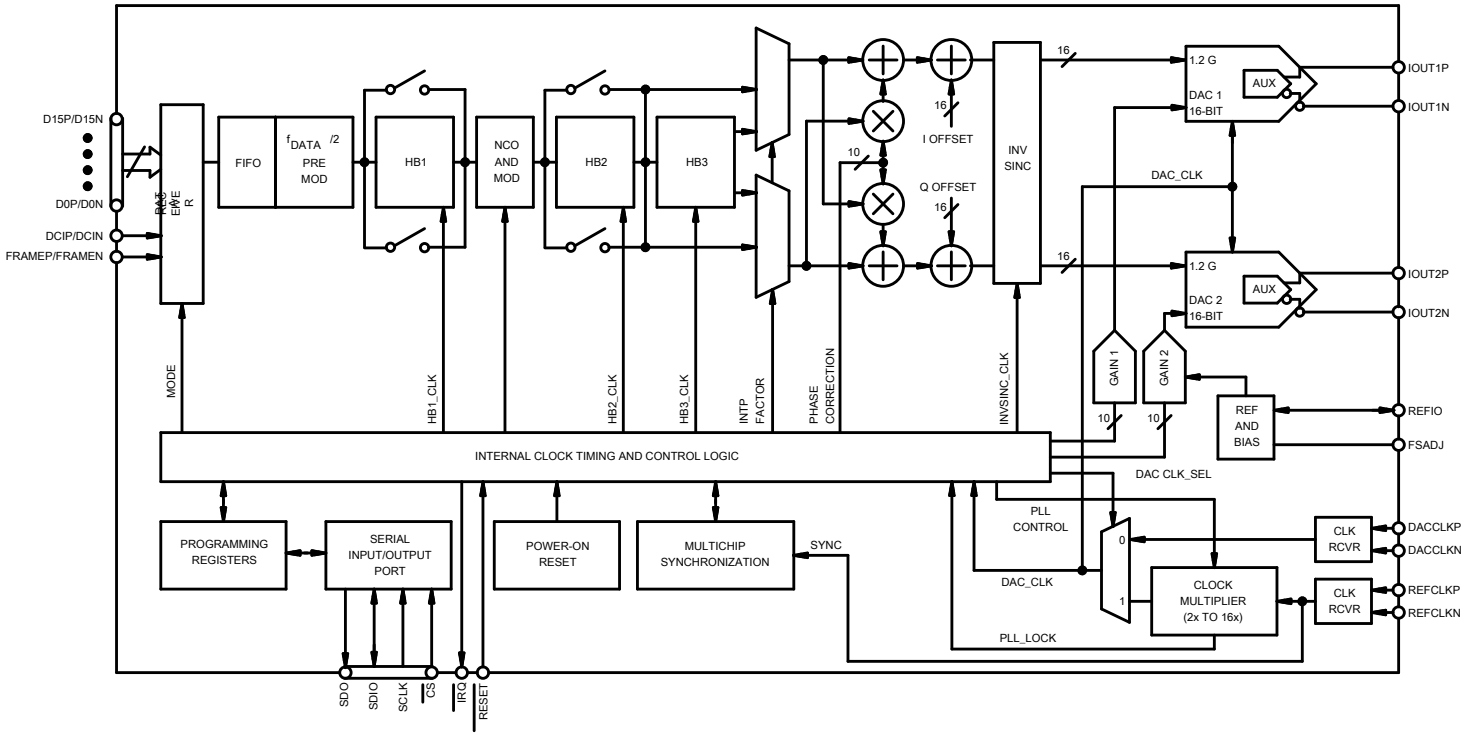

FIGURE 4. Functional block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12654
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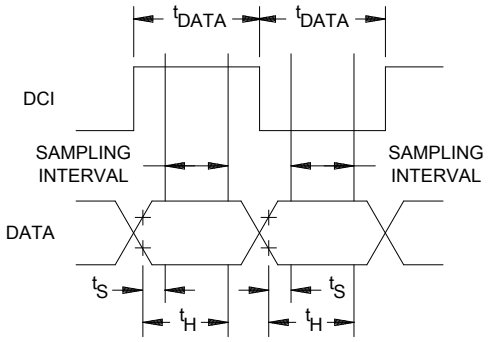

Data to DCI setup and hold times

DCI delay register 0x16, Bits[1:0]	Minimum setup time, t_s (ns)	Minimum hold time, t_H (ns)	Sampling interval (ns)
00	-0.01	0.65	0.64
01	-0.19	0.95	0.76
10	-0.38	1.22	0.84
11	-0.44	1.38	0.94

The data interface timing can be verified by using sample error detection (SED) circuitry. For more information, see the interface timing validation section in the manufacturer data sheet.

FIGURE 5. Timing diagram for input data port.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12654-01XE	24355	AD9122SCPZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland