REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make correction to CMRR V_S = 3.0 V test conditions column by deleting 4.0 V and replacing with 2.0 V as specified under Table I. Update document paragraphs to current requirements. - ro	18-08-21	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A									
	PAGE		1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 12-10-12	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	TITLE MICROCIRCUIT, LINEAR, 15 MHz, RAIL TO RAIL, DUAL OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE A **CODE IDENT. NO.** 16236	**DWG NO.** **V62/12639**
	REV A	**PAGE** 1 **OF** 10

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 15 MHz, rail to rail, dual operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12639	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OP262-EP	15 MHz. rail to rail, dual operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MS-012-AA	Standard small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage	±6 V	
Input voltage	±6 V	2/
Differential input voltage	±0.6 V	3/
Internal power dissipation SOIC (S)	Observe derating curves	
Output short circuit duration	Observe derating curves	
Operating temperature range:	-55°C to +125°C	
Storage temperature range	-65°C to +150°C	
Junction temperature range	-65°C to +150°C	
Lead temperature range (soldering, 10 seconds)	300°C	

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ For supply voltage greater than 6 V, the input voltage is limited to less than or equal to the supply voltage.
3/ For differential input voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input device.

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA} 4/	θ_{JC}	Unit
Case X	157	56	°C/W

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

4/ θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for a device soldered in circuit board for SOIC package.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions V_S = 5.0 V, V_{CM} = 0 V T_A = 25°C unless otherwise specified	Limits			Unit
			Min	Typ	Max	
Input characteristics						
Offset voltage	V_{OS}			45	325	µV
		-55°C ≤ T_A ≤ +125°C			1	mV
Input bias current	I_S			360	600	nA
		-55°C ≤ T_A ≤ +125°C			650	
Input offset current	I_{OS}			±2.5	±25	nA
		-55°C ≤ T_A ≤ +125°C			±40	
Input voltage range	V_{CM}		0		4	V
Common mode rejection	CMRR	0 V ≤ V_{CM} ≤ 4.0 V, -55°C ≤ T_A ≤ +125°C	70	110		dB
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_{OUT} ≤ 4.5 V		30		V/mV
		R_L = 10 kΩ, 0.5 V ≤ V_{OUT} ≤ 4.5 V	65	88		
		R_L = 10 kΩ, -55°C ≤ T_A ≤ +125°C	40			
Offset voltage drift 2/	$\Delta V_{OS}/\Delta T$			1		µV/°C
Bias current drift	$\Delta I_B/\Delta T$			250		pA/°C
Output characteristics						
Output voltage swing high	V_{OH}	I_L = 250 µA, -55°C ≤ T_A ≤ +125°C	4.95	4.99		V
		I_L = 5 mA	4.85	4.94		
Output voltage swing low	V_{OL}	I_L = 250 µA, -55°C ≤ T_A ≤ +125°C		14	50	mV
		I_L = 5 mA		65	150	
Short circuit current	I_{SC}	Short to ground		±80		mA
Maximum output current	I_{OUT}			±30		mA
Power supply						
Power supply rejection ratio	PSRR	V_S = 2.7 V to 7 V		120		dB
		-55°C ≤ T_A ≤ +125°C	90			
Supply current/Amplifier	I_{SY}	V_{OUT} = 2.5 V		500	700	µA
		-55°C ≤ T_A ≤ +125°C			850	
Dynamic performance						
Slew rate	SR	1 V ≤ V_{OUT} ≤ 4 V, R_L = 10 kΩ		10		V/µs
Settling time	t_S	To 0.1%, A_V = -1, V_O = 2 V step		540		ns
Gain bandwidth product	GBP			15		MHz
Phase margin	φm			61		Degrees

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions V_S = 3.0 V, V_{CM} = 0 V T_A = 25°C unless otherwise specified	Limits			Unit
			Min	Typ	Max	
Noise performance						
Voltage noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage noise density	e_n	f = 1 kHz		9.5		nV/$\sqrt{Hz}$
Current noise density	i_n	f = 1 kHz		0.4		pA/$\sqrt{Hz}$
Input characteristics						
Offset voltage	V_{OS}			50	325	µV
		-55°C ≤ T_A ≤ +125°C			1	mV
Input bias current	I_S			360	600	nA
Input offset current	I_{OS}			±2.5	±25	nA
Input voltage range	V_{CM}		0		2	V
Common mode rejection	CMRR	0 V ≤ V_{CM} ≤ 2.0 V, -55°C ≤ T_A ≤ +125°C	70	110		dB
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V		20		V/mV
		R_L = 10 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V	20	30		
Output characteristics						
Output voltage swing high	V_{OH}	I_L = 250 µA	2.95	2.99		V
		I_L = 5 mA	2.85	2.93		
Output voltage swing low	V_{OL}	I_L = 250 µA		14	50	mV
		I_L = 5 mA		66	150	
Power supply						
Power supply rejection ratio	PSRR	V_S = 2.7 V to 7 V		110		dB
		-55°C ≤ T_A ≤ +125°C	60			
Supply current/Amplifier	I_{SY}	V_{OUT} = 1.5 V		500	650	µA
		-55°C ≤ T_A ≤ +125°C			850	
Dynamic performance						
Slew rate	SR	R_L = 10 kΩ		10		V/µs
Settling time	t_S	To 0.1%, A_V = -1, V_O = 2 V step		575		ns
Gain bandwidth product	GBP			15		MHz
Phase margin	φm			59		Degrees
Noise performance						
Voltage noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage noise density	e_n	f = 1 kHz		9.5		nV/$\sqrt{Hz}$
Current noise density	i_n	f = 1 kHz		0.4		pA/$\sqrt{Hz}$

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions V_S = ±5.0 V, V_{CM} = 0 V T_A = 25°C unless otherwise specified	Limits			Unit
			Min	Typ	Max	
Input characteristics						
Offset voltage	V_{OS}			25	325	µV
		-55°C ≤ T_A ≤ +125°C			1	mV
Input bias current	I_S			260	500	nA
		-55°C ≤ T_A ≤ +125°C			650	
Input offset current	I_{OS}			±2.5	±25	nA
		-55°C ≤ T_A ≤ +125°C			±40	
Input voltage range	V_{CM}		-5		+4	V
Common mode rejection	CMRR	-4.9 V ≤ V_{CM} ≤ +4.0 V, -55°C ≤ T_A ≤ +125°C	70	110		dB
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, -4.5 V ≤ V_{OUT} ≤ +4.5 V		35		V/mV
		R_L = 10 kΩ, -4.5 V ≤ V_{OUT} ≤ 4.5 V	75	120		
		-55°C ≤ T_A ≤ +125°C	25			
Long term offset voltage 3/	V_{OS}				600	µV
Offset voltage drift 2/	$\Delta V_{OS}/\Delta T$			1		µV/°C
Bias current drift	$\Delta I_B/\Delta T$			250		pA/°C
Output characteristics						
Output voltage swing high	V_{OH}	I_L = 250 µA, -55°C ≤ T_A ≤ +125°C	4.95	4.99		V
		I_L = 5 mA	4.85	4.94		
Output voltage swing low	V_{OL}	I_L = 250 µA, -55°C ≤ T_A ≤ +125°C		-4.99	-4.95	V
		I_L = 5 mA		-4.94	-4.85	
Short circuit current	I_{SC}	Short to ground		±80		mA
Maximum output current	I_{OUT}			±30		mA
Power supply						
Power supply rejection ratio	PSRR	V_S = ±1.35 V to ±6 V		110		dB
		-55°C ≤ T_A ≤ +125°C	60			
Supply current/Amplifier	I_{SY}	V_{OUT} = 0 V		650	800	µA
		-55°C ≤ T_A ≤ +125°C			1.15	mA
		V_{OUT} = 0 V		550	775	µA
		-55°C ≤ T_A ≤ +125°C			1	mA
Supply voltage range	V_S		3.0 (±1.5)		12 (±6)	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

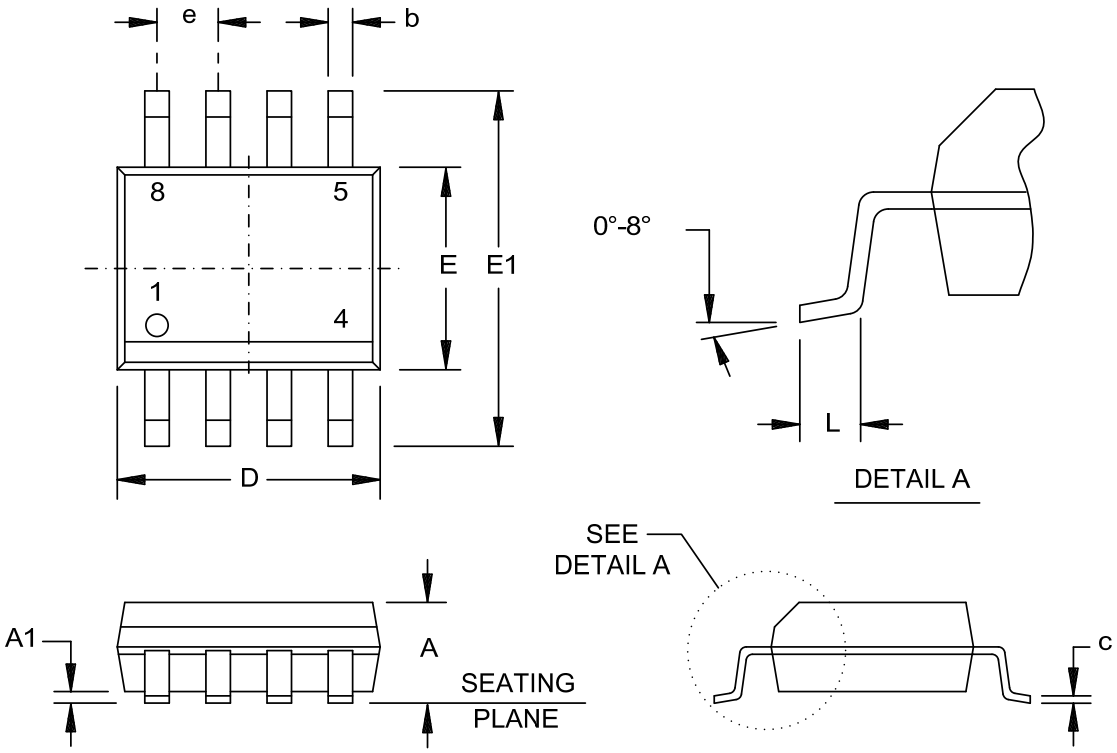
Test	Symbol	Test conditions V_S = ±5.0 V, V_{CM} = 0 V T_A = 25°C unless otherwise specified	Limits			Unit
			Min	Typ	Max	
Dynamic performance						
Slew rate	SR	-4 V ≤ V_{OUT} ≤ +4 V, R_L = 10 kΩ		13		V/µs
Settling time	t_S	To 0.1%, A_V = -1, V_O = 2 V step		475		ns
Gain bandwidth product	GBP			15		MHz
Phase margin	φm			64		Degrees
Noise performance						
Voltage noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage noise density	e_n	f = 1 kHz		9.5		nV/$\sqrt{Hz}$
Current noise density	i_n	f = 1 kHz		0.4		pA/$\sqrt{Hz}$

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Offset voltage drift is the average of the -55°C to +25°C delta and the +25°C to +125°C delta.

3/ Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125°C, with a LTPD of 1.3.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.35	1.75	.053	.068	E	3.80	4.00	.149	.157
A1	0.10	0.25	.004	.009	E1	5.80	6.20	.228	.244
b	0.31	0.51	.012	.020	e	1.27 BSC		.050 BSC	
c	0.17	0.25	.006	.009	L	0.40	1.27	.015	.050
D	4.80	5.00	.189	.197					

NOTES:
1. Controlling dimensions are in millimeters; inch dimensions are rounded-off millimeter equivalents for reference only and are not appropriate for use in design.
2. Falls within JEDEC MS-012-AA.

FIGURE 1. Case outline.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT A
2	-IN A
3	+IN A
4	V-
5	+IN B
6	-IN B
7	OUT B
8	V +

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/12639-01XE	24355	Reel, 1,000 units	OP262TRZ-EP-R7
V62/12639-01XE	24355	Tube, 98 units	OP262TRZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland