

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - ro	17-08-10	C. SAFFLE



Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/	
Original date of drawing YY-MM-DD 12-09-14	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, SINGLE SUPPLY, LOW POWER FET INPUT OPERATIONAL AMPLIFIER, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE	DWG NO. V62/12636	
	SIZE A	CODE IDENT. NO. 16236	PAGE 1 OF 17
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single supply, low power field effect transistor (FET) input operational microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/12636</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD822	Single supply, low power FET input operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (VS)	±18 V
Input voltage (VIN)	+VS + 0.2 V to -VS - 20 V
Output short duration	Indefinite
Differential input voltage	±30 V
Internal power dissipation (PD)	156.25 mW typical
Maximum junction temperature (TJ)	150°C
Storage temperature range (TSTG)	-65°C to +150°C
Lead temperature (soldering, 60 seconds)	+260°C

1.4 Recommended operating conditions. 2/

Supply voltage range (VS)	±15 V
Operating temperature range (TA)	-55°C to +125°C

1.5 Thermal characteristics.

Thermal resistance, junction to case (θJC)	43°C/W
Thermal resistance, junction to ambient (θJA)	160°C/W

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions VS = 0 V, 5 V, VCM = 0 V, VOUT = 0.2 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
DC performance.							
Initial offset voltage	V _{IO}		+25°C	01		0.8	mV
			-55°C to +125°C			1.2	
Initial offset voltage drift	ΔV _{IO}		-55°C to +125°C	01	2 typical		μV/ °C
Input bias current	I _{IB}	V _{CM} = 0 V to 4 V	+25°C	01		25	pA
			-55°C to +125°C			6	
Input offset current	I _{IO}		+25°C	01		20	pA
			-55°C to +125°C		0.5 typical		
Open loop gain	AO	V _{OUT} = 0.2 V to 4 V, R _L = 100 kΩ	+25°C	01	500		V/mV
			-55°C to +125°C		400		
		V _{OUT} = 0.2 V to 4 V, R _L = 10 kΩ	+25°C		80		
			-55°C to +125°C		80		
		V _{OUT} = 0.2 V to 4 V, R _L = 1 kΩ	+25°C		15		
			-55°C to +125°C		10		
Noise/harmonic performance.							
Input voltage noise	NV	f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		μV _{pp}
		f = 10 Hz			25 typical		
		f = 100 Hz			21 typical		
		f = 1 kHz			16 typical		
		f = 10 kHz			13 typical		
Input current noise	NI	f = 0.1 Hz to 10 Hz	+25°C	01	18 typical		f _{App}
		f = 1 kHz			0.8 typical		fA / √Hz
Harmonic distortion		V _{OUT} = 0.25 V to 4.75 V, f = 10 kHz, R _L = 10 kΩ to 2.5 V	+25°C	01	-93 typical		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VS = 0 V, 5 V, VCM = 0 V, VOUT = 0.2 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Unity gain frequency			+25°C	01	1.8 typical		MHz
Full power response		VOUTpp = 4.5 V	+25°C	01	210 typical		kHz
Slew rate	SR		+25°C	01	3 typical		V/μs
Settling time	tS	To 0.1%, VOUT = 0.2 V to 4.5 V	+25°C	01	1.4 typical		μs
		To 0.01%, VOUT = 0.2 V to 4.5 V			1.8 typical		
Matching characteristics.							
Initial offset voltage	VIO		+25°C	01		1.0	mV
			-55°C to +125°C			1.6	
Initial offset voltage drift	ΔVIO		+25°C	01	3 typical		μV/°C
Input bias current	IIB		+25°C	01		20	pA
Crosstalk	CT	At f = 1 kHz, RL = 5 kΩ	+25°C	01	-130 typical		dB
		At f = 100 kHz, RL = 5 kΩ			-93 typical		
Input characteristics.							
Input voltage range 2/			-55°C to +125°C	01	-0.2	+4	V
Common mode rejection ratio	CMRR	VCM = 0 V to 2 V	+25°C	01	66		dB
			-55°C to +125°C		66		
Differential input impedance	Z		+25°C	01	10 ¹³ 0.5 typical		Ω pF
Common mode input impedance	Z		+25°C	01	10 ¹³ 2.8 typical		Ω pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VS = 0 V, 5 V, VCM = 0 V, VOUT = 0.2 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit				
					Min	Max					
Output characteristics.											
Output saturation $\frac{3}{\text{voltage}}$		VOL – VEE, ISINK = 20 μ A	+25°C	01		7	mV				
			-55°C to +125°C			10					
		VCC – VOH, ISOURCE = 20 μ A	+25°C			14					
			-55°C to +125°C			20					
		VOL – VEE, ISINK = 2 mA	+25°C			55					
			-55°C to +125°C			80					
		VCC – VOH, ISOURCE = 2 mA	+25°C			110					
			-55°C to +125°C			160					
		VOL – VEE, ISINK = 15 mA	+25°C			500					
			-55°C to +125°C			1000					
		VCC – VOH, ISOURCE = 15 mA	+25°C			1500					
			-55°C to +125°C			1900					
		Operating output current	IOUT			+25°C		01	15		mA
						-55°C to +125°C			12		
Capacitive load drive	CL		+25°C	01	350 typical		pF				
Power supply.											
Quiescent current			-55°C to +125°C	01		1.6	mA				
Power supply rejection ratio	PSRR	+VS = 5 V to 15 V	+25°C	01	66		dB				
			-55°C to +125°C		66						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VS = ±5 V, VCM = 0 V, VOUT = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit	
					Min	Max		
DC performance.								
Initial offset voltage	V _{IO}		+25°C	01		0.8	mV	
			-55°C to +125°C			1.5		
Initial offset voltage drift	ΔV _{IO}		+25°C	01	2 typical		μV/ °C	
Input bias current	I _{IB}	V _{CM} = -5 V to 4 V	+25°C	01		25	pA	
			-55°C to +125°C			6		nA
Input offset current	I _{IO}		+25°C	01		20	pA	
			-55°C to +125°C		0.5 typical			nA
Open loop gain	AO	V _{OUT} = -4 V to 4 V, R _L = 100 kΩ	+25°C	01	400		V/mV	
			-55°C to +125°C		400			
		V _{OUT} = -4 V to 4 V, R _L = 10 kΩ	+25°C		80			
			-55°C to +125°C		80			
		V _{OUT} = -4 V to 4 V, R _L = 1 kΩ	+25°C		20			
			-55°C to +125°C		10			
Noise/harmonic performance.								
Input voltage noise	NV	f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		μV _{pp}	
		f = 10 Hz			25 typical			nV / √Hz
		f = 100 Hz			21 typical			
		f = 1 kHz			16 typical			
		f = 10 kHz			13 typical			
Input current noise	NI	f = 0.1 Hz to 10 Hz	+25°C	01	18 typical		fA _{pp}	
		f = 1 kHz			0.8 typical		fA / √Hz	
Harmonic distortion		V _{OUT} = ±4.5 V, f = 10 kHz, R _L = 10 kΩ	+25°C	01	-93 typical		dB	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VS = ±5 V, VCM = 0 V, VOUT = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Dynamic performance.							
Unity gain frequency			+25°C	01	1.9 typical		MHz
Full power response		VOUTpp = 9 V	+25°C	01	105 typical		kHz
Slew rate	SR		+25°C	01	3 typical		V/μs
Settling time	tS	To 0.1%, VOUT = 0 V to ±4.5 V	+25°C	01	1.4 typical		μs
		To 0.01%, VOUT = 0 V to ±4.5 V			1.8 typical		
Matching characteristics.							
Initial offset voltage	VIO		+25°C	01		1.0	mV
			-55°C to +125°C			3	
Initial offset voltage drift	ΔVIO		-55°C to +125°C	01	3 typical		μV/°C
Input bias current	IIB		+25°C	01		25	pA
Crosstalk	CT	At f = 1 kHz, RL = 5 kΩ	+25°C	01	-130 typical		dB
		At f = 100 kHz, RL = 5 kΩ			-93 typical		
Input characteristics.							
Input voltage range 2/			-55°C to +125°C	01	-5.2	+4	V
Common mode rejection ratio	CMRR	VCM = -5 V to 2 V	+25°C	01	66		dB
			-55°C to +125°C		66		
Differential input impedance	Z		+25°C	01	10 ¹³ 0.5 typical		Ω pF
Common mode input impedance	Z		+25°C	01	10 ¹³ 2.8 typical		Ω pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 5\text{ V}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit				
					Min	Max					
Output characteristics.											
Output saturation $\frac{3}{\text{voltage}}$		$V_{OL} - V_{EE}$, $I_{SINK} = 20\ \mu\text{A}$	+25°C	01		7	mV				
			-55°C to +125°C			10					
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 20\ \mu\text{A}$	+25°C			14					
			-55°C to +125°C			20					
		$V_{OL} - V_{EE}$, $I_{SINK} = 2\text{ mA}$	+25°C			55					
			-55°C to +125°C			80					
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 2\text{ mA}$	+25°C			110					
			-55°C to +125°C			160					
		$V_{OL} - V_{EE}$, $I_{SINK} = 15\text{ mA}$	+25°C			500					
			-55°C to +125°C			1000					
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 15\text{ mA}$	+25°C			1500					
			-55°C to +125°C			1900					
		Operating output current	I_{OUT}			+25°C		01	15		mA
						-55°C to +125°C			12		
Capacitive load drive	C_L		+25°C	01	350 typical		pF				
Power supply.											
Quiescent current			-55°C to +125°C	01		1.6	mA				
Power supply rejection ratio	PSRR	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$	+25°C	01	66		dB				
			-55°C to +125°C		66						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance.							
Initial offset voltage	V_{IO}		+25°C	01		2	mV
			-55°C to +125°C			3	
Initial offset voltage drift	ΔV_{IO}		-55°C to +125°C	01	2 typical		$\mu\text{V}/^\circ\text{C}$
Input bias current	I_{IB}	$V_{CM} = 0\text{ V}$	+25°C	01		25	pA
		$V_{CM} = -10\text{ V}$			40 typical		
		$V_{CM} = 0\text{ V}$	-55°C to +125°C			6	nA
Input offset current	I_{IO}		+25°C	01		20	pA
			-55°C to +125°C		0.5 typical		nA
Open loop gain	AO	$V_{OUT} = -10\text{ V to }10\text{ V}$, $R_L = 100\text{ k}\Omega$	+25°C	01	500		V/mV
			-55°C to +125°C		500		
		$V_{OUT} = -10\text{ V to }10\text{ V}$, $R_L = 10\text{ k}\Omega$	+25°C		100		
			-55°C to +125°C		100		
		$V_{OUT} = -10\text{ V to }10\text{ V}$, $R_L = 1\text{ k}\Omega$	+25°C		30		
			-55°C to +125°C		20		
Noise/harmonic performance.							
Input voltage noise	NV	$f = 0.1\text{ Hz to }10\text{ Hz}$	+25°C	01	2 typical		μV_{pp}
		$f = 10\text{ Hz}$			25 typical		$\text{nV} / \sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$			21 typical		
		$f = 1\text{ kHz}$			16 typical		
		$f = 10\text{ kHz}$			13 typical		
Input current noise	NI	$f = 0.1\text{ Hz to }10\text{ Hz}$	+25°C	01	18 typical		fApp
		$f = 1\text{ kHz}$			0.8 typical		$\text{fA} / \sqrt{\text{Hz}}$

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Noise/harmonic performance - continued.							
Harmonic distortion		$V_{OUT} = \pm 10\text{ V}$, $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$	+25°C	01	-85 typical		dB
Dynamic performance.							
Unity gain frequency			+25°C	01	1.9 typical		MHz
Full power response		$V_{OUTpp} = 20\text{ V}$	+25°C	01	45 typical		kHz
Slew rate	SR		+25°C	01	3 typical		V/ μs
Settling time	t_S	To 0.1%, $V_{OUT} = 0\text{ V}$ to $\pm 10\text{ V}$	+25°C	01	4.1 typical		μs
		To 0.01%, $V_{OUT} = 0\text{ V}$ to $\pm 10\text{ V}$			4.5 typical		
Matching characteristics.							
Initial offset voltage	V_{IO}		+25°C	01		3	mV
			-55°C to +125°C			4	
Initial offset voltage drift	ΔV_{IO}		-55°C to +125°C	01	3		$\mu\text{V}/^\circ\text{C}$
Input bias current	I_{IB}		+25°C	01		25	pA
Crosstalk	CT	At $f = 1\text{ kHz}$, $R_L = 5\text{ k}\Omega$	+25°C	01	-130 typical		dB
		At $f = 100\text{ kHz}$, $R_L = 5\text{ k}\Omega$			-93 typical		
Input characteristics.							
Input voltage range 2/			-55°C to +125°C	01	-15.2	+14	V
Common mode rejection ratio	CMRR	$V_{CM} = -15\text{ V}$ to +12 V	+25°C	01	70		dB
			-55°C to +125°C		70		
Differential input impedance	Z		+25°C	01	$10^{13} 0.5$ typical		ΩpF
Common mode input impedance	Z		+25°C	01	$10^{13} 2.8$ typical		ΩpF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_S = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output characteristics.							
Output saturation ^{3/} voltage		$V_{OL} - V_{EE}$, $I_{SINK} = 20\ \mu\text{A}$	+25°C	01		7	mV
			-55°C to +125°C			10	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 20\ \mu\text{A}$	+25°C			14	
			-55°C to +125°C			20	
		$V_{OL} - V_{EE}$, $I_{SINK} = 2\text{ mA}$	+25°C			55	
			-55°C to +125°C			80	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 2\text{ mA}$	+25°C			110	
			-55°C to +125°C			160	
		$V_{OL} - V_{EE}$, $I_{SINK} = 15\text{ mA}$	+25°C			500	
			-55°C to +125°C			1000	
		$V_{CC} - V_{OH}$, $I_{SOURCE} = 15\text{ mA}$	+25°C			1500	
			-55°C to +125°C			1900	
Operating output current	I_{OUT}		+25°C	01	20		mA
			-55°C to +125°C		15		
Capacitive load drive	C_L		+25°C	01	350 typical		pF
Power supply.							
Quiescent current			-55°C to +125°C	01		1.8	mA
Power supply rejection ratio	PSRR	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$	+25°C	01	70		dB
			-55°C to +125°C		70		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This is a functional specification. Amplifier bandwidth decreases when the input common mode voltage is driven in the range (+ $V_S - 1\text{ V}$) to + V_S . Common mode error voltage is typically less than 5 mV with the common mode voltage set at 1 V below the positive supply.
- 3/ $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

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Case X

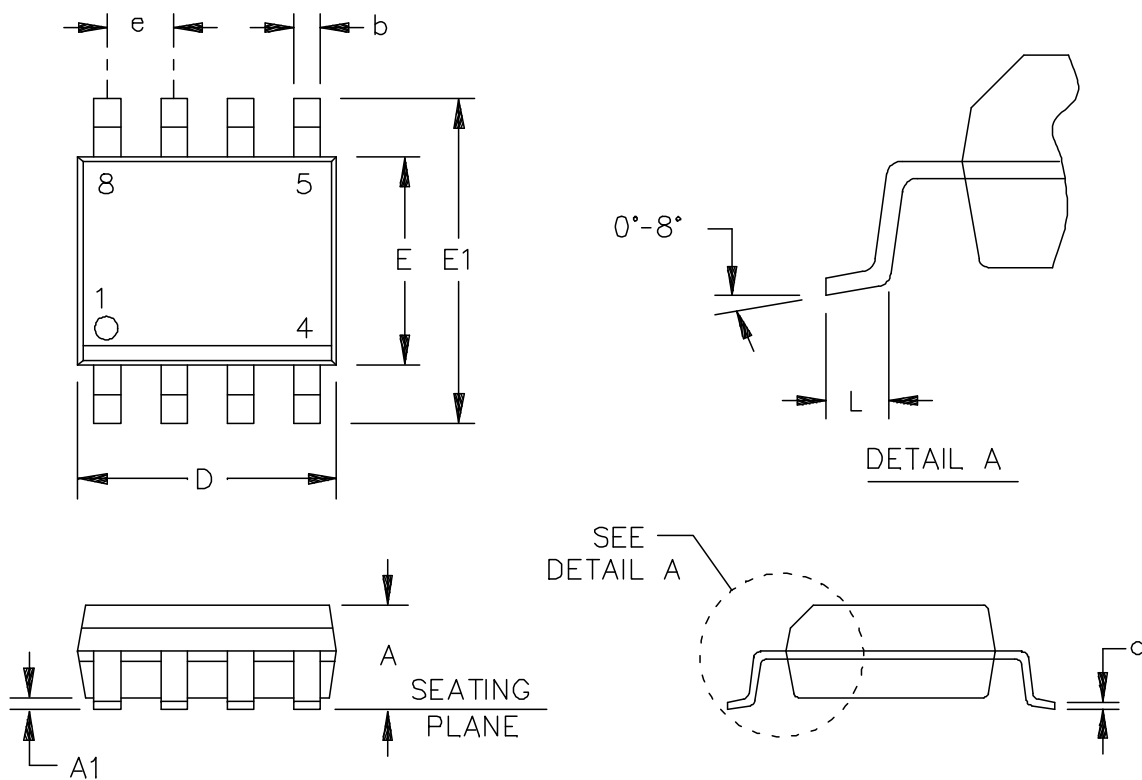


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/12636</p>
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.053	.068	1.35	1.75
A1	.003	.009	0.10	0.25
b	.012	.020	0.31	0.51
c	.006	.009	0.17	0.25
D	.188	.196	4.80	5.00
E	.149	.157	3.80	4.00
E1	.228	.244	5.80	6.20
e	.049 BSC		1.27 BSC	
L	.015	.049	0.40	1.27

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUTPUT 1
2	-INPUT 1
3	+INPUT 1
4	-Vs
5	+INPUT 2
6	-INPUT 2
7	OUTPUT 2
8	+Vs

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/12636-01XE	24355	AD822TRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: Raheen Business Park
 Limerick, Ireland

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