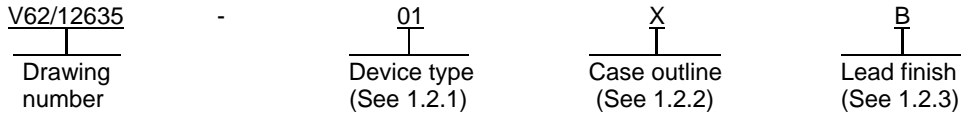


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 channel, 1 million samples per second (MSPS), 12 bit analog to digital converter with sequencer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD7490-EP	16 channel, 1 MSPS, 12 bit analog to digital converter with sequencer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	28	MO-153-AE	Plastic thin shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage (VDD) to ground (GND)	-0.3 V to +7 V
Logic power supply input (VDRIVE) to GND	-0.3 V to VDD + 0.3 V
Analog input voltage to GND	-0.3 V to VDD + 0.3 V
Digital input voltage to GND	-0.3 V to 7 V
Digital output voltage to GND	-0.3 V to VDD + 0.3 V
Reference input (REFIN) to GND	-0.3 V to VDD + 0.3 V
Input current to any pin except supplies	±10 m A 2/
Power dissipation (PD)	450 mW
Junction temperature range (TJ)	150°C
Storage temperature range (TSTG)	-65°C to +150°C
Lead temperature, soldering :	
Vapor phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Electrostatic discharge (ESD)	1 kV

1.4 Recommended operating conditions. 3/ 4/

Supply voltage (VDD) range	+4.75 V to +5.25 V
Operating free-air temperature range (TA)	-55°C to +125°C

1.5 Thermal characteristics.

Thermal impedance, junction to case(θ_{JC})	14°C/W
Thermal impedance, junction to ambient (θ_{JA})	97.9°C/W

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 4/ All ratings and specifications, please refer to the relevant manufacturer’s EP datasheet.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at <https://www.jedec.org>).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Load circuit for digital output timing specifications. The load circuit for digital output timing specifications shall be as shown in figure 1.

3.5.2 Case outline. The case outline shall be as shown in 1.2.2 and figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/12635</p>
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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Dynamic performance							
Signal to (noise + distortion)	SINAD	f _{IN} = 50 kHz sine wave, f _{SCLK} = 20 MHz	-55°C to +125°C	01	69		dB
Signal to noise ratio	SNR		-55°C to +125°C	01	69.5		dB
Total harmonic distortion	THD		-55°C to +125°C	01		-74	dB
Peak harmonic or spurious noise	SFDR		-55°C to +125°C	01		-75	dB
Intermodulation distortion	IMD	f _a = 40.1 kHz, f _b = 41.5 kHz					
Second order terms			-55°C to +125°C	01	-85 typical		dB
Third order terms			-55°C to +125°C	01	-85 typical		dB
Aperture delay			-55°C to +125°C	01	10 typical		ns
Aperture jitter			-55°C to +125°C	01	50 typical		ps
Channel to channel isolation		f _{IN} = 400 kHz	-55°C to +125°C	01	-82 typical		dB
Full power bandwidth	FPBW	3 dB	-55°C to +125°C	01	8.2 typical		MHz
		0.1 dB			1.6 typical		
DC accuracy							
Resolution			-55°C to +125°C	01	12		Bits
Integral nonlinearity			-55°C to +125°C	01		±1	LSB
Differential nonlinearity		Guaranteed no missed codes to 12 bits	-55°C to +125°C	01	-0.95	+1.5	LSB
0 V to REFIN input range		Straight binary output coding					
Offset error			-55°C to +125°C	01		±8	LSB
Offset error match			-55°C to +125°C	01		±0.5	LSB
Gain error			-55°C to +125°C	01		±2	LSB
Gain error match			-55°C to +125°C	01		±0.6	LSB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
DC accuracy – continued.							
0 V to 2 x REF _{IN} input range		-REF _{IN} to +REF _{IN} biased about REF _{IN} with two's complement output coding offset					
Positive gain error			-55°C to +125°C	01		±2	LSB
Positive gain error match			-55°C to +125°C	01		±0.5	LSB
Zero code error			-55°C to +125°C	01		±8	LSB
Zero code error match			-55°C to +125°C	01		±0.5	LSB
Negative gain error			-55°C to +125°C	01		±1	LSB
Negative gain error match			-55°C to +125°C	01		±0.5	LSB
Analog input.							
Input voltage range	V _{IN}	Range bit set to 1	-55°C to +125°C	01	0	REF _{IN}	V
		Range bit set to 0			0	2 x REF _{IN}	
DC leakage current			-55°C to +125°C	01		±1	μA
Input capacitance	C _{IN}		-55°C to +125°C	01	20 typical		pF
Reference input.							
REF _{IN} input voltage		±1% specified performance	-55°C to +125°C	01	2.5 typical		V
DC leakage current			-55°C to +125°C	01		±1	μA
REF _{IN} input impedance		f _{SAMPLE} = 1 MSPS	-55°C to +125°C	01	36 typical		kΩ

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Logic inputs.							
Input high voltage	V _{INH}		-55°C to +125°C	01	0.7 x V _{DRIVE}		V
Input low voltage	V _{INL}		-55°C to +125°C	01		0.3 x V _{DRIVE}	V
Input current	I _{IN}	V _{IN} = 0 V or V _{DRIVE}	-55°C to +125°C	01		±1	μA
Input capacitance <u>3/</u>	C _{IN +}		-55°C to +125°C	01		10	pF
Logic outputs.							
Output high voltage	V _{OH}	I _{SOURCE} = 200 μA	-55°C to +125°C	01	V _{DRIVE} - 0.2		V
Output low voltage	V _{OL}	I _{SINK} = 200 μA	-55°C to +125°C	01		0.4	V
Floating state leakage current		WEAK/ $\overline{\text{TRI}}$ bit set to 0	-55°C to +125°C	01		±10	μA
Floating state <u>3/</u> output capacitance		WEAK/ $\overline{\text{TRI}}$ bit set to 0	-55°C to +125°C	01		10	pF
Output coding		Coding bit set to 1	-55°C to +125°C	01	Straight natural binary		
		Coding bit set to 0			Two's complement		
Conversion rate.							
Conversion time		16 SCLK cycles, SCLK = 20 MHz	-55°C to +125°C	01		800	ns
Track and hold acquisition time		Sine wave input	-55°C to +125°C	01		300	ns
		Full scale step input				300	
Throughput rate			-55°C to +125°C	01		1	MSPS
Power requirements.							
Power supply input	V _{DD}		-55°C to +125°C	01	4.75	5.25	V
Logic power supply input	V _{DRIVE}		-55°C to +125°C	01	2.7	5.25	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Power requirements - continued.							
Power supply current	I _{DD}	Digital inputs = 0 V or V _{DRIVE}					
Normal mode (static)		SCLK on or off	-55°C to +125°C	01	600 typical		μA
Normal mode (operational)		fSCLK = 20 MHz, fS = maximum throughput	-55°C to +125°C	01		2.5	mA
Auto standby mode		fSAMPLE = 500 kSPS	-55°C to +125°C	01	1.55 typical		mA
		Static				100	
Auto shutdown		fSAMPLE = 250 kSPS	-55°C to +125°C	01	960 typical		μA
		Static				0.5	
Full shutdown mode		SCLK on or off	-55°C to +125°C	01		0.5	μA
Power dissipation .							
Normal mode (operational)		fSCLK = 20 MHz	-55°C to +125°C	01		12.5	mW
Auto standby mode (static)			-55°C to +125°C	01		460	μW
Auto shutdown mode (static)			-55°C to +125°C	01		2.5	μW
Full shutdown mode			-55°C to +125°C	01		2.5	μW

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>4/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Timing specification. <u>5/</u>							
Clock frequency <u>6/</u>	fSCLK		-55°C to +125°C	01	10		kHz
						20	MHz
Convert timing	t _{CONVERT}		-55°C to +125°C	01	16 x t _{SCLK}		
Minimum quiet timing required between bus relinquish and start of next conversion	t _{QUIET}		-55°C to +125°C	01	50		ns
$\overline{\text{CS}}$ to SCLK setup time	t ₂		-55°C to +125°C	01	10		ns
Delay from $\overline{\text{CS}}$ <u>7/</u> until DOUT three state disabled	t ₃		-55°C to +125°C	01		14	ns
Delay from $\overline{\text{CS}}$ to <u>8/</u> DOUT valid	t _{3b}		-55°C to +125°C	01		20	ns
Data access time <u>7/</u> after SCLK falling edge	t ₄		-55°C to +125°C	01		40	ns
SCLK low pulse width	t ₅		-55°C to +125°C	01	0.4 x t _{SCLK}		ns
SCLK high pulse width	t ₆		-55°C to +125°C	01	0.4 x t _{SCLK}		ns
SCLK to DOUT valid hold time	t ₇		-55°C to +125°C	01	15		ns
SCLK falling edge <u>9/</u> to DOUT high impedance	t ₈		-55°C to +125°C	01	15	50	ns
DIN setup time prior to SCLK falling edge	t ₉		-55°C to +125°C	01	20		ns
DIN hold time after SCLK falling edge	t ₁₀		-55°C to +125°C	01	5		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>4/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Timing specification continued. <u>5/</u>							
16th SCLK falling edge to $\overline{\text{CS}}$ high	t ₁₁		-55°C to +125°C	01	20		ns
Power up time from full power down/ auto shutdown/ auto standby modes	t ₁₂		-55°C to +125°C	01		1	μs

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, V_{DD} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, and f_{SCLK} = 20 MHz. Specifications apply for f_{SCLK} up to 20 MHz. However, for serial interfacing requirements, see manufacturer's datasheet.
- 3/ Guaranteed by characterization.
- 4/ Unless otherwise specified, V_{DD} = 4.75 V to 5.25 V, V_{DRIVE} ≤ V_{DD}, and REF_{IN} = 2.5 V.
- 5/ Guaranteed by characterization. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V, see figure1.
- 6/ The mark/space ratio for the SCLK input is 40/60 to 60/40.
- 7/ Measured with the load circuit of figure 1 and defined as the time required for the output to cross 0.4 V or 0.7 V_{DRIVE}.
- 8/ t_{3b} represents a worst case figure for having ADD3 available on the DOUT line, that is, if the device goes back into three state at the end of conversion and some other device takes control of the bus between conversions, the user has to wait a maximum time of t_{3b} before having ADD3 valid on the DOUT line. If the DOUT line is weakly driven to ADD3 between conversions, the user typically has to wait 12 ns at 5 V after the $\overline{\text{CS}}$ falling edge before seeing ADD3 valid on DOUT.
- 9/ t₈ is derived from the measured by the data outputs to change 0.5 V when loaded with the circuit of figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t₈, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

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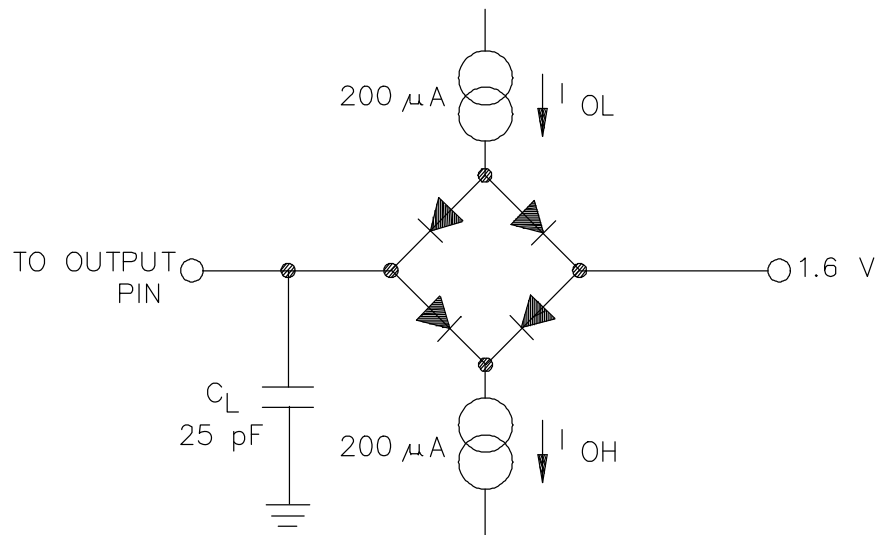


FIGURE 1. Load circuit for digital output timing specifications.

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Case X

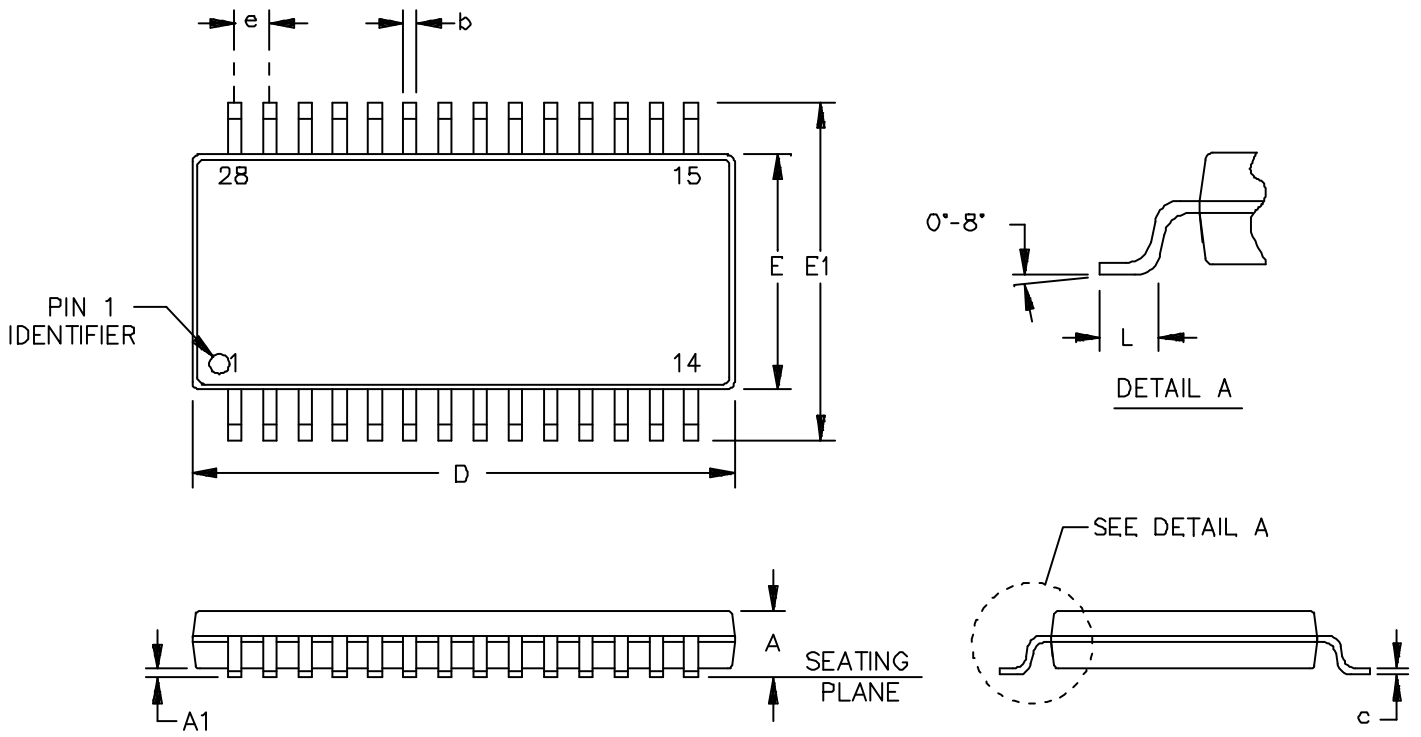


FIGURE 2. Case outline.

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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.003	.007	0.09	0.20
D	.377	.385	9.60	9.80
E	.169	.177	4.30	4.50
E1	.251 BSC		6.40 BSC	
e	.025 BSC		0.65 BSC	
L	.017	.029	.045	075

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AE.

FIGURE 2. Case outline - Continued.

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Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VIN11	15	DOUT
2	VIN10	16	SCLK
3	VIN9	17	VDRIVE
4	NC	18	NC
5	VIN8	19	DIN
6	VIN7	20	$\overline{\text{CS}}$
7	VIN6	21	AGND
8	VIN5	22	VDD
9	VIN4	23	REFIN
10	VIN3	24	AGND
11	VIN2	25	VIN15
12	VIN1	26	VIN14
13	VIN0	27	VIN13
14	AGND	28	VIN12

FIGURE 3. Terminal connections.

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Terminal symbol	Description
$\overline{\text{CS}}$	Chip select. Active low logic input. This input provides the dual function of initiating conversions on the device and also frames the serial data transfer.
REFIN	Reference input for the device. An external reference must be applied to this input. The voltage range for the external reference is $2.5 \text{ V} \pm 1\%$ for specified performance.
VDD	Power supply input. The VDD range for the device is from 2.7 V to 5.25 V. For the 0 V to 2 x REFIN range, VDD should be from 4.75 V to 5.25 V.
AGND	Analog ground. Ground reference point for all circuitry on the device. All analog/digital input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
VIN0 to VIN15	Analog input 0 through analog input 15. Sixteen single ended analog input channels that are multiplexed into the on chip track and hold. The analog input channel to be converted is selected by using the address bits ADD3 through ADD0 of the control register. The address bits, in conjunction with the SEQ and SHADOW bits, allow the sequence register to be programmed. The input range for all input channels can extend from 0 V to REFIN or 0 V to 2 x REFIN as selected via the RANGE bit in the control register. Any used input channels should be connected to AGND to avoid noise pickup.
DIN	Data in. Logic input. Data to be written to the control register of the device is provided on this input and is clocked into the register on the falling edge of SCLK.
DOUT	Data out. Logic out. The conversion result from the device is provided on this output as serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, which is provided by MSB first. The output coding can be selected as straight binary or twos complement via the CODING bit in the control register.
SCLK	Serial clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of the device.
VDRIVE	Logic power supply input. The voltage supplied at this pin determines at what voltage the serial interface of the device operates.

FIGURE 3. Terminal connections - continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/12635-01XB	24355	AD7490SRU-EP-RL7
V62/12635-01XE	24355	AD7490SRUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: Raheen Business Park
 Limerick, Ireland

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