REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add paragraph 1.4 and footnote 3/. Add typical limits to test parameters under Table I. Make correction to DIN pin description specified under figure 3 by deleting SCLK and replacing with DIN. Update document paragraphs to current requirements. - ro	18-04-10	C. SAFFLE
B	Delete the words, “IN A 10 LEAD PACKAGE” from the title block and paragraph 1.2.1. Make updates to b, c, and L dimension limits as specified under Figure 1. Made clarification to DIN terminal description as specified under Figure 3. Update document to current requirements. - ro	24-10-09	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B											
SHEET	1	2	3	4	5	6	7	8	9	10	11											

PMIC N/A

Original date of drawing YY-MM-DD 12-10-26

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TITLE

MICROCIRCUIT, LINEAR, 2.5 V TO 5.5 V, 500 µA, QUAD VOLTAGE OUTPUT 12 BIT, DAC, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/12628
REV B		PAGE 1 OF 11

AMSC N/A

5962-V087-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 2.5 V to 5.5 V, 500 µA, quad voltage output 12 bit digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12628	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	AD5324-EP	2.5 V to 5.5 V, 500 µA, quad voltage output 12 bit DAC

1.2.2 Case outline. The case outline are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	10	JEDEC MO-187-BA	Mini small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

V_{DD} to GND	-0.3 V to +7.0 V
Digital input voltage to GND	-0.3 V to V_{DD} + 0.3 V
Reference input voltage to GND	-0.3 V to V_{DD} + 0.3 V
V_{OUT}A through V_{OUT}D to GND	-0.3 V to V_{DD} + 0.3 V
Operating temperature range:	
Industrial	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature (T_J max)	150°C
Case outline X:	
Power dissipation	(T_J max – T_A) / θ_{JA}
θ_{JA} Thermal impedance	206°C/W
θ_{JC} Thermal impedance	44°C/W
Reflow soldering:	
Peak temperature	220°C
Time at peak temperature	10 seconds to 40 seconds

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{DD})	2.5 V to 5.5V

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Serial interface timing diagram. The serial interface timing diagram shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits		Unit
			Min	Max	
DC performance 3/					
Resolution			12 typical		Bits
Relative accuracy				±10	LSB
			±2 typical		
Differential nonlinearity 4/		5/		±1	LSB
			±0.2 typical		
Offset error		See FIGURE 5		±3	% of FSR
			±0.4 typical		
Gain error		See FIGURE 5		±1	% of FSR
			±0.15 typical		
Lower dead band		6/		60	mV
			20 typical		
Offset error drift 7/			-12 typical		ppm of FSR/°C
Gain error drift 7/			-5 typical		ppm of FSR/°C
DC power supply rejection ratio 7/		ΔV_{DD} = ±10%	-60 typical		dB
DC crosstalk 7/		R_L = 2 kΩ to GND or V_{DD}	200 typical		µV
DAC reference inputs 7/					
V_{REF} input range			0.25	V_{DD}	V
V_{REF} input impedance		Normal operation	37		kΩ
			45 typical		
		Power down mode	>10 typical		MΩ
Reference feedthrough		Frequency = 10 kHz	-90 typical		dB
Output characteristics 7/					
Minimum output voltage 8/		9/	0.001 typical		V
Maximum output voltage 8/		10/	V_{DD} – 0.001 typical		V
DC output impedance			0.5 typical		Ω
Short circuit current		V_{DD} = 5 V	25 typical		mA
		V_{DD} = 3 V	16 typical		
Power up time		Coming out of power down mode V_{DD} = 5 V	2.5 typical		µs
		Coming out of power down mode V_{DD} = 3 V	5 typical		
Logic inputs 7/					
Input current				±1	µA
Input low voltage	V_{IL}	V_{DD} = 5 V ±10%		0.8	V
		V_{DD} = 3 V ±10%		0.6	
		V_{DD} = 2.5 V		0.5	
Input high voltage	V_{IH}	V_{DD} = 5 V ±10%	2.4		V
		V_{DD} = 3 V ±10%	2.1		
		V_{DD} = 2.5 V	2.0		
Pin capacitance			3 typical		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits		Unit
			Min	Max	
Power requirements					
V_{DD}			2.5	5.5	V
I_{DD} (Normal mode) 11/		$V_{IH} = V_{DD}$ and V_{IL} = GND		900	µA
V_{DD} = 4.5 V to 5.5 V			600 typical		
V_{DD} = 2.5 V to 3.6 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		700	µA
			500 typical		
I_{DD} (Power down mode)		$V_{IH} = V_{DD}$ and V_{IL} = GND		1	µA
V_{DD} = 4.5 V to 5.5 V			0.2 typical		
V_{DD} = 2.5 V to 3.6 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		1	µA
			0.08 typical		
AC characteristics					
Output voltage settling time		$V_{REF} = V_{DD}$ = 5 V;		10	µs
		1/4 scale to 3/4 scale change (0x400 to 0xC00)	8 typical		
Slew rate			0.7 typical		V/µs
Major code transition glitch energy		1 LSB change around major carry	12 typical		nV-sec
Digital feedthrough			1 typical		nV-sec
Digital crosstalk			1 typical		nV-sec
DAC to DAC crosstalk			3 typical		nV-sec
Multiplying bandwidth		V_{REF} = 2 V ±0.1 V_{p-p}	200 typical		kHz
Total harmonic distortion		V_{REF} = 2.5 V ±0.1 V_{p-p}, frequency = 10 kHz	-70 typical		dB

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	2.5 V ≤ V_{DD} ≤ 3.6 V		3.6 V ≤ V_{DD} ≤ 5.5 V		Unit
			Min	Max	Min	Max	
Timing characteristics 7/ 12/ (see FIGURE 5)							
SCLK cycle time	t_1		40		33		ns
SCLK high time	t_2		16		13		ns
SCLK low time	t_3		16		13		ns
$\overline{SYNC}$ to SCLK falling edge setup time	t_4		16		13		ns
Data setup time	t_5		5		5		ns
Data hold time	t_6		4.5		4.5		ns
SCLK falling edge to $\overline{SYNC}$ rising edge	t_7		0		0		ns
Minimum $\overline{SYNC}$ high time	t_8		80		33		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 2.5 V to 5.5 V; V_{REF} = 2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; T_A = -55°C to +125°C; T_A = 25°C for typical (TYP) value; unless otherwise noted.

3/ DC specifications tested with the output unloaded.

4/ Linearity is tested using a reduced code range: Code 115 to Code 3981.

5/ Guaranteed monotonic by design over all code.

6/ Lower dead band exits only if offset error is negative.

7/ Guaranteed by design and characterization, not production test.

8/ For the amplifier output to reach its minimum voltage, offset error must be negative. For the amplifier output to reach its maximum voltage, V_{REF} = V_{DD} and offsets plus gain error must be positive.

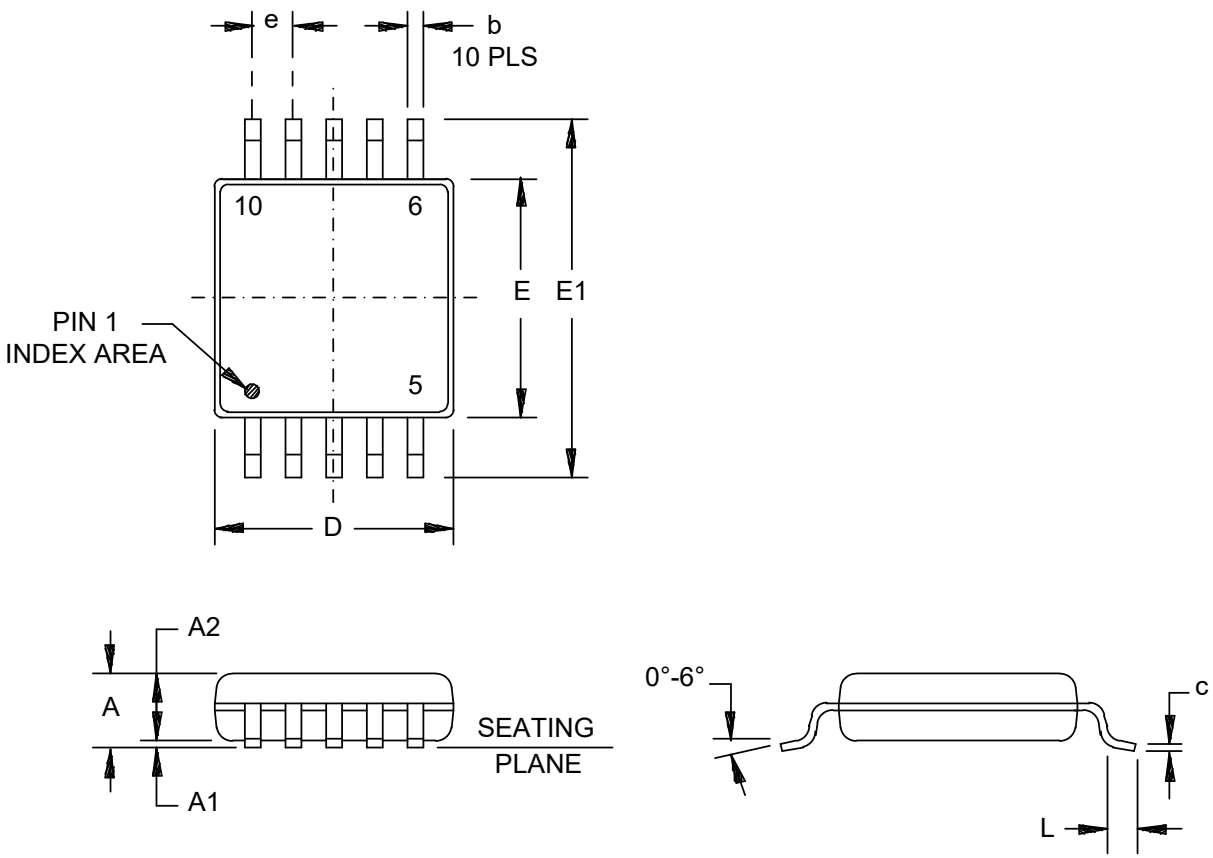
9/ Measurement of the minimum and maximum.

10/ V drive capability of the output amplifier.

11/ I_{DD} specification is valid for all DAC codes; interface inactive; load currents excluded.

12/ All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.10	D/E	2.90	3.10
A1	0.05	0.15	E1	4.65	5.15
A2	0.75	0.95	e	0.50 BSC	
b	0.15	0.30	L	0.40	0.70
c	0.13	0.23			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-15-AB3.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{DD}	10	$\overline{SYNC}$
2	$V_{OUT}A$	9	SCLK
3	$V_{OUT}B$	8	DIN
4	$V_{OUT}C$	7	GND
5	REFIN	6	$V_{OUT}D$

FIGURE 2. Terminal connections.

Terminal		Description
Number	Symbol	
1	V_{DD}	Power supply input. This part can be operated from 2.5 V to 5.5 V and the supply can be decoupled to GND
2	$V_{OUT}A$	Buffered analog output voltage from DAC A. The output amplifier has rail to rail operation.
3	$V_{OUT}B$	Buffered analog output voltage from DAC B. The output amplifier has rail to rail operation.
4	$V_{OUT}C$	Buffered analog output voltage from DAC C. The output amplifier has rail to rail operation.
5	REFIN	Reference input pin for all four DACs. It is an input range from 0.25 V to V_{DD}.
6	$V_{OUT}D$	Buffered analog output voltage from DAC D. The output amplifier has rail to rail operation.
7	GND	Ground reference point for all circuitry on the part.
8	DIN	Serial data input. This device has a 16 bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered down after each write cycle.
9	SCLK	Serial clock input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30 MHz. The SCLK input buffer is powered down after each write cycle.
10	$\overline{SYNC}$	Active low control input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edge of the foolowing 16 clocks. If $\overline{SYNC}$ is taken high before 16^{th} falling edge of SCLK. the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the device.

FIGURE 3. Terminal function.

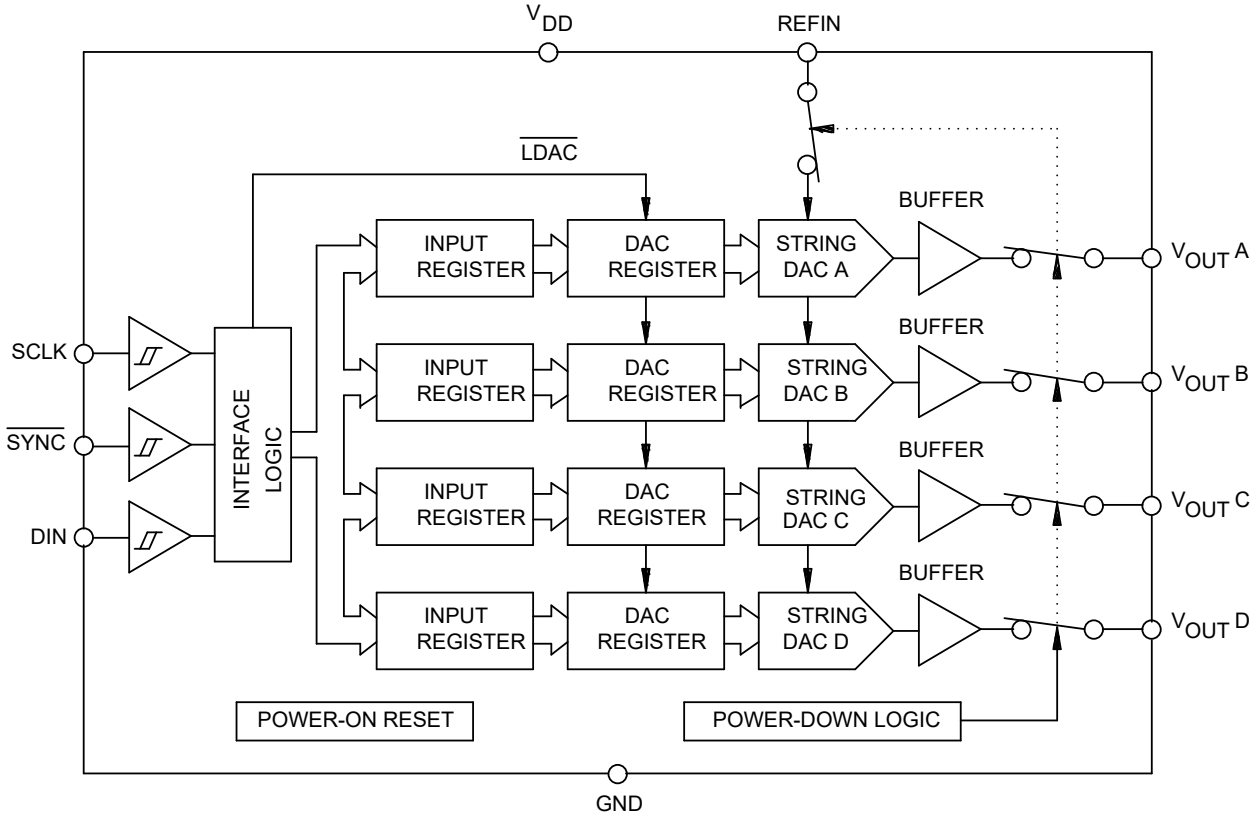


FIGURE 4. Functional block diagram.

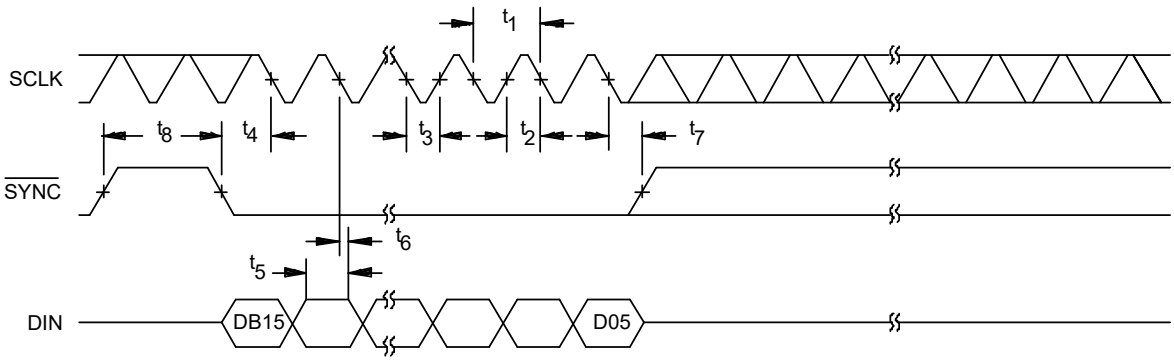


FIGURE 5. Serial interface timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12628-01XE	24355	AD5324SRMZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123