REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 13-01-23	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, LINEAR, 36 V, SINGLE SUPPLY, LOW POWER OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12627**
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AMSC N/A

5962-V092-12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 36 V, single supply, low power operational amplifier microcircuit, with an operating temperature range of -40°C to +150°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12627	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA170-EP	36 V, single supply, low power operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	5	See figure 1	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S) ..... ±20 V, +40 V (single supply)
Signal input terminals:
Voltage ..... $-V_S$ – 0.5 V to $+V_S$ + 0.5 V
Current ..... ±10 mA
Output short circuit ..... Continuous 2/
Junction temperature range (T_J) ..... +150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Electrostatic discharge (ESD) rating:
Human body model (HBM) ..... 4000 V
Charged device model (CDM) ..... 750 V

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (T_A) ..... -40°C to +150°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	226.8	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	80.3	°C/W
Thermal resistance, junction-to-board	θ_{JB}	42.9	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	3.2	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	42.5	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Short circuit to ground, one amplifier per package.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ V_S = +4 V to +36 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V_{OS}		+25°C	01		±1.8	mV
			-40°C to +150°C			±2.5	
Input offset voltage versus temperature	$\Delta V_{OS} / \Delta T$		-40°C to +150°C	01	±0.3 typical		µV/°C
Input offset voltage versus power supply	PSRR	V_S = +4 V to +36 V	-40°C to +150°C	01		±5	µV/V
Channel separation, dc	CS	At dc	+25°C	01	5 typical		µV/V
Input bias current							
Input bias current	I_B		+25°C	01		±15	pA
			-40°C to +150°C			±8	nA
Input offset current	I_{OS}		+25°C	01		±15	pA
			-40°C to +150°C			±8	nA
Noise							
Input voltage noise		f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		μV_{PP}
Input voltage noise density	en	f = 100 Hz	+25°C	01	22 typical		nV / $\sqrt{Hz}$
		f = 1 kHz			19 typical		
Input voltage range							
Common mode 3/ voltage range	V_{CM}		+25°C	01	$-V_S$ - 0.1	$+V_S$ - 2	V
Common mode rejection ratio	CMRR	V_S = ±2 V, $-V_S - 0.1\ V < V_{CM} < +V_S - 2\ V$	-40°C to +150°C	01	87		dB
		V_S = ±18 V, $-V_S - 0.1\ V < V_{CM} < +V_S - 2\ V$			100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = +4 V to +36 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input impedance							
Differential 4/			+25°C	01	100||3 typical		MΩ||pF
Common mode 4/			+25°C	01	6||3 typical		10^{12}Ω||pF
Open loop gain							
Open loop voltage gain	A_{OL}	V_S = +4 V to 36 V, $-V_S$ + 0.35 V < V_O < $+V_S$ – 0.35 V	-40°C to +150°C	01	107		dB
Frequency response							
Gain bandwidth product	GBP		+25°C	01	1.2 typical		MHz
Slew rate	SR	G = +1	+25°C	01	0.4 typical		V/μs
Settling time	t_S	To 0.1%, V_S = ±18 V, 10 V step, G = +1	+25°C	01	20 typical		μs
		To 0.01% (12 bit), V_S = ±18 V, 10 V step, G = +1			28 typical		
Overload recovery time		V_{IN} x Gain > V_S	+25°C	01	2 typical		μs
Total harmonic distortion + noise	THD+N	V_O = 3 VRMS, G = +1, f = 1 kHz	+25°C	01	0.0002 typical		%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ V_S = +4 V to +36 V, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail	V_O						
Positive rail		V_S = +4 V to +36 V, I_L = 0 mA	+25°C	01	10		mV
		V_S = +4 V to +36 V, I_L sourcing 1 mA			130		
Negative rail		V_S = +4 V to +36 V, I_L = 0 mA	+25°C			8	
		V_S = +4 V to +36 V, I_L sinking 1 mA				72	
Over temperature		V_S = 5 V, R_L = 10 kΩ	-40°C to +150°C		$-V_S$ + 0.03	$+V_S$ - 0.05	V
		$A_{OL} \geq$ 110 dB, R_L = 10 kΩ			$-V_S$ + 0.35	$+V_S$ - 0.35	
Short circuit current	I_{SC}	The limits are dependent on the negative or positive source	+25°C	01	+17/-20 typical		mA
Open loop output resistance	R_O	f = 1 MHz, I_O = 0 A	+25°C	01	900 typical		Ω
Power supply							
Specified voltage range	V_S		+25°C	01	+2.7	+36	V
Quiescent current per amplifier	I_Q	I_O = 0 mA	+25°C	01		145	μA
			-40°C to +150°C			160	
Temperature							
Specified range				01	-40	+125	°C
Operating range				01	-40	+150	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, T_A = +25°C, $V_{CM} = V_{OUT} = V_S / 2$, and R_L = 10 kΩ connected to $V_S / 2$.

3/ The input range can be extended beyond $+V_S$ – 2 V up to $+V_S$.

4/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

Case X

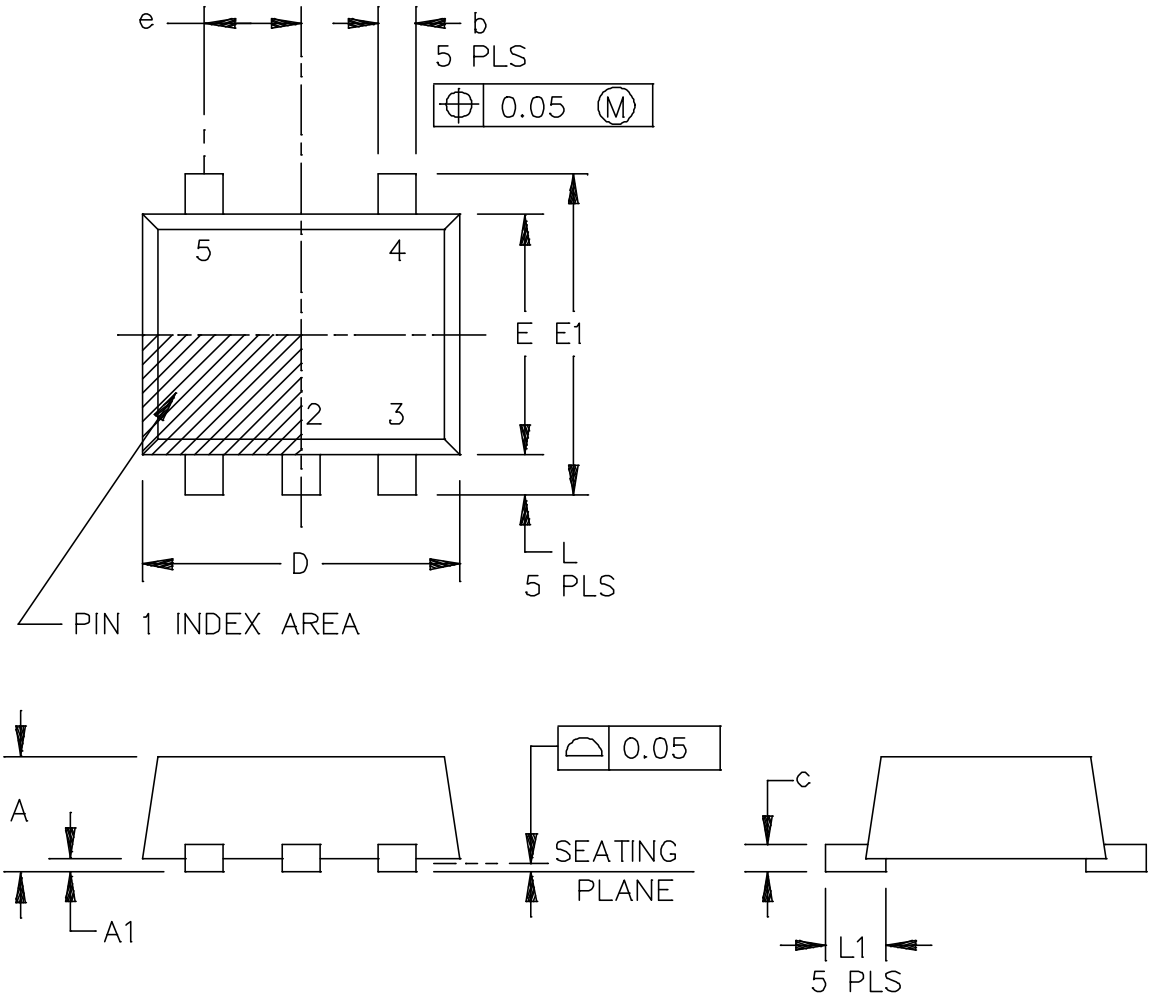

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12627
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.019	.023	0.50	0.60
A1	.000	.001	0.00	0.05
b	.005	.009	0.15	0.25
c	.003	.007	0.08	0.18
D	.059	.066	1.50	1.70
E	.043	.051	1.10	1.30
E1	.059	.066	1.50	1.70
e	.019 BSC		0.50 BSC	
L	.005	.010	0.13	0.27
L1	.007	.015	0.20	0.40

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensions D and E do not include mold flash, interlead flash, protrusion, or gate burrs.
   Mold flash, interlead flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per end or side.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	+INPUT
2	$-V_S$
3	-INPUT
4	OUTPUT
5	$+V_S$

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/ 3/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/12627-01XE	01295	SHN	OPA170ASDRLTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet , or use website www.ti.com.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493