

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current requirements. - ro	18-08-16	C. SAFFLE
B	Add typical limits to V <sub>OS</sub> , PSRR, I <sub>B</sub> , I <sub>OS</sub> , CMRR, A <sub>OL</sub> , and I <sub>Q</sub> tested parameters as specified under Table I. Update figure 1 case outline X JEDEC package to MO-293 variation UAAD-1. Make change to Top side marking by deleting SHN and replacing with DAQ as specified under paragraph 6.3. Update document to current requirements. - ro	24-07-17	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

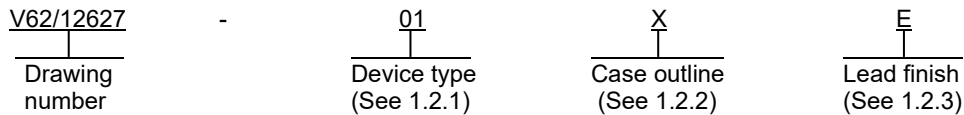
Revision Status of Sheets												
REV												
SHEET												
REV	B	B	B	B	B	B	B	B	B	B	B	
SHEET	1	2	3	4	5	6	7	8	9	10	11	

<b>PMIC N/A</b>  Original date of drawing  YY-MM-DD 13-01-23	<b>PREPARED BY</b> RICK OFFICER		<b>DLA LAND AND MARITIME</b> COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/landandmaritime">https://www.dla.mil/landandmaritime</a>	
	<b>CHECKED BY</b> RAJESH PITHADIA		<b>TITLE</b>	
	<b>APPROVED BY</b> CHARLES F. SAFFLE		MICROCIRCUIT, LINEAR, 36 V, SINGLE SUPPLY LOW POWER OPERATIONAL AMPLIFIER, MONOLITHIC SILICON	
	<b>SIZE</b> A	<b>CAGE CODE</b> 16236	<b>DWG NO.</b> V62/12627	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 36 V, single supply, low power operational amplifier microcircuit, with an operating temperature range of -40°C to +150°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type.

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	OPA170-EP	36 V, single supply, low power operational amplifier

1.2.2 Case outline. The case outline are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	MO-293-UAAD-1	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage (VS) ..... ±20 V, +40 V (single supply)  
 Signal input terminals:  
     Voltage ..... -VS – 0.5 V to +VS + 0.5 V  
     Current ..... ±10 mA  
 Output short circuit ..... Continuous 2/  
 Junction temperature range (TJ) ..... +150°C  
 Storage temperature range (TSTG) ..... -65°C to +150°C  
 Electrostatic discharge (ESD) rating:  
     Human body model (HBM) ..... 4000 V  
     Charged device model (CDM) ..... 750 V

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (TA) ..... -40°C to +150°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	$\theta_{JA}$	226.8	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	80.3	°C/W
Thermal resistance, junction-to-board	$\theta_{JB}$	42.9	°C/W
Characterization parameter, junction-to-top	$\psi_{JT}$	3.2	°C/W
Characterization parameter, junction-to-board	$\psi_{JB}$	42.5	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Short circuit to ground, one amplifier per package.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u> VS = +4 V to +36 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	VOS		+25°C	01		±1.8	mV
			-40°C to +150°C			±2.5	
					0.25 typical		
Input offset voltage versus temperature	$\Delta V_{OS} / \Delta T$		-40°C to +150°C	01	±0.3 typical		$\mu V/^{\circ}C$
Input offset voltage versus power supply	PSRR	VS = +4 V to +36 V	-40°C to +150°C	01		±5	$\mu V/V$
					1 typical		
Channel separation, dc	CS	At dc	+25°C	01	5 typical		$\mu V/V$
Input bias current							
Input bias current	IB		+25°C	01		±15	pA
			-40°C to +150°C			±8	
					±8 typical		
Input offset current	IOS		+25°C	01		±15	pA
					±4 typical		
			-40°C to +150°C			±8	nA
Noise							
Input voltage noise		f = 0.1 Hz to 10 Hz	+25°C	01	2 typical		$\mu V_{PP}$
Input voltage noise density	en	f = 100 Hz	+25°C	01	22 typical		$nV / \sqrt{Hz}$
		f = 1 kHz			19 typical		
Input voltage range							
Common mode <u>3/</u> voltage range	VCM		+25°C	01	-VS - 0.1	+VS - 2	V
Common mode rejection ratio	CMRR	VS = ±2 V, -VS - 0.1 V < VCM < +VS - 2 V	-40°C to +150°C	01	87		dB
		104 typical					
		100					
		VS = ±18 V, -VS - 0.1 V < VCM < +VS - 2 V			120 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> VS = +4 V to +36 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Input impedance							
Differential <u>4/</u>			+25°C	01	100  3 typical		MΩ  pF
Common mode <u>4/</u>			+25°C	01	6  3 typical		10 <sup>12</sup> Ω  pF
Open loop gain							
Open loop voltage gain	AOL	VS = +4 V to 36 V, -VS + 0.35 V < VO < +VS – 0.35 V	-40°C to +150°C	01	107		dB
					130 typical		
Frequency response							
Gain bandwidth product	GBP		+25°C	01	1.2 typical		MHz
Slew rate	SR	G = +1	+25°C	01	0.4 typical		V/μs
Settling time	ts	To 0.1%, VS = ±18 V, 10 V step, G = +1	+25°C	01	20 typical		μs
		To 0.01% (12 bit), VS = ±18 V, 10 V step, G = +1			28 typical		
Overload recovery time		VIN x Gain > VS	+25°C	01	2 typical		μs
Total harmonic distortion + noise	THD+N	VO = 3 VRMS, G = +1, f = 1 kHz	+25°C	01	0.0002 typical		%

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ VS = +4 V to +36 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output swing from rail	VO						
Positive rail		VS = +4 V to +36 V, IL = 0 mA	+25°C	01	10		mV
		VS = +4 V to +36 V, IL sourcing 1 mA			130		
Negative rail		VS = +4 V to +36 V, IL = 0 mA	+25°C			8	
		VS = +4 V to +36 V, IL sinking 1 mA				72	
Over temperature		VS = 5 V, RL = 10 kΩ	-40°C to +150°C		-VS + 0.03	+VS - 0.05	V
		AOL ≥ 110 dB, RL = 10 kΩ			-VS + 0.35	+VS - 0.35	
Short circuit current	ISC	The limits are dependent on the negative or positive source	+25°C	01	+17/-20 typical		mA
Open loop output resistance	RO	f = 1 MHz, IO = 0 A	+25°C	01	900 typical		Ω
Power supply							
Specified voltage range	VS		+25°C	01	+2.7	+36	V
Quiescent current per amplifier	IQ	IO = 0 mA	+25°C	01		145	μA
			-40°C to +150°C		110 typical	160	
Temperature							
Specified range				01	-40	+125	°C
Operating range				01	-40	+150	°C

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, TA = +25°C, VCM = VOUT = VS / 2, and RL = 10 kΩ connected to VS / 2.

3/ The input range can be extended beyond +VS – 2 V up to +VS.

4/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

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Case outline X

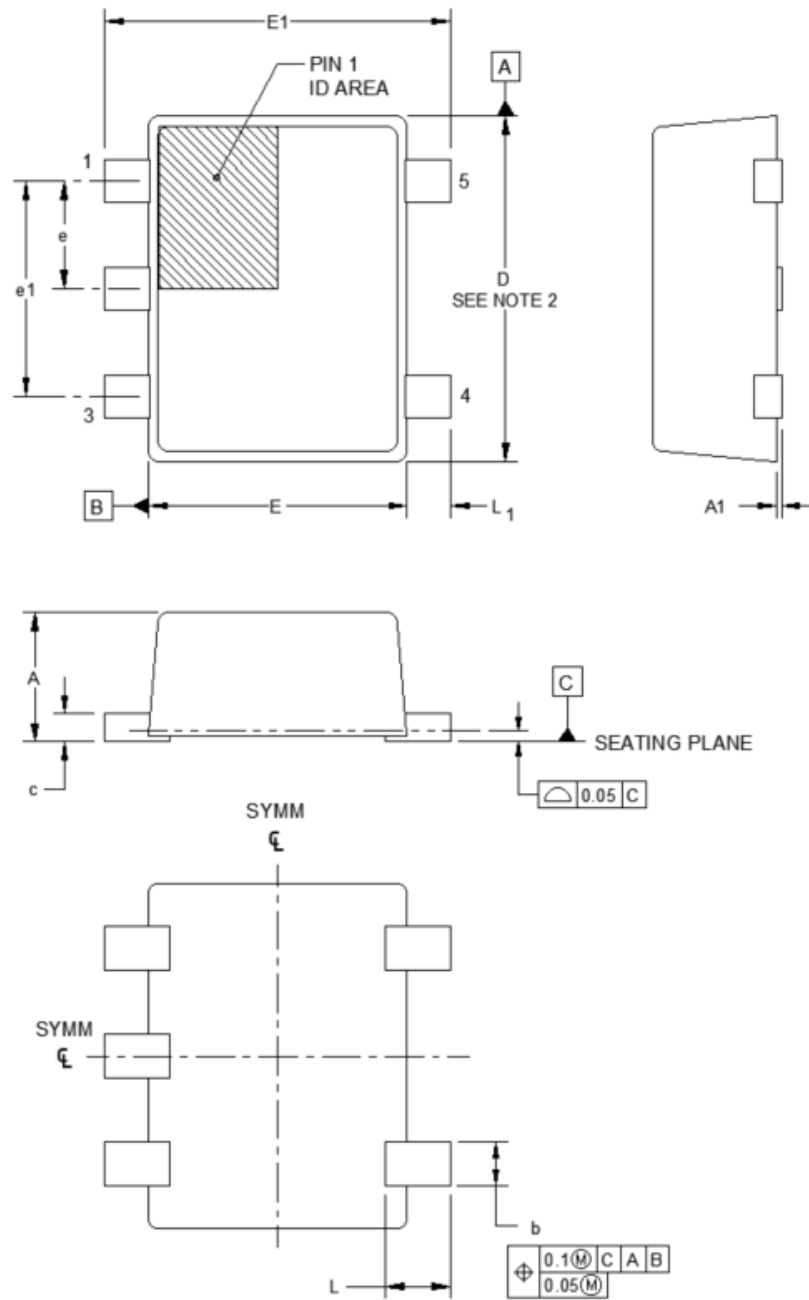


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.024	---	0.6
A1	.000 TYP	.002 TYP	0.00 TYP	0.05 TYP
b	.006	.011	0.15	0.27
c	.003	.007	0.08	0.18
D	.059	.067	1.50	1.70
E	.043	.051	1.10	1.30
E1	.059	.067	1.50	1.70
e	.020 BSC		0.5 BSC	
e1	.039 BSC		1.0 BSC	
L	.008	.016	0.20	0.40
L1	.004	.012	0.10	0.30

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension D length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
3. Falls within reference to JEDEC MO-293 variation UAAD-1.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	+INPUT
2	-Vs
3	-INPUT
4	OUTPUT
5	+Vs

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u> <u>2/</u> <u>3/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/12627-01XE	01295	DAQ	OPA170ASDRLTEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer’s data sheet.
- 3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
12500 TI Blvd.  
Dallas, TX 75243

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