REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|---|---|---|---|
| A | Update boilerplate to current MIL-PRF-38535 requirements. - PHN | 18-05-22 | Thomas M. Hess |
| B | Update boilerplate paragraphs to current VID description requirements. - PHN | 23-10-18 | Muhammad A. Akbar |
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Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | | | |
| REV | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B | |
| SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | |

**PMIC N/A**

Original date of drawing

YY MM DD

12-12-10

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**TITLE**
MICROCIRCUIT, DIGITAL, MIXED SIGNAL MICROCONTROLLER, MONOLITHIC SILICON

| SIZE | CAGE CODE | DWG NO. |
|---|---|---|
| A | 16236 | V62/12623 |
| REV B | | PAGE 1 OF 21 |

AMSC N/A

5962-V169-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -40ºC to +85ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/12623 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (see 1.2.1) | Case outline (see 1.2.2) | Lead finish (see 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | MSP430G2302-EP | Mixed signal microcontroller |

1.2.2 Case outline(s). The case outlines are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 14 | JEDEC MO-153 | Plastic small outline |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Voltage applied at $V_{CC}$ to $V_{SS}$ ..... -0.3 V to 4.1 V
Voltage applied to any pin ..... -0.3 V to $V_{CC}$ +0.3 V 2/
Diode current at any device terminal ..... ±2 mA
Storage temperature: 3/
Unprogrammed device ..... -55°C to 150°C
Programmed device ..... -55°C to 150°C

1.4 Thermal characteristics.

Thermal information

| | Case outline X | Units |
|---|---|---|
| Junction to ambient thermal resistance, $\theta_{JA}$ 4/ | 98.7 | °C/W |
| Junction to case (top) thermal resistance, $\theta_{JCtop}$ 5/ | 26.8 | °C/W |
| Junction to board thermal resistance, $\theta_{JB}$ 6/ | 41.2 | °C/W |
| Junction to top characterization parameter, $\Psi_{JT}$ 7/ | 1.1 | °C/W |
| Junction to board characterization parameter, $\Psi_{JB}$ 8/ | 40.5 | °C/W |
| Junction to case (bottom) thermal resistance, $\theta_{JCbot}$ 9/ | N/A | °C/W |

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values referenced to $V_{SS}$. The JTAG fuse blow voltage, $V_{FB}$ is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse..
3/ Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
4/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-k-board, as specified in JESD51-7, in an environment described in JESD51-2a.
5/ The junction to case (top) thermal resistance is obtanied by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
6/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
7/ The junction to top characterization parameter, $\Psi_{JT}$, estimates the junction teperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
8/ The junction to board characterization parameter, $\Psi_{JB}$, estimates the junction teperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
9/ The junction to case (bottom) thermal resistance is obtanied by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

1.5 Recommended operating conditions.

Supply voltage, ($V_{CC}$):
During program execution ..... 1.8 V to 3.6 V
During flash program/erase ..... 2.2 V to 3.6 V
Supply voltage, ($V_{SS}$) ..... 0 V
Operating free air temperature, ($T_A$) ..... -40°C to 85°C
Processor frequency (Maximum MCLK frequency) 10/ 11/
$V_{CC}$ = 1.8 V, Duty cycle = 50% ±10% ..... dc to 6 MHz
$V_{CC}$ = 2.7 V, Duty cycle = 50% ±10% ..... dc to 12 MHz
$V_{CC}$ = 3.3 V, Duty cycle = 50% ±10% ..... dc to 16 MHz

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

| | | |
|---|---|---|
| JEP95 | – | Registered and Standard Outlines for Semiconductor Devices |
| JESD51-2 | – | Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air) |
| JESD51-7 | – | High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages |
| JESD51-8 | – | Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board |
| J-STD-020 | – | Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices. |

(Copies of these documents are available online at https://www.jedec.org.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at https://www.ansi.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, 1.5 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

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10/ The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
11/ Modules might have different maximum input clock specification. See the specification from the manufacturer data sheet.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Safe operating area. The safe operating area shall be as shown in figure 5.

3.5.6 POR/Brownout Reset (BOR) vs Supply voltage. The POR/Brownout Reset (BOR) vs Supply voltage shall be as shown in figure 6.

3.5.7 $V_{CC(drop)}$ level with a Square voltage drop to generate a POR/Brownout signal. The $V_{CC(drop)}$ level with a Square voltage drop to generate a POR/Brownout signal shall be as shown in figure 7.

3.5.8 $V_{CC(drop)}$ level with a Triangle voltage drop to generate a POR/Brownout signal. The $V_{CC(drop)}$ level with a Triangle voltage drop to generate a POR/Brownout signal shall be as shown in figure 8.

3.5.9 DCO wake-up time from LPM3/4 vs DCO frequency. The DCO wake-up time from LPM3/4 vs DCO frequency waveforms shall be as shown in figure 9.

3.5.10 USI low level output voltage vs output current. The USI low level output voltage vs output current shall be as shown in figure 10.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions<br>2/ 3/ 4/ | $T_A$ | $V_{CC}$ | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| **Active mode supply current into $V_{CC}$ excluding external current.** | | | | | | | |
| Active mode (AM) current (1 MHz) | $I_{AM, 1MHz}$ | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz,<br>$f_{ACLK}$ = 32768 Hz,<br>Program executes in flash,<br>BCSCTL1 = CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>CPUOFF = 0, SCG0 = 0<br>SCG1 = 0, OSCOOFF = 0 | | 2.2 V | 220 TYP | | µA |
| | | | | 3 V | | 400 | µA |
| **Low power mode Supply current (into $V_{CC}$) Excluding external current** | | | | | | | |
| Low power mode 0 (LPM0) current<br>5/ | $I_{LPM0, 1MHz}$ | $f_{MCLK}$ = 0 MHz,<br>$f_{SMCLK} = f_{CDO}$ = 1 MHz,<br>$f_{ACLK}$ = 32,768 Hz,<br>BCSCTL1 = CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>CPUOFF = 1, SCG0 = 0,<br>SCG1 = 0, OSCOFF = 0 | 25°C | 2.2 V | 55 TYP | | µA |
| Low power mode 2 (LPM2) current<br>6/ | $I_{LPM2}$ | $f_{MCLK} = f_{SMCLK}$ = 0 MHz,<br>$f_{CDO}$ = 1 MHz,<br>$f_{ACLK}$ = 32,768 Hz,<br>BCSCTL1 = CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>CPUOFF = 1, SCG0 = 0,<br>SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | 22 TYP | | µA |
| Low power mode 3 (LPM3) current 6/ | $I_{LPM3, LFXT1}$ | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz,<br>$f_{ACLK}$ = 32768 Hz,<br>CPUOFF = 1, SCG0 = 1,<br>SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 1.0 | µA |
| Low power mode 3 (LPM3) current 6/ | $I_{LPM3, VLO}$ | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz,<br>$f_{ACLK}$ = from internal LF oscillator (VLO),<br>CPUOFF = 1, SCG0 = 1,<br>SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.7 | µA |
| Low power mode 4 (LPM4) current<br>7/ | $I_{LPM4}$ | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz,<br>$f_{ACLK}$ = 0 Hz,<br>CPUOFF = 1, SCG0 = 1,<br>SCG1 = 1, OSCOFF = 1 | 25°C | 2.2 V | | 0.5 | µA |
| | | | 85°C | | | 1.5 | µA |

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions<br>2/ 3/ 4/ | $V_{CC}$ | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Schmitt Trigger inputs (Port Px)** 8/ | | | | | | |
| Positive going input threshold voltage | $V_{IT+}$ | | | 0.45 $V_{CC}$ | 0.75 $V_{CC}$ | V |
| | | | 3 V | 1.35 | 2.25 | V |
| Negative going input threshold voltage | $V_{IT-}$ | | | 0.25 $V_{CC}$ | 0.55 $V_{CC}$ | V |
| | | | 3 V | 0.75 | 1.65 | V |
| Input voltage hysteresis ($V_{IT+}$ - $V_{IT-}$) | $V_{hys}$ | | 3 V | 0.3 | 1.0 | V |
| Pullup/pulldown resistor | $R_{Pull}$ | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | 3 V | 20 | 50 | kΩ |
| Input capacitance | $C_I$ | $V_{IN} = V_{SS}$ or $V_{CC}$ | | 5 TYP | | pF |
| **Leakage current (Port Px)** | | | | | | |
| High impedance leakage current | $I_{lkg(Px.y)}$ | 9/ 10/ | 3 V | | ±50 | nA |
| **Outputs (Port Px)** | | | | | | |
| High level output voltage | $V_{OH}$ | $I_{(OHmax)}$ = -6 mA 11/ | 3 V | $V_{CC}$ - 0.3 | | V |
| Low level output voltage | $V_{OL}$ | $I_{(OLmax)}$ = 6 mA 11/ | 3 V | $V_{SS}$ + 0.3 | | V |
| **Output frequency (Port Px)** | | | | | | |
| Port output frequency (with load) | $f_{Px.y}$ | Px.y, $C_L$ = 20 pF, $R_L$ = 1 kΩ 12/ 13/ | 3 V | 12 TYP | | MHz |
| Clock output frequency | $f_{Port°CLK}$ | Px.y, $C_L$ = 20 pF 13/ | 3 V | 16 TYP | | MHz |
| **Pin Oscillator frequency – Ports Px** | | | | | | |
| Port output oscillation frequency | $fo_{P1.x}$ | P1.y, $C_L$ = 10 pF, $R_L$ = 100 kΩ 14/ 15/ | 3 V | 1400 TYP | | kHz |
| | | P1.y, $C_L$ = 20 pF, $R_L$ = 100 kΩ 14/ 15/ | | 900 TYP | | kHz |
| Port output oscillation frequency | $fo_{P2.x}$ | P2.0 to P2.5, $C_L$ = 10 pF, $R_L$ = 100 kΩ 14/ 15/ | 3 V | 1800 TYP | | kHz |
| | | P2.0 to P2.5, $C_L$ = 20 pF, $R_L$ = 100 kΩ 14/ 15/ | | 1000 TYP | | kHz |
| Port output oscillation frequency | $fo_{P2.6/7}$ | P2.6 and P2.7, $C_L$ = 20 pF, $R_L$ = 100 kΩ 14/ 15/ | 3 V | 700 TYP | | kHz |
| **POR/Brownout Reset (BOR)** 16/ | | | | | | |
| See figure 10 | $V_{CC(start)}$ | $dV_{CC}/dt \le 3$ V/s | | 0.7 x $V_{(B\_IT-)}$ TYP | | V |
| See figure 10 through figure 12 | $V_{(B\_IT-)}$ | $dV_{CC}/dt \le 3$ V/s | | 1.40 | TYP | V |
| See figure 10 | $V_{hys(B\_IT-)}$ | $dV_{CC}/dt \le 3$ V/s | | 140 | TYP | mV |
| See figure 10 | $t_{d(BOR)}$ | | | | 2000 | µs |
| Pulse length needed at $\overline{RST}$/NMI pin to accept reset internally | $t_{(reset)}$ | | 2.2 V | 2 | | µs |

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions 2/ 3/ 4/ | $V_{CC}$ | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Schmitt Trigger input** | | | | | | |
| Supply voltage | $V_{CC}$ | RSELx < 14 | | 1.8 | 3.6 | V |
| | | RSELx = 14 | | 2.2 | 3.6 | V |
| | | RSELx = 15 | | 3.0 | 3.6 | V |
| DCO frequency (0, 0) | $f_{DCO(0,0)}$ | RSELx = 0, DCOx = 0, MDDx = 0 | 3 V | 0.06 | 0.14 | MHz |
| DCO frequency (0, 3) | $f_{DCO(0,3)}$ | RSELx = 0, DCOx = 3, MDDx = 0 | 3 V | 0.07 | 0.17 | MHz |
| DCO frequency (1, 3) | $f_{DCO(1,3)}$ | RSELx = 1, DCOx = 3, MDDx = 0 | 3 V | 0.15 TYP | | MHz |
| DCO frequency (2, 3) | $f_{DCO(2,3)}$ | RSELx = 2, DCOx = 3, MDDx = 0 | 3 V | 0.21 TYP | | MHz |
| DCO frequency (3, 3) | $f_{DCO(3,3)}$ | RSELx = 3, DCOx = 3, MDDx = 0 | 3 V | 0.30 TYP | | MHz |
| DCO frequency (4, 3) | $f_{DCO(4,3)}$ | RSELx = 4, DCOx = 3, MDDx = 0 | 3 V | 0.41 TYP | | MHz |
| DCO frequency (5, 3) | $f_{DCO(5,3)}$ | RSELx = 5, DCOx = 3, MDDx = 0 | 3 V | 0.58 TYP | | MHz |
| DCO frequency (6, 3) | $f_{DCO(6,3)}$ | RSELx = 6, DCOx = 3, MDDx = 0 | 3 V | 0.54 | 1.06 | MHz |
| DCO frequency (7, 3) | $f_{DCO(7,3)}$ | RSELx = 7, DCOx = 3, MDDx = 0 | 3 V | 0.80 | 1.50 | MHz |
| DCO frequency (8, 3) | $f_{DCO(8,3)}$ | RSELx = 8, DCOx = 3, MDDx = 0 | 3 V | 1.6 TYP | | MHz |
| DCO frequency (9, 3) | $f_{DCO(9,3)}$ | RSELx = 9, DCOx = 3, MDDx = 0 | 3 V | 2.3 TYP | | MHz |
| DCO frequency (10, 3) | $f_{DCO(10,3)}$ | RSELx = 10, DCOx = 3, MDDx = 0 | 3 V | 3.4 TYP | | MHz |
| DCO frequency (11, 3) | $f_{DCO(11,3)}$ | RSELx = 11, DCOx = 3, MDDx = 0 | 3 V | 4.25 TYP | | MHz |
| DCO frequency (12, 3) | $f_{DCO(12,3)}$ | RSELx = 12, DCOx = 3, MDDx = 0 | 3 V | 4.3 | 7.30 | MHz |
| DCO frequency (13, 3) | $f_{DCO(13,3)}$ | RSELx = 13, DCOx = 3, MDDx = 0 | 3 V | 6.00 | 9.60 | MHz |
| DCO frequency (14, 3) | $f_{DCO(14,3)}$ | RSELx = 14, DCOx = 3, MDDx = 0 | 3 V | 8.6 | 13.9 | MHz |
| DCO frequency (15, 3) | $f_{DCO(15,3)}$ | RSELx = 15, DCOx = 3, MDDx = 0 | 3 V | 12.0 | 18.5 | MHz |
| DCO frequency (15, 7) | $f_{DCO(15,7)}$ | RSELx = 15, DCOx = 7, MDDx = 0 | 3 V | 16.0 | 26.0 | MHz |
| Frequency step between range RSEL and RSEL + 1 | $S_{RESL}$ | $S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$ | 3 V | 1.35 TYP | | ratio |
| Frequency step between tap DCO and DCO + 1 | $S_{DCO}$ | $S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$ | 3 V | 1.08 TYP | | ratio |
| Duty cycle | | Measured at SMCLK output | 3 V | 50 TYP | | % |

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Conditions 2/ 3/ 4/ | $T_A$ | $V_{CC}$ | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Calibrated DCO frequencies – Tolerance** | | | | | | |
| 1 MHz tolerance over temperature 17/ | BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | 3 | % |
| 1 MHz tolerance over $V_{CC}$ | BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V | 30°C | 1.8 V to 3.6 V | -3 | 3 | % |
| 1 MHz tolerance overall | BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V | -40°C to 85°C | 1.8 V to 3.6 V | -6 | 6 | % |
| 8 MHz tolerance over temperature 17/ | BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | 3 | % |
| 8 MHz tolerance over $V_{CC}$ | BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, calibrated at 30°C and 3 V | 30°C | 2.2 V to 3.6 V | -3 | 3 | % |
| 8 MHz tolerance overall | BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, calibrated at 30°C and 3 V | -40°C to 85°C | 2.2 V to 3.6 V | -6 | 6 | % |
| 12 MHz tolerance over temperature 17/ | BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | 3 | % |
| 12 MHz tolerance over $V_{CC}$ | BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, calibrated at 30°C and 3 V | 30°C | 2.7 V to 3.6 V | -3 | 3 | % |
| 12 MHz tolerance overall | BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, calibrated at 30°C and 3 V | -40°C to 85°C | 2.7 V to 3.6 V | -6 | 6 | % |
| 16 MHz tolerance over temperature 17/ | BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, calibrated at 30°C and 3 V | 0°C to 85°C | 3.3 V | -3 | 3 | % |
| 16 MHz tolerance over $V_{CC}$ | BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, calibrated at 30°C and 3 V | 30°C | 3.3 V to 3.6 V | -3 | 3 | % |
| 16 MHz tolerance overall | BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, calibrated at 30°C and 3 V | -40°C to 85°C | 3.3 V to 3.6 V | -6 | 6 | % |

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions 2/ 3/ 4/ | $V_{CC}$ | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Wake up from Lower Power Models (LPM3/4)** | | | | | | |
| DCO clock wake up time from LPM3/4 18/ | $t_{DCO,LPM3/4}$ | BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, | 3 V | 1.5 TYP | | µs |
| CPU wake up time from LPM3/4 19/ | $t_{CPU,LPM3/4}$ | | | 1 / $f_{MCLK}$ + $t_{Clock,LPM3/4}$ TYP | | |
| **Crystal oscillator, XT1, low frequency mode** 20/ | | | | | | |
| LFXT1 oscillator crystal frequency, LF mode 0, 1 | $f_{LFXT1,LF}$ | XTS = 0, LFXT1Sx = 0 or 1 | 1.8 V to 3.6 V | 32768 TYP | | Hz |
| LFXT1 oscillator logic level square wave input frequency, LF mode | $f_{LFXT1,LF,logic}$ | XTS = 0, XCAPx = 0, LFXT1Sx = 3 | 1.8 V to 3.6 V | 10000 | 50000 | Hz |
| Oscillation allowance for LF crystals | $OA_{LF}$ | XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | 500 TYP | | kΩ |
| | | XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | 200 TYP | | kΩ |
| Integrated effective load capacitance, LF mode 21/ | $C_{L,eff}$ | XTS = 0, XCAPx = 0 | | 1 TYP | | pF |
| | | XTS = 0, XCAPx = 1 | | 5.5 TYP | | pF |
| | | XTS = 0, XCAPx = 2 | | 8.5 TYP | | pF |
| | | XTS = 0, XCAPx = 3 | | 11 TYP | | pF |
| Duty cycle, LF mode | | XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz | 2.2 V | 30 | 70 | % |
| Oscillator fault frequency, LF mode 22/ | $f_{Fault,LF}$ | XTS = 0, XCAPx = 0, LFXT1Sx = 3 23/ | 2.2 V | 10 | 10000 | Hz |
| **Internal Very Low power Low frequency Oscillator (VLO)** | | | | | | |
| VLO frequency | $f_{VLO}$ | -40°C ≤ $T_A$ ≤ 85°C | 3 V | 4 | 20 | kHz |
| VLO frequency temperature drift 30/ | $df_{VLO}/d_T$ | -40°C ≤ $T_A$ ≤ 85°C | 3 V | 0.5 | TYP | %/°C |
| VLO frequency supply voltage drift | $df_{VLO}/dV_{CC}$ | $T_A$ = 25°C | 1.8 V to 3.6 V | 4 | TYP | %/V |
| **Timer_A** | | | | | | |
| Timer_A input clock frequency | $f_{TA}$ | SMCLK, Duty cycle = 50% ±10% | | $f_{SYSTEM}$ | | MHz |
| Timer_A capture timing | $f_{TA,cap}$ | TA0, TA1 | 3 V | 20 | | ns |
| **USI, Universal Serial Interface** | | | | | | |
| USI clock frequency | $f_{USI}$ | External: SCLK, Duty cycle = 50% ±10% | | $f_{SYSTEM}$ | | MHz |
| Serial clock frequency, slave mode | $f_{(SCLK)}$ | SPI slve mode | 3 V | | 6 | MHz |
| Low level output voltage on SDA and SCL | $V_{OL,I2C}$ | USI module in $I^2C$ mode, $I_{(OLmax)}$ = 1.5 mA | 3 V | $V_{SS}$ | $V_{SS}$ + 0.4 | V |

See footnote at end of table.

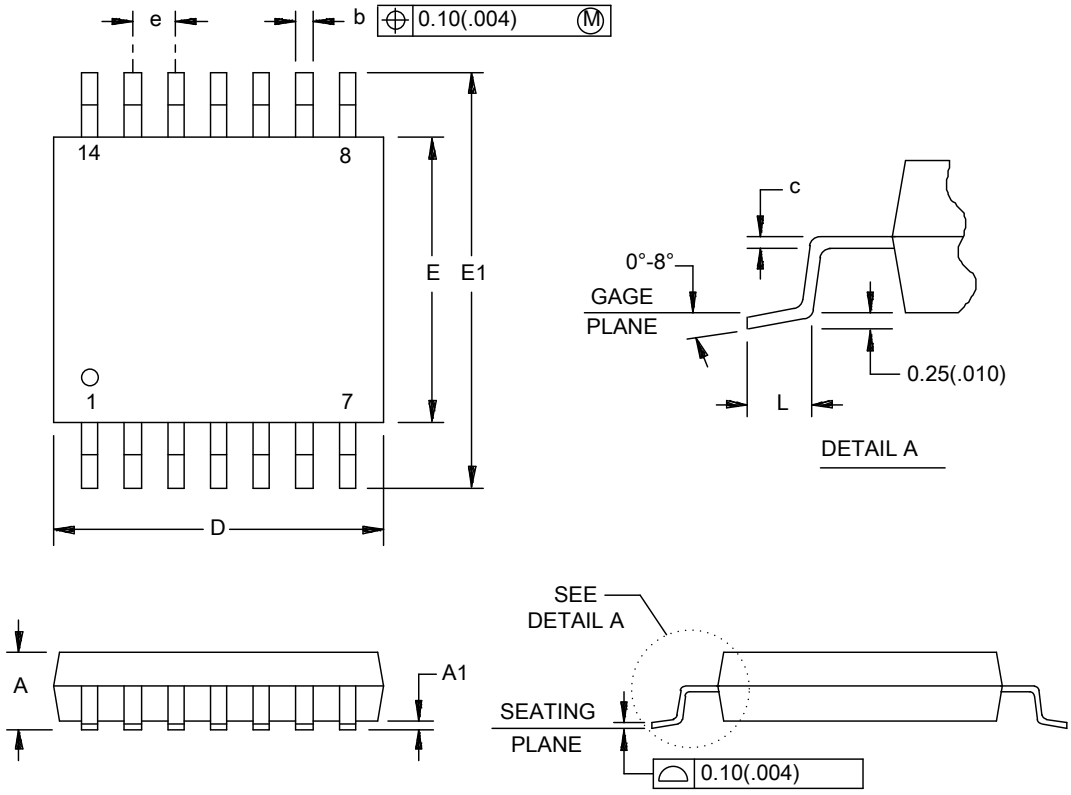
TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Conditions 2/ 3/ 4/ | $V_{CC}$ | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Flash memory** | | | | | | |
| Program and erase supply voltage | $V_{CC(PGM/ERASE)}$ | | | 2.2 | 3.6 | V |
| Flash timing generator frequency | $f_{FTG}$ | | | 257 | 476 | kHz |
| Supply current from $V_{CC}$ during program | $I_{PGM}$ | | 2.2 V/3.6 V | | 5 | mA |
| Supply current from $V_{CC}$ during erase | $I_{ERASE}$ | | 2.2 V/3.6 V | | 7 | mA |
| Cumulative program time 24/ | $t_{CPT}$ | | 2.2 V/3.6 V | | 10 | ms |
| Cumulative mass erase time | $t_{CMErase}$ | | 2.2 V/3.6 V | 20 | | ms |
| Program/erase endurance | | | | $10^4$ | | cycles |
| Data retention duration | $t_{Retention}$ | $T_J$ = 25°C | | 100 | | years |
| Word or byte program time | $t_{Word}$ | 25/ | | 30 | TYP | $t_{FTG}$ |
| Block program time for first byte or word | $t_{Block, 0}$ | 25/ | | 25 | TYP | $t_{FTG}$ |
| Block program time for each additional byte or word | $t_{Block, 1-63}$ | 25/ | | 18 | TYP | $t_{FTG}$ |
| Block program end sequence wait time | $t_{Block, End}$ | 25/ | | 6 | TYP | $t_{FTG}$ |
| Mass erase time | $t_{Mass\ Erase}$ | 25/ | | 10593 | TYP | $t_{FTG}$ |
| Segment erase time | $t_{Seg\ Erase}$ | 25/ | | 4819 | TYP | $t_{FTG}$ |
| **RAM** | | | | | | |
| RAM retention supply voltage 26/ | $V_{(RAMh)}$ | CPU halted | | 1.6 | | V |
| **JTAG and Spy-Bi-Wire Interface** | | | | | | |
| Spy-Bi-Wire input frequency | $f_{SBW}$ | | 2.2 V | 0 | 20 | MHz |
| Spy-Bi-Wire low clock pulse length | $t_{SBW,Low}$ | | 2.2 V | 0.025 | 15 | µs |
| Spy-Bi-Wire enable time (Test high to acceptance of first clock edge 27/) | $t_{SBW,En}$ | | 2.2 V | | 1 | µs |
| Spy-Bi-Wire return to normal operation time | $t_{SBW,Ret}$ | | 2.2 V | 15 | 100 | µs |
| TCK input frequency 28/ | $f_{TCK}$ | | 2.2 V | 0 | 5 | MHz |
| Internal pulldown resistance on TEST | $R_{Internal}$ | | 2.2 V | 25 | 90 | kΩ |
| **JTAG fuse** 29/ | | | | | | |
| Supply voltage during fuse blow condition | $V_{CC(FB)}$ | $T_A$ = 25°C | | 2.5 | | V |
| Voltage level on TEST for fuse blow | $V_{FB}$ | | | 6 | 7 | V |
| Supply current into TEST during fuse blow | $I_{FB}$ | | | | 100 | mA |
| Time to blow fuse | $t_{FB}$ | | | | 1 | ms |

See footnote at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended operating free air temperature range (unless otherwise noted).
3/ All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
4/ The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen closely match the required 9 pF.
5/ Current for brownout and WDT clocked by SMCLK included.
6/ Current for brownout and WDT clocked by ACLK included.
7/ Current for brownout included.
8/ An external signal sets interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.
9/ The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
10/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
11/ The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
12/ A resistive divider with 2 x 0.5 kΩ resistors between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
13/ The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.
14/ A resistive divider with two 100 kΩ resistors between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
15/ The output voltage oscillator with a typical amplitude of 700 mV at the specified toggle frequency.
16/ The current consumption of the brownout module is already included in the ICC current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
17/ This is the frequency change from the measured frequency at 30°C over temperature.
18/ The DCO clock wake up time is measured from the edge of an external wake up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
19/ Parameter applicable only if DCOCLK is used for MCLK.
20/ To improve EMI on the XT1 oscillator, the following guide lines should be observed.
   a) Keep the trace between the device and the crystal as short as possible.
   b) Design a good ground plane around the oscillator pins.
   c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
21/ Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct set up, the effective load capacitance should always match the specification of the used crystal.
22/ Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
23/ Measured with logic level input frequency but also applies to operation with crystals.
24/ The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
25/ These values are hardwired into the Flash controller's state machine ($t_{FTG} = 1/f_{FTG}$).
26/ This parameter defines the minimum supply voltage $V_{CC}$ when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.
27/ Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
28/ $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.
29/ Once the fuse is blown, no further access to the JATG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.
30/ Ensured by design on specified temperature.

Case X




| Dimensions | | | | | |
|---|---|---|---|---|---|
| Symbol | Millimeters | | Symbol | Millim eters | |
| | Min | Max | | Min | Max |
| A | | 1.20 | E | 4.30 | 4.50 |
| A1 | 0.05 | 0.15 | E1 | 6.20 | 6.60 |
| b | 0.19 | 0.30 | e | 0.65 BSC | |
| c | 0.15 NOM | | L | 0.50 | 0.70 |
| D | 4.90 | 5.10 | | | |

NOTES:
1. All linear dimensions are in millimeters (inches).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 0.15 each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
5. Fall within JEDEC MO-153

FIGURE 1. Case outline.

Case Outline X

| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
|---|---|---|---|
| 1 | DVCC | 8 | P1.6/TA0.1/SDO/SCL/A6/TDI/TCLK |
| 2 | P1.0/TA0CLK/ACLK/A0 | 9 | P1.7/SDI/SDA/A7/TDO/TDI |
| 3 | P1.1/TA0.0/A1 | 10 | $\overline{\text{RST}}$/NMI/SBWTDIO |
| 4 | P1.2/TA0.1/A2 | 11 | TEST/SBWTCK |
| 5 | P1.3/ADC10CLK/A3/VREF-/VEREF- | 12 | XOUT/P2.7 |
| 6 | P1.4/TA0.2/SMCLK/A4/VREF+/VEREF+/TCK | 13 | XIN/P2.6/TA0.1 |
| 7 | P1.5/TA0.0/SCLK/A5/TMS | 14 | DVSS |

NOTES:
1. The pulldown resistors of port pins P2.0, P2.1, P2.2, P2.3, P2.4, and P2.5 should be enabled by setting P2REN.x = 1..

FIGURE 2. Terminal connections.

Case outline X

| Terminal | | I/O | Description |
|---|---|---|---|
| Name | Number | | |
| P1.0/<br>TA0CLK/<br>ACLK<br>A0 | 2 | I/O | General purpose digital I/O pin<br>Timer0_A, clock signal TACLK input<br>ACLK signal output<br>ADC10 analog input A0 1/ |
| P1.1/<br>TA0.0/<br>A1 | 3 | I/O | General purpose digital I/O pin<br>Timer0_A, capture:CCI0A input, compare: Out0 output<br>ADC10 analog input A1 1/ |
| P1.2/<br>TA0.1/<br>A2 | 4 | I/O | General purpose digital I/O pin<br>Timer0_A, capture:CCI1A input, compare: Out1 output<br>ADC10 analog input A2 1/ |
| P1.3/<br>ADC10CLK/<br>A3/<br>VREF-/VEREF- | 5 | I/O | General purpose digital I/O pin<br>ADC10, conversion clock output 1/<br>ADC10 analog input A3 1/<br>ADC10 negative reference voltage 1/ |
| P1.4/<br>TA0.2/<br>SMCLK/<br>A4/<br>VREF+/VEREF+/<br>TCK | 6 | I/O | General purpose digital I/O pin<br>Timer0_A, capture:CCI2A input, compare: Out2 output<br>SMCLK signal output<br>ADC10 analog input A4 1/<br>ADC10 positive reference voltage 1/<br>JTAG test clock, input terminal for device programming and test |
| P1.5/<br>TA0.0/<br>A5/<br>SCLK/<br>TMS | 7 | I/O | General purpose digital I/O pin<br>Timer0_A, compare: Out0 output<br>ADC10 analog input A5<br>USI: clock input in I2C mode; clock input/output in SPI mode<br>JTAG test data input or test clock input during programming and test |
| P1.6/<br>TA0.1/<br>A6/<br>SDO/<br>SCL/<br>TDI/TCLK | 8 | I/O | General purpose digital I/O pin<br>Timer0_A, capture: CCI1A input, compare Out1 output<br>ADC10 analog input A6<br>USI: Data output in SPI mode<br>USI: I2C clock in I2C mode<br>JTAG test data input or test clock input during programming and test |
| P1.7/<br>A7/<br>SDI/<br>SDA/<br>TDO/TDI 2/ | 9 | I/O | General purpose digital I/O pin<br>ADC10 analog input A7 1/<br>USI: Data output in SPI mode<br>USI: Data i2c in I2C mode<br>JTAG test data output terminal or test data input during programming and test |
| XIN/<br>P2.6/<br>TA0.1 | 13 | I/O | Input terminal of crystal oscillator 3/<br>General purpose digital I/O pin<br>Timer0_A, compare: Out1 output |
| XOUT/<br>P2.7 | 12 | I/O | Output terminal of crystal oscillator 3/<br>General purpose digital I/O pin |

See footnote at end of table

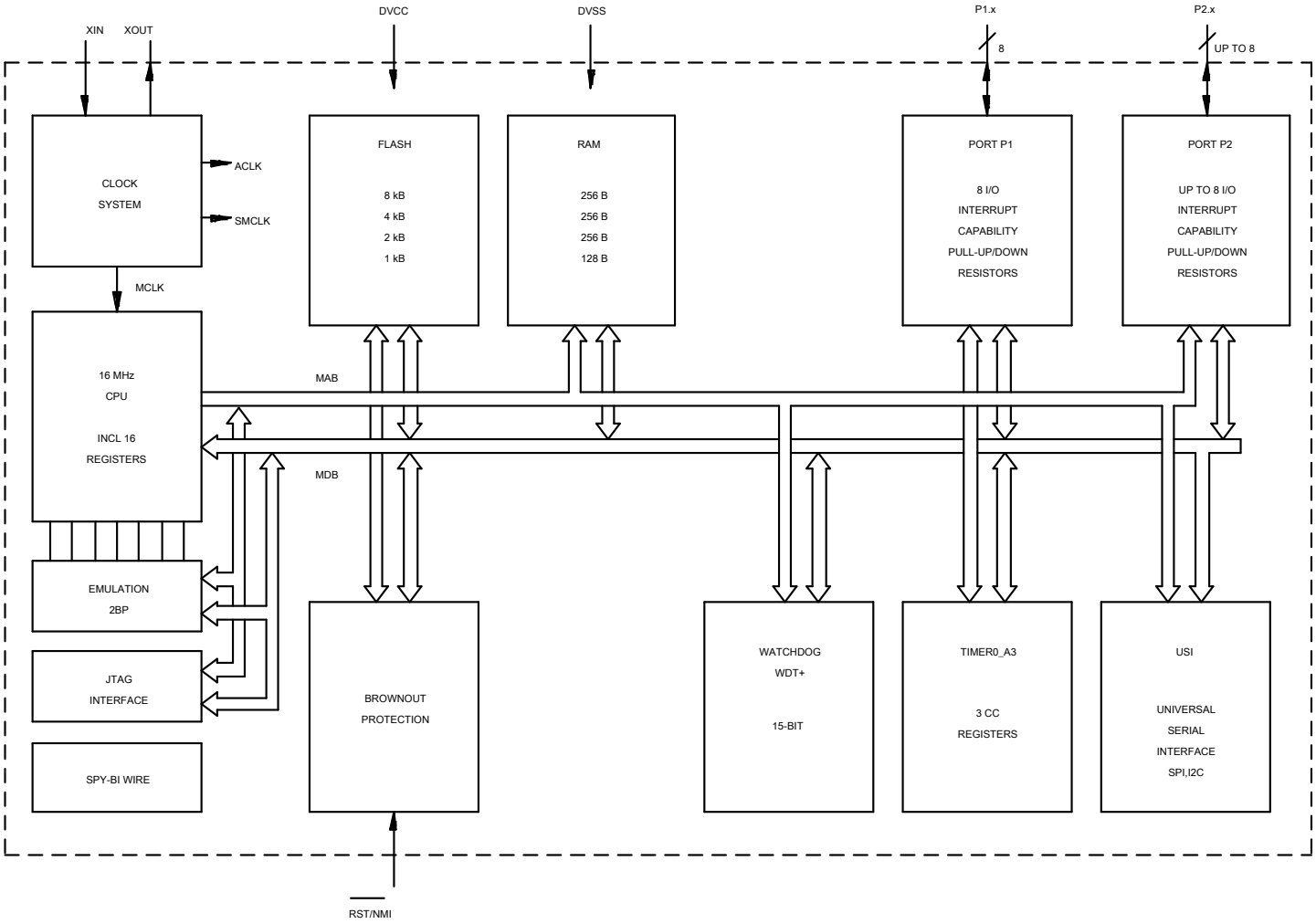
FIGURE 3. Terminal function.

| Terminal | | I/O | Description |
|---|---|---|---|
| Name | Number | | |
| $\overline{\text{RST}}$/<br>NMI/<br>SBWTDIO | 10 | I | Reset<br>Nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output during programming and test |
| TEST/<br><br>SBWTCK | 11 | I | Select test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST.<br>Spy-Bi-Wire test clock input during programming and test. |
| DVCC | 1 | NA | Supply voltage |
| AVCC | NA | NA | Supply voltage |
| DVSS | 14 | NA | Ground reference |
| AVSS | NA | NA | Ground reference |
| NC | - | NA | Not connected |
| QFN Pad | - | NA | QFN package pad connection to $V_{SS}$ recommended. |

NOTES:
1. Available only on device type 02.
2. TDO or TDI is selected via JTAG instruction.
3. If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

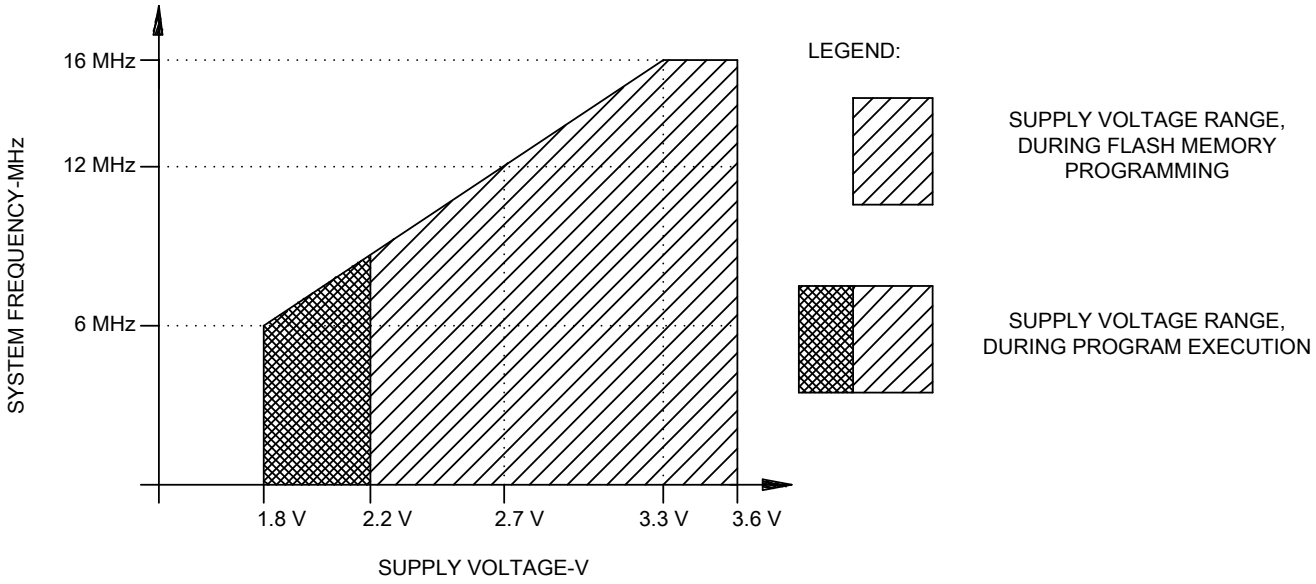
FIGURE 3. Terminal function - Continued.

Device type 01




NOTE:
1. Port P2: two pins are available on the 14 pin package option. Eight pins are available on the 20 pin package option.

FIGURE 4. Functional block diagram.




NOTE:
1. Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum $V_{CC}$ of 2.2 V.

FIGURE 5. Safe operating area.

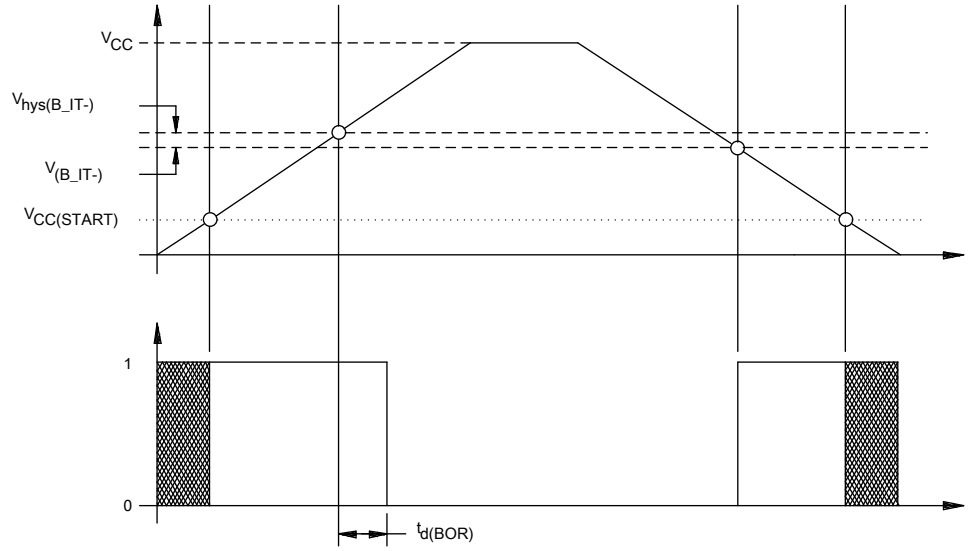



FIGURE 6. POR/Brownout Reset (BOR) vs Supply voltage.

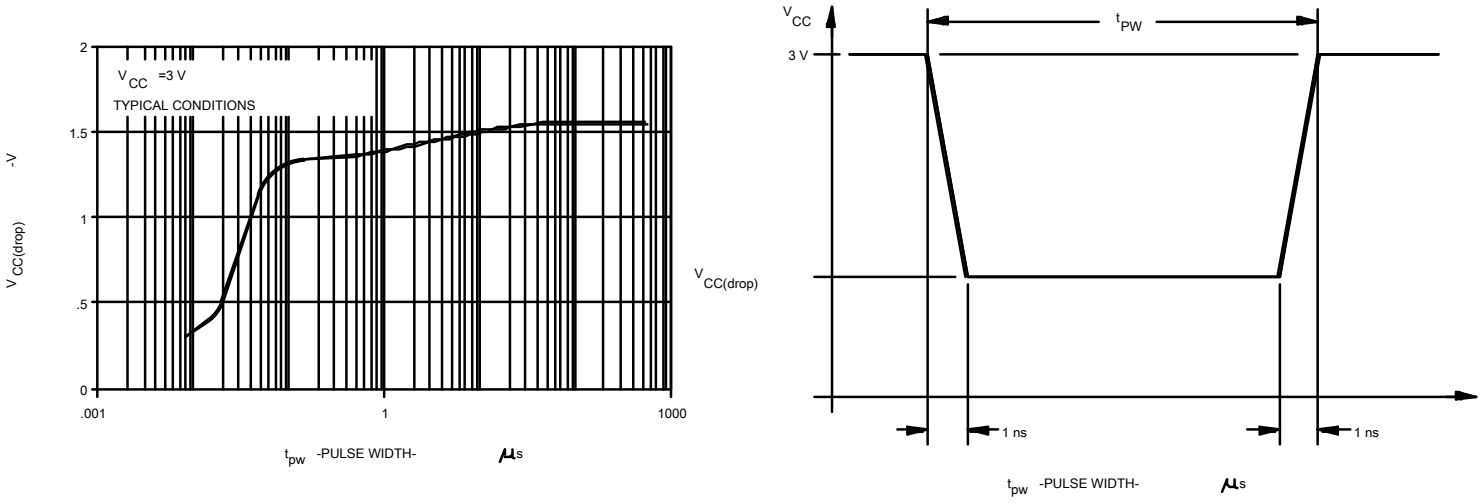



FIGURE 7. $V_{CC(drop)}$ level with a Square voltage drop to generate a POR/Brownout signal.

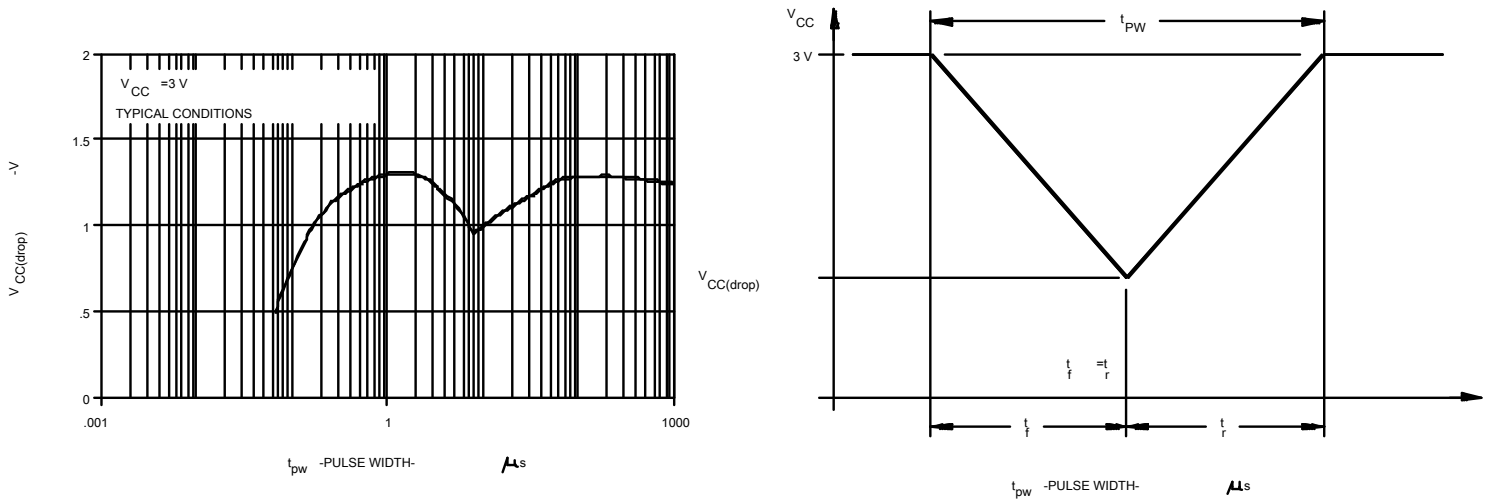



FIGURE 8. $V_{CC(drop)}$ level with a Triangle voltage drop to generate a POR/Brownout signal.

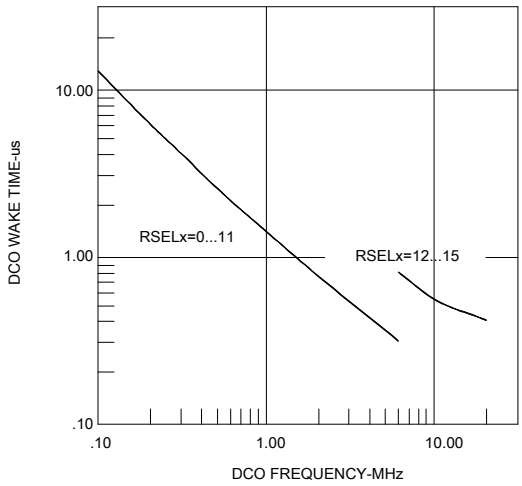



FIGURE 9. DCO wake-up time from LPM3/4 vs DCO frequency.

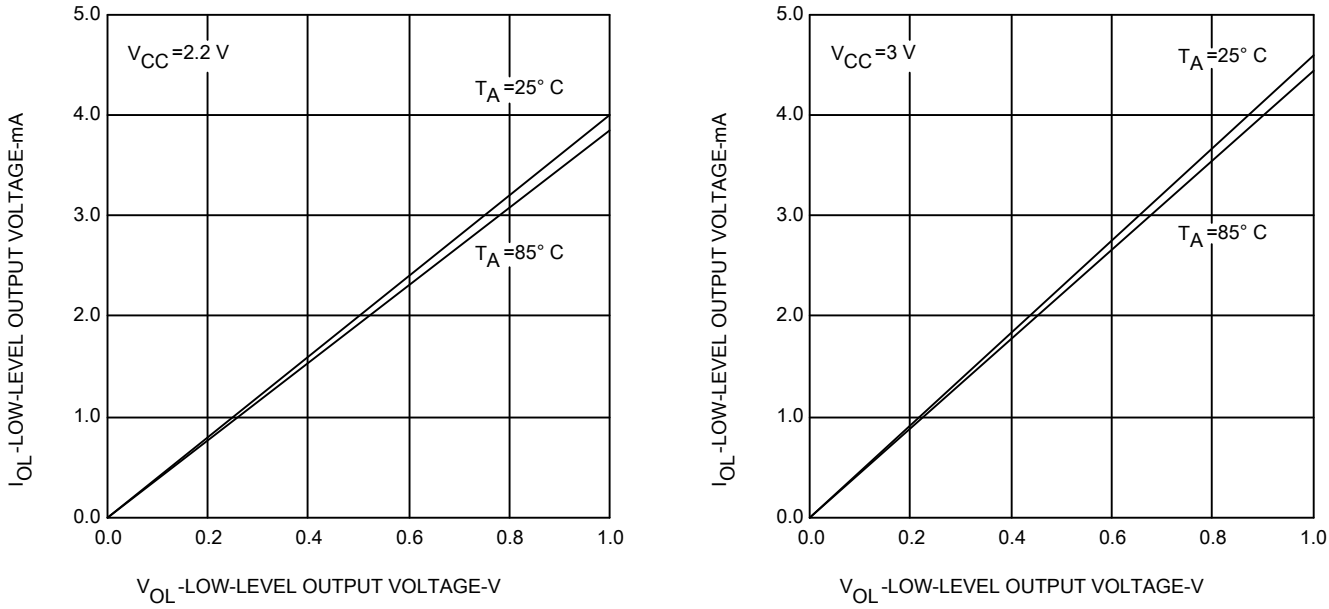



FIGURE 10. USI low level output voltage vs output current.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Top side marking | Transport media | Vendor part number |
|---|---|---|---|---|
| V62/12623-01XE | 01295 | G2302EP | Tape and real | MSP430G2302IPW1REP |
| | | | Tube | MSP430G2302IPW1EP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243 |