REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct Low level and high level output voltage in section 1.5. Change setup time, SPISOMI before SPICLK low and high, in Table I. - phn	12-12-10	Thomas M. Hess
B	Change case outline Y to Lead Finish “F”. Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-05-04	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	23-09-18	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

Original date of drawing

YY MM DD

12-08-14

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TITLE
MICROCIRCUIT, DIGITAL, 16/32 BIT RISC FLASH MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/12622
REV C		PAGE 1 OF 12

AMSC N/A

5962-V157-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16/32 bit RISC Flash microcontroller microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12622	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TMS570LS20206-EP	16/32 bit RISC Flash microcontroller
02	TMS570LS20216-EP	16/32 bit RISC Flash microcontroller

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	144	MS-026	Plastic Quad Flatpack
Y	337	MO-275	Plastic Ball Grid Array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of Sn= 63%, Pb=34.5%. Ag- 2.0% and Sb =0.5% .

1.3 Absolute maximum ratings. 2/

Supply voltage range:
VCC , ... -0.3 V to 2.12 V 3/
VCCIO, VCCAD, VCCP (Flash pump) ..... -0.3 V to 4.1 V 3/
Input voltage ranges, All input pins (V_I): ..... -0.3 V to 4.1 V
Input clamp current:
I_{IK} (V_I < 0 or V_I > V_{CCIO}) ..... ±20 mA
All pins except AD1IN[7:0], AD2IN[7:0], ADSIN[15:8]
I_{IK} (V_I < 0 or V_I > V_{CCAD})
AD1IN[7:0], AD2IN[7:0], ADSIN[15:8] ..... ±10 Ma
Total ..... ±40 mA
Operating free air temperature ranges, (T_A) ..... -55°C to 125°C
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 4/

Parameters	Symbol	Limits		Unit
		Min	Max	
Digital logic supply voltage (Core)	V_{CC}	1.35	1.65	V
Digital logic supply voltage (I/O)	V_{CCIO}	3	3.6	V
MibDC supply voltage	V_{CCAD}	3	3.6	V
Flash pump supply voltage	V_{CCP}	3	3.6	V
Digital logic supply ground	V_{SS}	0 TYP		V
MibADC supply ground	V_{SSAD}	-0.1	0.1	V
Operating free air temperature	T_A	-55	125	°C

1.5 Electrical Characteristics over operating free air temperature range. 5/

Parameters		Symbol	Test conditions	Limits		Unit
				Min	Max	
Input hysteresis		V_{hys} 6/		0.15		V
Low level input voltage	All input 7/	V_{IL}		-0.3	0.8	V
High level output voltage	All input	V_{IH}		2	V_{CCIO} + 0.3	V

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3/ All voltage value are with respect to their associate ground.
4/ All voltages are with respect to VSS except V_{CCAD} is with respect to V_{SSAD}.
5/ Source currents (out of the device) are negative while sink current (into the device) are positive.
6/ This parameter is characterized from -40°C to 125°C only.
7/ This does not apply to $\overline{\text{PORRST}}$ pin.

1.5 Electrical Characteristics over operating free air temperature range - Continued. 5/

Parameters		Symbol	Test conditions	Limits		Unit
				Min	Max	
Low level output voltage		V_{OL}	I_{OL} = I_{OL} MAX		0.2 V_{CCIO}	V
			I_{OL} = 50 µA		0.2	V
High level output voltage		V_{OH}	I_{OH} = I_{OH} MAX	0.8 V_{CCIO}		V
			I_{OH} = 50 µA	V_{CCIO} – 0.2		V
Low level input voltage	OSCIN	$V_{ILoscin}$		-0.3	0.2 V_{CC}	V
High level input voltage	OSCIN	$V_{IHoscin}$		0.8 V_{CC}	V_{CC} + 0.3	V
Voltage monitoring threshold	V_{CC} low	V_{MON}		1.0	1.35	V
	V_{CC} high			1.7	2.38	V
	V_{CCIO} low			2.0	3.0	V
Input clamp current 6/		I_{IC}	V_I < V_{SSIO} -0.3 or V_I > V_{SSIO} + 0.3	-2	2	mA
Input current (I/O pins)	I_{IL} Pulldown	I_I	V_I = V_{SS}	-1	1	µA
	I_{IH} Pulldown 20 µA		V_I = V_{CCIO}	5	40	µA
	I_{IH} Pulldown 100 µA		V_I = V_{CCIO}	40	195	µA
	I_{IL} Pullup 20 µA		V_I = V_{SS}	-40	-3.6	µA
	I_{IL} Pullup 100 µA		V_I = V_{SS}	-195	-40	µA
	I_{IH} Pullup		V_I = V_{CCIO}	-1	1	µA
	All other pins		No pullup or pulldown	-1	1	µA
Low level output current	TDO, TDI, TMS, RTCK, ECLK, FRAYTX1, FRAYTXEN1, FRAYTX2, FRAYTXEN2, $\overline{\text{DMMENA}}$, ETMTRACECTL, ETMTRACECLKOUT, ETMDATA[31:0], RTPSYNC, RTPCLK, RTPDATA[15:0], $\overline{\text{EMIFWE}}$, $\overline{\text{EMIFOE}}$, $\overline{\text{EMIFCS[3:0]}}$, EMIFDATA[15:0], EMIFADD[21:0], EMIFBAD[1:0], $\overline{\text{EMIFDQM[1:0]}}$,$\overline{\text{ERROR}}$	I_{OL}	V_{OL} = V_{OL} MAX		8	mA
	$\overline{\text{RST}}$, MIBSP1CLK, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI3CLK, MIBSPI3SIMO, MIBSPI3SOMI, MIBSPI5CLK, MIBSPI5SIMO[3:0], MIBSPI5SOMI[15:8], DMMDATA[4]				4	mA
	All other input pins				2	mA

See footnote at end of table.

1.5 Electrical Characteristics over operating free air temperature range - Continued. 8/

Parameters		Symbol	Test conditions		Limits Min	Limits Max	Unit
High level output current	TDO, TDI, TMS, RTCK, ECLK, FRAYRX1, FRAYTX1, FRAYTXEN1, FRAYRX2, FRAYTXEN2, ETMTRACECTL, ETMTRACECLKOUT, ETMDATA[31:0], RTPSYNC, RTPCLK, RTPDATA[15:0], $\overline{\text{DMMENA}}$, $\overline{\text{EMIFWE}}$, $\overline{\text{EMIFOE}}$, $\overline{\text{EMIFCS[3:0]}}$, EMIFDATA[15:0], EMIFADD[21:0], EMIFBAD[1:0], $\overline{\text{EMIFDQM[1:0]}}$, $\overline{\text{ERROR}}$	I_{OH}	V_{OH} = V_{OH} MIN			-8	mA
	$\overline{\text{RST}}$, MIBSP1CLK, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI3CLK, MIBSPI3SIMO, MIBSPI3SOMI, MIBSPI5CLK, MIBSPI5SIMO[3:0], MIBSPI5SOMI[15:8], DMMDATA[4]					-4	
	All other input pins					-2	
V_{CC} digital supply current (Operating mode)	All packages	I_{CC} 8/	HCLK = 100MHz, VCLK = 100MHz 6/			350	mA
			HCLK = 140MHz, VCLK = 70MHz			390	
	Case Y package		HCLK = 160MHz, VCLK = 80MHz			430	
V_{CC} digital supply current (CPU selftest mode: LBIST) 6/ 9/ 10/	All packages		STCCLK = 46.666MHz	Peak		510	
			STCCLK = 50MHz	Peak		540	
	Case Y package		STCCLK = 53.333MHz	Peak		580	
V_{CC} digital supply current (Mem selftest mode: PBIST) 6/ 9/ 11/	All packages		HCLK = 800MHz, VCLK = 40MHz	Peak		340	
			HCLK = 100MHz, VCLK = 100MHz	Peak		430	
V_{CC} digital supply current (doze mode)			OSCIN = 6 MHz, V_{CC} = 1.65 V 12/			35	
V_{CC} digital supply current (snooze mode)			All frequencies, V_{CC} = 1.65 V 12/			30	
V_{CC} digital supply current (sleep mode)			All frequencies, V_{CC} = 1.65 V 12/			25	
V_{CCIO} digital supply current (operating mode)		I_{CCIO}	No DC load, V_{CCIO} = 3.6 V 13/			15	mA
V_{CCIO} digital supply current (doze mode)			No DC load, V_{CCIO} = 3.6 V 13/			700	µA
V_{CCIO} digital supply current (snooze mode)			No DC load, V_{CCIO} = 3.6 V 13/			100	
V_{CCIO} digital supply current (sleep mode)			No DC load, V_{CCIO} = 3.6 V 13/			100	

See footnote at end of table.

1.5 Electrical Characteristics over operating free air temperature range - Continued. 6/

Parameters	Symbol	Test conditions	Limits		Unit
			Min	Max	
V_{CCAD} supply current (operating mode)	I_{CCAD}	All frequencies, V_{CCAD} = 3.6 V		30	mA
V_{CCAD} supply current (doze mode)		All frequencies, V_{CCAD} = 3.6 V 12/		200	µA
V_{CCAD} supply current (snooze mode)		All frequencies, V_{CCAD} = 3.6 V 12/		200	µA
V_{CCAD} supply current (sleep mode)		All frequencies, V_{CCAD} = 3.6 V 12/		200	µA
V_{CCP} pump supply current	I_{CCP}	V_{CCP} = 3.6 V read operation		25	mA
		V_{CCP} = 3.6 V program 6/ 14/		90	mA
		V_{CCP} = 3.6 V erase 6/		90	mA
		V_{CCP} = 3.6 V doze mode 12/		5	µA
		V_{CCP} = 3.6 V snooze mode 12/		5	µA
		V_{CCP} = 3.6 V sleep mode 12/		5	µA
Input capacitance 15/	C_I 6/		2 TYP		pF
Output capacitance	C_O 6/		3 TYP		pF

Thermal resistance characteristics :

Parameter	Case outline X	Case outline Y	Unit
Junction to ambient thermal resistance, θ_{JA} 16/	32.1	30.7	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 17/	3.3	4.7	°C/W
Junction to board thermal resistance, θ_{JB} 18/	13.7	15	°C/W
Junction to top characterization parameter, Ψ_{JT} 19/	0.1	0.1	°C/W
Junction to board characterization parameter, Ψ_{JB} 20/	13.3	15	°C/W
Junction to case (bottom) thermal resistance, θ_{JCbot} 21/	N/A	N/A	°C/W

8/ Typical values are at V_{CC} = 1.5 V and maximum are at V_{CC} = 1.65 V.
9/ The peak current is measured on the manufacturer EVM board with two 10 µF and thirteen 100 nF capacitors on VCC domain. Running at a lower frequency consumes less current.
10/ LBIST currents specified are for execution of LBIST with a certain STC clock. Lower current consumption can be achieved by configuring a slower STC clock frequency. The current peak duration can last for the duration of 1 LBIST test interval.
11/ PBIST current specified are for execution of PBIST on all RAMs (group 1-14) and all algorithms. Lower current consumption can be achieved by configuring a slower HCLK frequency. Different algorithms consume different current. For more information, please refer to the manufacturer data.
12/ For Flash banks/pump in sleep mode.
13/ I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} – 0.2 V.
14/ This assumes reading from one bank while programming a different bank.
15/ The maximum input capacitance C_I of the FlexRay RX pin(s) is 10 pF.
16/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC standard, high K board, as specified in JEDEC 51-7, in an environment described in JESD51-2a.
17/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
18/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
19/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
20/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
21/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
J-STD-020	–	Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.
JESD51-8	–	Junction-to-board thermal resistance Theta-JB or RθJB

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Wait states. The wait states shall be as shown in figure 4.

3.5.5 ECLK timing diagram. The ECLK timing diagram shall be as shown in figure 5.

3.5.6 PORRST timing diagram. The PORRST timing diagram shall be as shown in figure 6.

3.5.7 JTAG timing. The JTAG timing shall be as shown in figure 7.

3.5.8 CMOS level outputs. The CMOS level outputs shall be as shown in figure 8.

3.5.9 CMOS level inputs. The CMOS level inputs shall be as shown in figure 9.

3.5.10 SPI Master mode external timing (Clock Phase = 0). The SPI Master mode external timing (Clock Phase = 0) shall be as shown in figure 10.

3.5.11 SPI Master mode chip select timing (Clock Phase = 0). The SPI Master mode chip select timing (Clock Phase = 0) shall be as shown in figure 11.

3.5.12 SPI Master mode external timing (Clock Phase = 1). The SPI Master mode external timing (Clock Phase = 1) shall be as shown in figure 12.

3.5.13 SPI Master mode chip select timing (Clock Phase = 1). The SPI Master mode chip select timing (Clock Phase = 1) shall be as shown in figure 13.

3.5.14 SPI Slave mode external timing (Clock Phase = 0). The SPI Slave mode external timing (Clock Phase = 0) shall be as shown in figure 14.

3.5.15 SPI Slave mode chip select timing (Clock Phase = 0). The SPI Slave mode chip select timing (Clock Phase = 0) shall be as shown in figure 15.

3.5.16 SPI Slave mode external timing (Clock Phase = 1). The SPI Slave mode external timing (Clock Phase = 1) shall be as shown in figure 126

3.5.17 SPI Slave mode chip select timing (Clock Phase = 1). The SPI Slave mode chip select timing (Clock Phase = 1) shall be as shown in figure 17.

3.5.18 Asynchronous memory Read timing for EMIF. The asynchronous memory Read timing for EMIF shall be as shown in figure 18.

3.5.19 Asynchronous memory Write timing for EMIF. The asynchronous memory Write timing for EMIF shall be as shown in figure 19.

3.5.20 ETMTRACECLK timing. The ETMTRACECLK timing shall be as shown in figure 20.

3.5.21 ETMDATA timing. The ETMDATA timing shall be as shown in figure 21.

3.5.22 RTPCLK timing. The RTPCLK timing shall be as shown in figure 22.

3.5.23 RTPDATA timing. The RTPDATA timing shall be as shown in figure 23.

3.5.24 RTPENABLE timing. The RTPENABLE timing shall be as shown in figure 24.

3.5.25 DMMCLK timing. The DMMCLK timing shall be as shown in figure 25.

3.5.26 DMMDATA timing. The DMMDATA timing shall be as shown in figure 26.

3.5.27 $\overline{\text{DMMENA}}$ timing. The $\overline{\text{DMMENA}}$ timing shall be as shown in figure 27.

3.5.28 MibADC input equivalent circuit. The MibADC input equivalent circuit shall be as shown in figure 28.

3.5.29 Differential Nonlinearity (DNL). The Differential Nonlinearity (DNL) shall be as shown in figure 29.

3.5.30 Integral Nonlinearity (INL) error. The Integral Nonlinearity (INL) error shall be as shown in figure 30.

3.5.31 Absolute accuracy (Total) error. The absolute accuracy (Total) error shall be as shown in figure 31.

TABLE I. Electrical performance characteristics. 1/

No.	Test	Symbol	Test conditions 2/	Limits		Unit
				Min	Max	
Peripheral and Electrical Specifications						
Timing requirements for PLL circuits Enabled and disabled						
Input clock frequency		$f_{(OSC)}$ 3/		5		MHz
Input clock frequency		$f_{(OSC)}$			20	MHz
Cycle time, OSCIN		$t_{c(OSC)}$		50		ns
Pulse duration, OSCIN low		$t_{w(OSCL)}$		15		ns
Pulse duration, OSCIN high		$t_{w(OSCH)}$		15		ns
OSC FAIL frequency – upper level		$f_{(OSCRST)}$ 3/		20	50	MHz
OSC FAIL frequency – upper level		$f_{(OSCRST)}$ 3/		1.5	5	MHz
LPO and Clock Detection						
LPO and Clock detection						
Invalid frequency	low threshold			1.5	5	MHz
	upper threshold			20	50	MHz
Limp mode frequency (HFosc)				7.9	14.4	MHz
HFosc frequency				7.9	14.4	MHz
LFosc frequency				62	113	kHz
Switching characteristics for clocks						
HCLK-System clock frequency		$f_{(HCLK)}$	Pipeline mode enabled		160	MHz
(Case outline Y)			Pipeline mode disenabled		36	MHz
HCLK-System clock frequency		$f_{(HCLK)}$	Pipeline mode enabled		140	MHz
(Case outline X)			Pipeline mode disenabled		36	MHz
GCLK – CPU clock frequency (ratio GCLK: HCLK = 1:1)		$f_{(GCLK)}$			$f_{(HCLK)}$	MHz
RCLK – Frequency out of PLL macro into R-divider		$f_{(RCLK)}$			160	MHz
RTICLK – clock frequency		$f_{(RTICLK)}$ 4/			$f_{(VCLK)}$	MHz
VCLK – Primary peripheral clock frequency		$f_{(VCLK)}$			$f_{(VCLK2)}$	MHz
VCLK2 – Secondary peripheral clock frequency		$f_{(VCLK2)}$			100	MHz
AVCLK1 - Primary asynchronous peripheral clock frequency		$f_{(AVCLK1)}$			$f_{(VCLK)}$	MHz
AVCLK2 - Secondary asynchronous peripheral clock frequency		$f_{(AVCLK2)}$			$f_{(VCLK)}$	MHz
ECLK – External clock output frequency for ECP module		$f_{(ECLK)}$ 5/			80	MHz
System clock frequency – Flash programming/erase		$f_{(PROG/ERASE)}$			$f_{(HCLK)}$	MHz
ECLK specification						
Switching characteristics for External clocks 3/ 6/ 7/ (see FIGURE 5)						
3	Pulse duration, ECLK low	$t_{w(EOL)}$	Under all prescale factor combinations (X and N)	$0.5t_{c(ECLK)}$ - tf		ns
4	Pulse duration, ECLK high	$t_{w(EOL)}$	Under all prescale factor combinations (X and N)	$0.5t_{c(ECLK)}$ - tr		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
	$\overline{\text{RST}}$ and $\overline{\text{PORRST}}$				
Timing requirement for $\overline{\text{PORRST}}$ (See FIGURE 6)					
	V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up	V_{CCPORL} 3/		0.5	V
	V_{CC} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	V_{CCPORH} 3/	1.35		V
	V_{CCIO}/ V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up	$V_{CCIOPORL}$ 3/		1.1	V
	V_{CCIO}/ V_{CC} low supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	$V_{CCIOPORH}$ 3/	3		V
	Low level input voltage of $\overline{\text{PORRST}}$ V_{CCIO} > 2.5 V	$V_{IL(PORRST)}$ 3/		0.2 V_{CCIO}	V
	Low level input voltage of $\overline{\text{PORRST}}$ V_{CCIO} < 2.5 V			0.5	V
3	Setup time, $\overline{\text{PORRST}}$ active before V_{CCIO} and V_{CCP} > $V_{CCIOPORL}$ during power up	$t_{su(PORRST)}$ 3/	0		ms
6	Hold time, $\overline{\text{PORRST}}$ active after V_{CC} > V_{CCPORH}	$t_{h(PORRST)}$ 3/	1		ms
7	Setup time, $\overline{\text{PORRST}}$ active before V_{CC} ≤ V_{CCPORH} during power down	$t_{su(PORRST)}$ 3/	8		ms
8	Hold time, $\overline{\text{PORRST}}$ active after V_{CCIO} and V_{CCP} > V_{CCPORH}	$t_{h(PORRST)}$ 3/	1		ms
9	Hold time, $\overline{\text{PORRST}}$ active after V_{CC} > V_{CCPORL}	$t_{h(PORRST)}$ 3/	0		ms
	Filter time, $\overline{\text{PORRST}}$, pulses less than MIN will be filtered out, pulses greater than MAX are guaranteed to generate a reset 8/	$t_{f(PORRST)}$ 3/	20	150	ns
	Filter time, $\overline{\text{RST}}$, pulses less than MIN will be filtered out, pulses greater than MAX are guaranteed to generate a reset	$t_{f(RST)}$	20	150	ns
Switching characteristics for $\overline{\text{RST}}$ 3/ 40/					
	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$t_{v(RST)}$	$1048_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all other)		$8_{c(VCLK)}$		ns
	TEST Pin timing				
	Filler time TEST, pulses less than MIN will be filtered out, pulses greater than MAX are guaranteed to enter TEST mode	$t_{f(TEST)}$	10	80	ns
	JTAG Scan interface timings 10/ (see FIGURE 7)				
	TCK frequency (at HCLKmax)	$f_{(TCK)}$		12	MHz
	RTCK frequency (at TCKmax and HCLKmax)	$f_{(RTCK)}$	10		MHz
1	Delay time, TCK to RTCK	$t_{d(TCK-RTCK)}$		20	ns
2	Setup time, TDI, TMS before RTCK rise (RTCKr)	$t_{su(TDI/TMS-RTCKr)}$	15		ns
3	Hold time, TDI, TMS after RTCKr	$t_{h(RTCKr-TDI/TMS)}$	0		ns
4	Hold time, TDO after RTCKf	$t_{h(RTCKf-TDO)}$	0		ns
5	Delay time, TDO valid after RTCK fall (RTCKf)	$t_{d(RTCKf-TDO)}$		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test		Symbol	Limits	Unit
				TYP	
	Output timing				
	Switching characteristics for output timings versus load capacitance (C_L) (see FIGURE 8)				
	8 mA pins	C_L = 15 pF	t_r	2.5	ns
		C_L = 50 pF		5	ns
		C_L = 100 pF		9	ns
		C_L = 150 pF		12	ns
		C_L = 15 pF	t_f	2.5	ns
		C_L = 50 pF		5	ns
		C_L = 100 pF		9	ns
		C_L = 150 pF		12	ns
	4 mA pins	C_L = 15 pF	t_r	7	ns
		C_L = 50 pF		13	ns
		C_L = 100 pF		21	ns
		C_L = 150 pF		29	ns
		C_L = 15 pF	t_f	7	ns
		C_L = 50 pF		13	ns
		C_L = 100 pF		21	ns
		C_L = 150 pF		29	ns
	2 mA-z pins	C_L = 15 pF	t_r	10	ns
		C_L = 50 pF		17	ns
		C_L = 100 pF		25	ns
		C_L = 150 pF		35	ns
		C_L = 15 pF	t_f	10	ns
		C_L = 50 pF		17	ns
		C_L = 100 pF		25	ns
		C_L = 150 pF		35	ns

No.	Test	Symbol	Limits		Unit
			Min	Max	
	Input timings				
	Timing requirements for input timings 3/ 11/ (see FIGURE 9)				
	Input minimum pulse width	t_{pw}	$t_{c(VCLK)}$ + 10 12/		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test		Symbol	Limits		Unit
				Min	Max	
	Flash timings					
	Timing requirements for program Flash					
	Full word (32 bits) programming time		$t_{prog(32\text{-}bit)}$		300	µs
	2M-byte programming time 13/	-40°C to 125°C	$t_{prog(Total)}$		74	s
		0°C to 60°C, for first 25 cycles			25	s
	ECC programming time		$t_{prog\ ECC(16\text{-}bit)}$		300	µs
	Total ECC bit programming time (256K-byte)	-40°C to 125°C	$t_{prog\ ECC(Total)}$		15	s
		0°C to 60°C, for first 25 cycles			7	s
	Sector erase time (including compaction)	-40°C to 125°C	$t_{erase(sector)}$		15	s
		0°C to 60°C, for first 25 cycles			10	s
	Bank erase time (including compaction, 0°C to 60°C, for first 25 cycles	Bank 0	$t_{erase(bank)}$		20	s
		Bank 1			12	s
		Bank 2			12	s
		Bank 3			12	s
	Write/Erase cycles at T_A = -40°C to 125°C with 15 yrs Data retention requirement 14/		t_{wec}		1000	cycles
	Data retention with continuous 150°C 14/		t_{ret}	1000		hours

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
SPI Master mode timings					
SPI Master mode external timings (clock phase = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)					
SPI Master mode external timings 3/ 15/ 16/ 17/ (see FIGURE 10 and 11)					
1	Cycle time, SPICLK 18/	$t_{c(SPC)M}$	50	$256t_{c(VCLK)}$	ns
2	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} - 3 - t_r$	$0.5t_{c(SPC)M} + 5$	ns
19/	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} - 3 - t_f$	$0.5t_{c(SPC)M} + 5$	ns
3	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} - 3 - t_f$	$0.5t_{c(SPC)M} + 5$	ns
19/	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} - 3 - t_r$	$0.5t_{c(SPC)M} + 5$	ns
4 19/	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)	$t_{d(SIMO-SPCL)M}$	$0.5t_{c(SPC)M} - 10$		ns
	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)	$t_{d(SIMO-SPCH)M}$	$0.5t_{c(SPC)M} - 10$		ns
5 19/	Valid time, SPISIMO valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)M}$	$0.5t_{c(SPC)M} - t_{f(SPC)} - 7$		ns
	Valid time, SPISIMO valid before SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)M}$	$0.5t_{c(SPC)M} - t_{r(SPC)} - 7$		ns
6 19/	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	$t_{su(SOMI-SPCL)M}$	$t_{f(SPC)}$		ns
	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	$t_{su(SOMI-SPCH)M}$	$t_{r(SPC)} + 4$		ns
7 19/	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SOMI)M}$	10		ns
	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SOMI)M}$	10		ns
8 20/	Setup time CS active until SPICLK high, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 0)	$t_{C2TDELAY}$	21/	22/	ns
	Setup time CS active until SPICLK low, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 1)		21/	22/	ns
9 20/	Hold time SPICLK low until CS inactive (clock polarity = 0)	$t_{C2TDELAY}$	23/	24/	ns
	Hold time SPICLK high until CS inactive (clock polarity = 1)		23/	24/	ns
10	SPIENAn sample point	t_{SPIENA}	25/	26/	ns
11	SPIENAn sample point from write to buffer	$t_{SPIENAW}$		27/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
SPI Master mode timings – Continued.					
SPI Master mode external timings (clock phase = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)					
SPI Master mode external timings 3/ 15/ 16/ 17/ (see FIGURE 12 and 13)					
1	Cycle time, SPICLK 18/	$t_{c(SPC)M}$	50	$256t_{c(VCLK)}$	ns
2	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} – 3 - t_r$	$0.5t_{c(SPC)M} + 5$	ns
19/	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} – 3 – t_f$	$0.5t_{c(SPC)M} + 5$	ns
3	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$	$0.5t_{c(SPC)M} – 3 – t_f$	$0.5t_{c(SPC)M} + 5$	ns
19/	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$	$0.5t_{c(SPC)M} – 3 - t_r$	$0.5t_{c(SPC)M} + 5$	ns
4	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)	$t_{d(SIMO-SPCL)M}$	$0.5t_{c(SPC)M} - 10$		ns
19/	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)	$t_{d(SIMO-SPCH)M}$	$0.5t_{c(SPC)M} - 10$		ns
5	Valid time, SPISIMO valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)M}$	$0.5t_{c(SPC)M} – t_{f(SPC)} - 7$		ns
19/	Valid time, SPISIMO valid before SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)M}$	$0.5t_{c(SPC)M} – t_{r(SPC)} - 7$		ns
6	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	$t_{su(SOMI-SPCL)M}$	$t_{f(SPC)} + 4$		ns
19/	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	$t_{su(SOMI-SPCH)M}$	$t_{r(SPC)}$		ns
7	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SOMI)M}$	10		ns
19/	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SOMI)M}$	10		ns
8	Setup time CS active until SPICLK high, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 0)	$t_{C2TDELAY}$	21/	22/	ns
20/	Setup time CS active until SPICLK low, assumes that SPInENA is low at t_{SPIENA} (clock polarity = 1)		21/	22/	ns
9	Hold time SPICLK low until CS inactive (clock polarity = 0)	$t_{C2TDELAY}$	23/	24/	ns
20/	Hold time SPICLK high until CS inactive (clock polarity = 1)		23/	24/	ns
10	SPIENAn sample point	t_{SPIENA}	25/	26/	ns
11	SPIENAn sample point from write to buffer	$t_{SPIENAW}$		27/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
	SPI Slave mode timings				
	SPI Slave mode external timings (clock phase = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)				
SPI Slave mode external timings 3/ 15/ 16/ 17/ (see FIGURE 14 and 15)					
1	Cycle time, SPICLK 28/	$t_{c(SPC)S}$	90		ns
2	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$	30		ns
19/	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$	30		ns
3	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$	30		ns
19/	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$	30		ns
4	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)	$t_{d(SPCH-SOMI)S}$		$t_{rf(SOMI)}$ + 15	ns
19/	Delay time, SPISIMO valid after SPICLK low (clock polarity = 1)	$t_{d(SPCL-SOMI)S}$		$t_{rf(SOMI)}$ + 15	ns
5	Valid time, SPISOMI valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$	0		ns
19/	Valid time, SPISOMI valid before SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$	0		ns
6	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{su(SIMO-SPCL)S}$	4		ns
19/	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{su(SIMO-SPCH)S}$	4		ns
7	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SIMO)S}$	6		ns
19/	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SIMO)S}$	6		ns
8	Delay time SPIENAn high after last SPICLK low (clock polarity = 0)	$t_{d(SPCL-SENAH)S}$	$1.5t_{c(VCLK)}$	29/	ns
	Delay time SPIENAn high after last SPICLK high (clock polarity = 1)	$t_{d(SPCH-SENAH)S}$	$1.5t_{c(VCLK)}$	29/	ns
9	Delay time SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{d(SPCH-SENAL)S}$	$t_{f(ENAn)}$	30/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
	SPI Slave mode timings – Continued.				
	SPI Slave mode external timings (clock phase = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)				
SPI Slave mode external timings 3/ 15/ 16/ 17/ (see FIGURE 16 and 17)					
1	Cycle time, SPICLK 28/	$t_{c(SPC)S}$	90		ns
2	Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$	30		ns
19/	Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$	30		ns
3	Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$	30		ns
19/	Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$	30		ns
4	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)	$t_{d(SPCH-SOMI)S}$		$t_{rf(SOMI)}$ + 15	ns
19/	Delay time, SPISIMO valid after SPICLK low (clock polarity = 1)	$t_{d(SPCL-SOMI)S}$		$t_{rf(SOMI)}$ + 15	ns
5	Valid time, SPISOMI valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$	0		ns
19/	Valid time, SPISOMI valid before SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$	0		ns
6	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{su(SIMO-SPCL)S}$	4		ns
19/	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{su(SIMO-SPCH)S}$	4		ns
7	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SIMO)S}$	6		ns
19/	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SIMO)S}$	6		ns
8	Delay time SPIENAn high after last SPICLK low (clock polarity = 0)	$t_{d(SPCL-SENAH)S}$	$1.5t_{c(VCLK)}$	29/	ns
	Delay time SPIENAn high after last SPICLK high (clock polarity = 1)	$t_{d(SPCH-SENAH)S}$	$1.5t_{c(VCLK)}$	29/	ns
9	Delay time SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{d(SPCH-SENAL)S}$	$t_{f(ENAn)}$	30/	ns
10	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)	$t_{d(SPCL-SOMI)S}$	$t_{c(VCLK)}$	31/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
	CAN controller mode timings				
Dynamic characteristics for the CANxTX and CANnRX pins 3/					
	Delay time, transmit shift register to CANnTX pin 32/	$t_{d(CANnTX)}$		15	ns
	Delay time, CANnRX pin to receive shift register	$t_{d(CANnRX)}$		5	ns
	Jitter timing 3/				
	clock jitter and signal symmetry	t_{TX1bit}	98	102	ns
	Flexray BSS (byte star sequence) to BSS	$t_{TX10bit}$	999	1001	ns
	average over 10000 samples	$t_{TX10bitAvg}$	999.5	1000.5	ns
	delay difference between rise and fall from Rx pin to sample point in FlexRay core	$t_{RXAsymDelay}$		2.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
	EMIF timings 3/ 33/ 34/				
Reads and Writes					
1	Turn around time	$t_{d(TURNAROUND)}$	(TA+1)*E – $t_{r(CS)}$ -2	(TA+1)*E –$t_{r(CS)}$+3	ns
Reads (see FIGURE 18)					
2	EMIF read cycle time	$t_{c(EMRCYCLE)}$	(RS+RST+RH+ TA+4)*E-$t_{f(CS)}$ -3	(RS+RST+RH+ TA+4)*E-$t_{f(CS)}$ +3	ns
3	Output setup time, $\overline{\text{EMIFCS}[3:0]}$ low to $\overline{\text{EMIFOE}}$ low (SS=0)	$t_{su(EMCSL-EMOEL)}$	(RS+1)*E-$t_{r(CS)}$ +$t_{f(OE)}$ -5	(RS+1)*E-$t_{r(CS)}$ +$t_{f(OE)}$ +5	ns
	Output setup time, $\overline{\text{EMIFCS}[3:0]}$ low to $\overline{\text{EMIFOE}}$ low (SS=1)		-$t_{r(CS)}$ +$t_{f(OE)}$ -5	-$t_{r(CS)}$ +$t_{f(OE)}$ +5	ns
4	Output hold time, $\overline{\text{EMIFCS}[3:0]}$ high to $\overline{\text{EMIFCS}[3:0]}$ high (SS=0)	$t_{h(EMOEH-EMCSH)}$	(RH+1)*E-$t_{r(OE)}$ +$t_{r(CS)}$ - 4	(RH+1)*E-$t_{r(OE)}$ +$t_{r(CS)}$ + 6	ns
	Output hold time, $\overline{\text{EMIFCS}[3:0]}$ high to $\overline{\text{EMIFCS}[3:0]}$ high (SS=1)		-$t_{r(OE)}$ +$t_{r(CS)}$ - 4	-$t_{r(OE)}$ +$t_{r(CS)}$ +6	ns
5	Output setup time, EMIFBADD[1:0] valid to $\overline{\text{EMIFOE}}$ low	$t_{su(EMBAV-EMOEL)}$	(RS+1)*E-$t_{rf(AD)}$ +$t_{f(OE)}$ - 5	(RS+1)*E-$t_{rf(AD)}$ +$t_{f(OE)}$ + 5	ns
6	Output hold time, $\overline{\text{EMIFOE}}$ high to EMIFBADD[1:0] invalid	$t_{h(EMOEH-EMBAIV)}$	(RS+1)*E-$t_{r(OE)}$ - 5	(RS+1)*E-$t_{r(OE)}$ + 5	ns
7	Output setup time, EMIFADD[21:0] valid to $\overline{\text{EMIFOE}}$ low	$t_{su(EMAV-EMEOL)}$	(RS+1)*E-$t_{rf(AD)}$ +$t_{f(OE)}$ - 6	(RS+1)*E-$t_{rf(AD)}$ +$t_{f(OE)}$ + 6	ns
8	Output hold time, $\overline{\text{EMIFOE}}$ high to EMIFADD[21:0] invalid	$t_{h(EMOEH-EMAIV)}$	(RH+1)*E-$t_{r(OE)}$ - 5	(RH+1)*E-$t_{r(OE)}$ + 6	ns
9	$\overline{\text{EMIFOE}}$ active low width	$t_{w(EMEOL)}$	(RST+1)*E-$t_{f(OE)}$ - 1	(RST+1)*E-$t_{f(OE)}$ + 0	ns
10	Setup time, EMIFD[15:0] valid before $\overline{\text{EMIFOE}}$ high	$t_{su(EMDV-EMOEH)}$	$t_{r(OE)}$ + 9		ns
11	Hold time, EMIFD[15:0] valid after $\overline{\text{EMIFOE}}$ high	$t_{h(EMOEH-EMDV)}$	-$t_{r(OE)}$ - 3		ns
Writes (see FIGURE 19)					
12	EMIF write cycle time	$t_{c(EMWCYCLE)}$	(WS+WST+WH+ TA+4)*E-$t_{f(CS)}$ -3	(WS+WST+WH+ TA+4)*E-$t_{f(CS)}$+ 2	ns
13	Output setup time, $\overline{\text{EMIFCS}[3:0]}$ low to $\overline{\text{EMIFWE}}$ low (SS=0)	$t_{su(EMCSL-EMWEL)}$	(WS+1)*E-$t_{r(CS)}$ +$t_{f(WE)}$ -5	(WS+1)*E-$t_{r(CS)}$ +$t_{f(WE)}$ + 5	ns
	Output setup time, $\overline{\text{EMIFCS}[3:0]}$ low to $\overline{\text{EMIFWE}}$ low (SS=1)		-$t_{r(CS)}$ +$t_{f(WE)}$ -5	-$t_{r(CS)}$ +$t_{f(WE)}$ + 5	ns
14	Output hold time, $\overline{\text{EMIFWE}}$ high to $\overline{\text{EMIFCS}[3:0]}$ high (SS=0)	$t_{h(EMWEH-EMCSH)}$	(WH+1)*E-$t_{r(WE)}$ +$t_{r(CS)}$ - 4	(WH+1)*E-$t_{r(WE)}$ +$t_{r(CS)}$ + 5	ns
	Output hold time, $\overline{\text{EMIFWE}}$ high to $\overline{\text{EMIFCS}[3:0]}$ high (SS=1)		-$t_{r(WE)}$ +$t_{r(CS)}$ - 4	-$t_{r(WE)}$ +$t_{r(CS)}$ +5	ns
15	Output setup time, EMIFBADD[1:0] valid to $\overline{\text{EMIFWE}}$ low	$t_{su(EMBAV-EMWEL)}$	(WS+1)*E-$t_{rf(AD)}$ +$t_{f(WE)}$ - 5	(WS+1)*E-$t_{rf(AD)}$ +$t_{f(WE)}$ + 5	ns
16	Output hold time, $\overline{\text{EMIFWE}}$ high to EMIFBADD[1:0] invalid	$t_{h(EMWEH-EMBAIV)}$	(WH+1)*E-$t_{r(WE)}$ - 5	(WH+1)*E-$t_{r(WE)}$+ 5	ns
17	Output setup time, EMIFADD[21:0] valid to $\overline{\text{EMIFWE}}$ low	$t_{su(EMAV-EMEWL)}$	(WS+1)*E-$t_{rf(AD)}$ +$t_{f(WE)}$ - 6	(WS+1)*E-$t_{rf(AD)}$ +$t_{f(WE)}$ + 6	ns
18	Output hold time, $\overline{\text{EMIFWE}}$ high to EMIFADD[21:0] invalid	$t_{h(EMWEH-EMAIV)}$	(WH+1)*E-$t_{r(WE)}$ - 5	(WH+1)*E-$t_{r(OE)}$+ 6	ns
19	$\overline{\text{EMIFWE}}$ active low width	$t_{w(EMEWL)}$	(WST+1)*E-$t_{f(WE)}$ - 1	(WST+1)*E-$t_{f(WE)}$+1	ns
20	Setup time, EMIFD[15:0] valid before $\overline{\text{EMIFWE}}$ low	$t_{su(EMDV-EMWEH)}$	(WS+1)*E-$t_{rf(AD)}$ +$t_{f(WE)}$ - 6	(WS+1)*E-$t_{rf(AD)}$ +$t_{f(WE)}$ + 5	ns
21	Hold time, EMIFD[15:0] valid after $\overline{\text{EMIFWE}}$ high	$t_{h(EMWEH-EMDV)}$	(WH+1)*E-$t_{r(WE)}$ - 5	(WH+1)*E-$t_{r(WE)}$+ 5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Limits		Unit
			Min	Max	
	ETM timings				
ETMTRACECLK timing 3/ (see FIGURE 20)					
	Clock frequency	$f(ETM)_{cyc}$		40	MHz
	Clock period	$t(ETM)_{cyc}$	25		ns
	Low pulse width	$t(ETM)_{l}$	2		ns
	High pulse width	$t(ETM)_{h}$	2		ns
	Clock and data rise time	$t(ETM)_{r}$	3		ns
	Clock and data fall time	$t(ETM)_{f}$	3		ns
ETMDATA timing 10/ (see FIGURE 21)					
	Data setup time	$t(ETM)_{su}$	2.5 TYP		ns
	Data hold time	$t(ETM)_{ho}$	1.5 TYP		ns
	TTP timings				
RTPCLK timing 3/ (see FIGURE 22)					
	Clock period (depending on HCLK divide ratio)	$t(RTP)_{cyc}$	10		ns
	High pulse width (depending on HCLK divide ratio and load on pin)	$t(RTP)_{h}$	$(t(RTP)_{cyc}/2) - ((tr+tf)/2) - 1.5$		ns
	Low pulse width (depending on HCLK divide ratio and load on pin)	$t(RTP)_{l}$	$(t(RTP)_{cyc}/2) - ((tr+tf)/2) - 1.5$		ns
RTPDATA timing 3/ 10/ (see FIGURE 23)					
	Data setup time	$t(RTP)_{dsu}$	$0.5\ t(RTP)_{cyc} - 3$		ns
	Data hold time	$t(RTP)_{dho}$	$0.5\ t(RTP)_{cyc} - 2$		ns
	SYNC setup time	$t(RTP)_{ssu}$	$0.5\ t(RTP)_{cyc} - 3$		ns
	SYNC hold time	$t(RTP)_{sho}$	$0.5\ t(RTP)_{cyc} - 2$		ns
RTPENABLE timing 3/ (see FIGURE 24)					
	Time that $\overline{RTPENA}$ must go high before the next scheduled RTPSYNC in order to suspend transmission for the packet following the scheduled RTPSYNC	$t(RTP)_{disable}$	$1.5t_{c(HCLK)} + t_{r(RTPSYNC)} + 12$		ns
	Time after $\overline{RTPENA}$ must goes low before a packet that has been halted, resumes	$t(RTP)_{enable}$	$4.5t_{c(HCLK)} + t_{r(RTPSYNC)}$	$5.5t_{c(HCLK)} + t_{r(RTPSYNC)} + 12$	ns
	DMM timings				
DMMCLK timing 3/ (see FIGURE 25)					
	Clock period	$t(DMM)_{cyc}$	$t_{c(HCLK)} + 2$		ns
	High pulse width	$t(DMM)_{h}$	$t(DMM)_{cyc}/2 - (tr+tf)/2$		ns
	Low pulse width	$t(DMM)_{l}$	$t(DMM)_{cyc}/2 - (tr+tf)/2$		ns
DMMDATA timing 3/ (see FIGURE 26)					
	SYNC active to clk falling edge setup time	$t(DMM)_{ssu}$	2		ns
	clk falling edge to SYNC deactive hold time	$t(DMM)_{sho}$	3		ns
	DATA to clk falling edge setup time	$t(DMM)_{dsu}$	2		ns
	clk falling edge to DATA hold time	$t(DMM)_{dho}$	3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Test conditions 2/		Limits Min	Limits Max	Unit
			MibADC				
MibADC recommended operating conditions 35/			(see FIGURE 28 - 31)				
	A-to-D high voltage reference source	AD_{REFHI}			3	3.6	V
	A-to-D low voltage reference source	AD_{REFLO}			0	0.3	V
	Analog input voltage	V_{AI}			AD_{REFLO}	AD_{REFHI}	V
	Analog input clamp current 36/ ($VAI < V_{SSAD}$ -0.3 or $VAI > V_{CCAD}$ + 0.3)	I_{AIC}			-2	2	mA
Operating characteristics over full range of Recommended operating conditions							
	Analog input mux on-resistance					250	Ω
	ADC sample switch on-resistance					250	Ω
	Input mux capacitance					16	pF
	ADC sample capacitance				11	13	pF
	Analog input leakage current		Input leakage per ADC input pin		-200	200	nA
	ADREFHI input current		AD_{REFHI} = 3.6 V, $AD_{REFLO} = V_{SSAD}$			5	mA
	Conversion range over which specified accuracy is maintained		AD_{REFHI} - AD_{REFLO}		3	3.6	V
	Differential nonlinearity error		Difference between the actual step width and the idel value			±3.8	LSB
	Integral nonlinearity error		Maximum deviation from the best straight line through the MibADC . MibADC transfer characteristics, excluding the quantization error.			±3.7	LSB
	Total error/Absolute accuracy		Maximum value of the difference between an analog value and the ideal midstep value	Executing periodic internal calibration		±8 38/	LSB
				No calibration		±15	LSB
MibADC timings 3/							
	Cycle time, MibADC clock	$t_{c(ADCLK)}$			33		ns
	Delay time, sample and hold time	$t_{d(SH)}$			200		ns
	Delay time, conversion time	$t_{d(C)}$			400		ns
	Delay time, total sample/hold and conversion time	$t_{d(SHC)}$ 39/			600		ns

See footnotes at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Recommended ranges of supply voltage and operating junction temperature (unless otherwise noted).

3/ These parameters is characterized from -40°C to 125°C only.

4/ If the RTIx clock source is chosen to be anything other than the default VCLK, then the RTI clock needs to be at least three times slower than the VCLK.

5/ (ECLK) = f(VCLK) / N, where N = (1 to 65536). N is the ECP prescale value defined by the ECPCNTL.[15:0] register bits in the System module. Pipeline mode enabled or disabled is determined by the FRDCNTL[2:0].

6/ X = {1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16}. X is the VBUS interface clock divider ratio determined by the CLKCNTL.[19:16] bits in the SYS module.

7/ N = {1 to 65536}. N is the ECP prescal value defined by the ECPCNTL.[15:0] register bits in the System module.

8/ A low pulse on the nPORRST pin which is just barely longer than the glitch filter implemented on this pin will result in a very short internal reset. This may result in unpredictable behavior as some parts of the device may be reset while other parts of the device are not.

9/ Specified values do not include rise/fall times. For rise and fall timings, see the switching characteristics for output timings versus load capacitance table.

10/ The timings in this table are measured with a 50 pF and 50 µA load. And they are measured at the 50% point, not 20% 0r 80% point.

11/ $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = $1/f_{(VCLK)}$

12/ The timings shown is only valid for pin used in GIO mode.

13/ This programming time includes overhead of state machine, but does not include data transfer time.

14/ Flash write/erase cycles and data retention specifications are based on a validated implementation of the manufacturer flash API. Non manufacturer flash API implementation is not supported. For detail information see manufacturer data. The flash memory cells are qualified for data retention greater than 1000 hours at 150°C. Data retention at reduced temperatures can be estimated based on an Amherius model with activation energy of 1 eV.

15/ The Master bit (SPIGCR1.0) is set and the CLOCK Phase bit (SPIMTx.16) is set.

16/ $t_{c(VCLK)}$ = interface clock cycle time = 1/ f(VCLK).

17/ For rise and fall timings, see the “switching characteristics for output timings versus load capacitance” table.

18/ When the SPI is Master mode, the following must be true:

For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)tc(VCLK) \geq 50$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.

For PS value of 0: : $t_{c(SPC)M} = 2tc(VCLK) \geq 50$ ns. The external load on the SPICLK pin must be less than 60 pF.

19/ The active edge of the SPICLK signal references is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

20/ C2TDELAY and T2CDELAY are programmed in the SPIDELAY register.

21/ $(C2TDELAY + CSHOLD + 2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 9$

22/ $(C2TDELAY + CSHOLD + 2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5$

23/ $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 5$

24/ $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 10$

25/ $C2TDELAY*t_{c(VCLK)} - t_{f(SPICS)} - 20$

26/ $C2TDELAY*t_{c(VCLK)}$

27/ $(C2TDELAY+2)*t_{c(VCLK)}$

28/ When the SPI is Slave mode, the following must be true:

$t_{c(SPC)S} > 2tc(VCLK)$ and $t_{c(SPC)S} \geq 90$ ns.

$t_{w(SPC)S} > tc(VCLK)$ and $t_{w(SPCL)S} > t_{c(VCLK)}$.

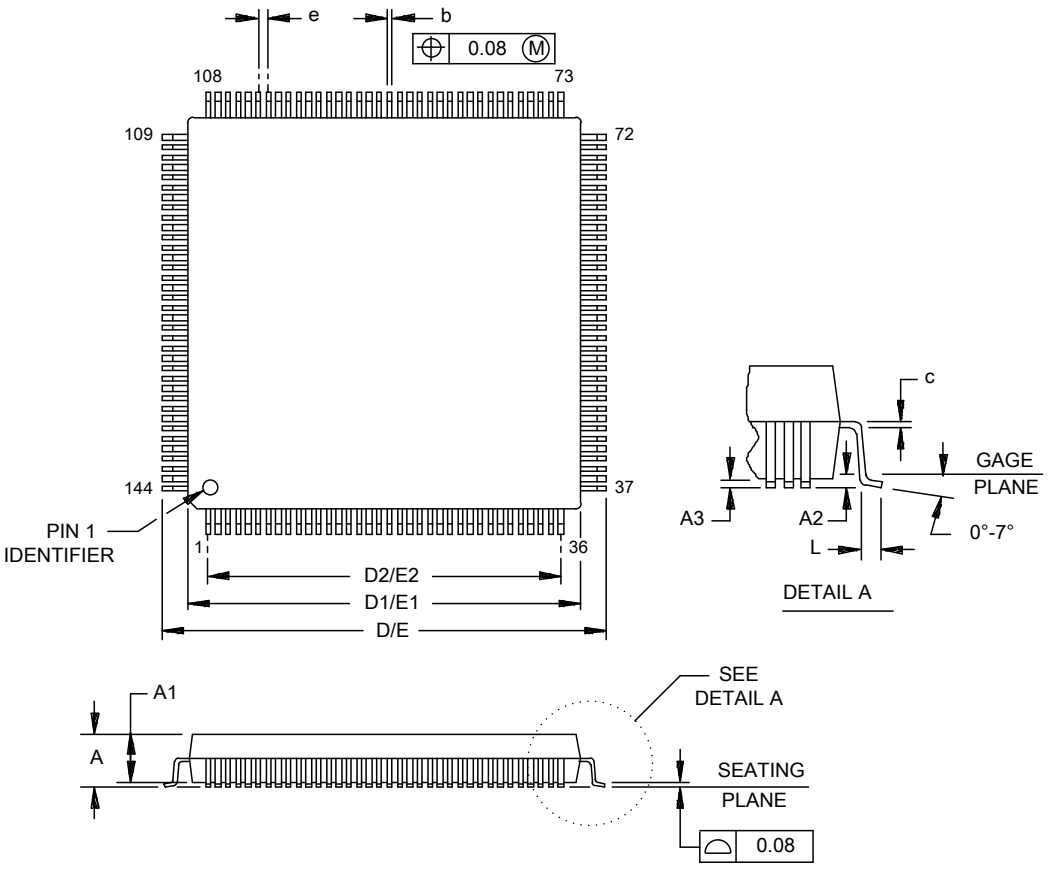
29/ $2.5t_{c(VCLK)} + t_{r(ENAn)} + 26$

TABLE I. Electrical performance characteristics - Continued. 1/

30/ $t_{c(VCLK)} + t_{f(ENAn)} + 18$
31/ $2t_{c(VCLK)} + t_{rf(SOMI)} + 20$
32/ These values do not include rise/fall times of the output buffer.
33/ RS = Read setup, RST = Read Strobe, RH = Read Hold, WS = Write setup, WST = Write Strobe, WH = Writ Hold, TA = Turn around, SS = Strobe Select mode.
34/ E = VCLK period in ns.
35/ For VCCAD and VSSAD recommended operating conditions, see “device recommended operating conditions” table.
36/ Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.
37/ 1 LSB = $(AD_{REFHI} – ADR_{EFLO})/2^{12}$ for the MibADC.
38/ An periodic internal offset calibration is required to achieve the absolute accuracy. Please refer to manufacturer data for more information.
39/ This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, e.g the prescale settings.

40/ Specified values do not include rise/fall times. For rise and fall timings, see the switching characteristics for output timings versus load capacitance table.

Case X

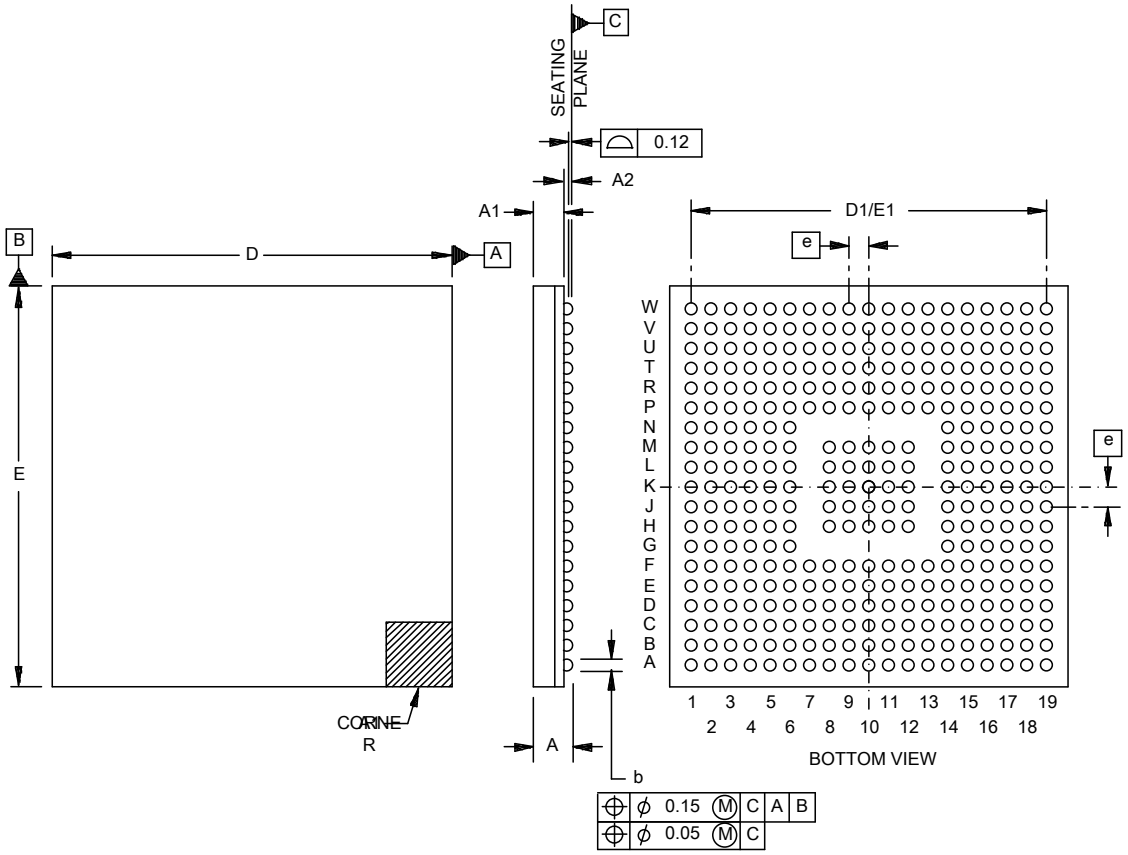


Dimensions					
Symbol	Millimeters		Symbol	Millim eters	
	Min	Max		Min	Max
A		1.60	D/E	21.80	22.20
A1	1.35	1.45	D1/E1	19.80	20.20
A2	0.25 TYP		D2/E2	17.50 TYP	
A3	.005		e	0.50 BSC	
b	0.17	0.27	L	0.45	0.75
c	0.13 NOM				

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Fall within JEDEC MS-026.

FIGURE 1. Case outlines.

Case Y



Dimensions					
Symbol	Millimeters		Symbol	Millim eters	
	Min	Max		Min	Max
A	1.19	1.40	D/E	15.90	16.10
A1	0.84	0.95	D1/E1	14.40	TYP
A2	0.35	0.45	e	0.65	BSC
b	0.45	0.55			

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.
4. Falls within JEDEC MO-275.

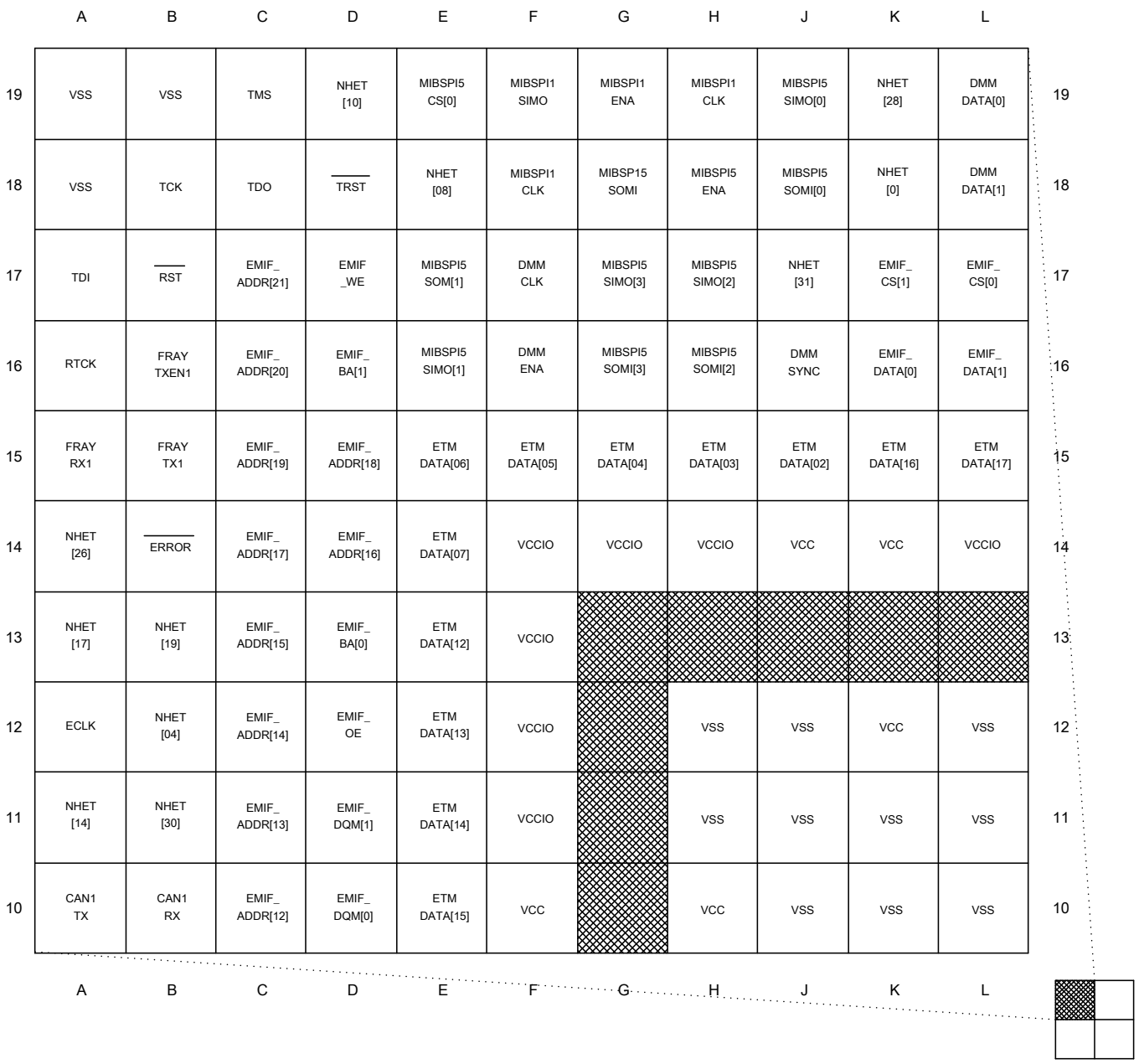
FIGURE 1. Case outlines - Continued.

Case X

Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name	Terminal number	Terminal name
1	VCCIO	37	VCC	73	ADSIN[10]	109	NHET[7]
2	VSSIO	38	VSS	74	ADSIN[9]	110	GIO[4]/INT[4]
3	MIBSPI3CLK	39	VSSIO	75	ADSIN[8]	111	GIO[5]/INT[5]
4	MIBSPI3SIMO	40	VCCIO	76	ADSIN[7]	112	NHET[18]
5	MIBSPI3SOMI	41	NHET[3]	77	ADSIN[6]	113	NHET[15]
6	nMIBSPI3ENA	42	NHET[1]	78	ADSIN[5]	114	VCC
7	NMIBSPI3CS[0]	43	NHET[24]	79	ADSIN[4]	115	VSS
8	NHET[12]	44	NHET[5]	80	ADSIN[3]	116	NHET[10]
9	NHET[22]	45	NHET[20]	81	ADSIN[2]	117	NHET[11]
10	NHET[18]	46	VSS	82	ADSIN[1]	118	GIO[0]/INT[0]
11	NHET[21]	47	VCC	83	ADSIN[0]	119	VCCIO
12	NHET[23]	48	NHET[6]	84	AD1EVT	120	VSSIO
13	MIBSPI1SOMI	49	CAN1RX	85	nRST	121	NHET[4]
14	MIBSPI1SIMO	50	CAN1TX	86	VSS	122	FLTP1
15	VCCIO	51	GIOA[7]/INT[7]	87	VCC	123	FLTP2
16	VSSIO	52	LIN1TX	88	ECLK	124	FRAYTX1
17	MIBSPI1CLK	53	LIN1RX	89	VSSIO	125	FRAYTXEN1
18	nMIBSPI1ENA	54	CAN2TX	90	VCCIO	126	FRAYRX1
19	VCC	55	CAN2RX	91	DMMDATA[4]/MIBSPI5CLK	127	VSS
20	OSCIN	56	NHET[2]	92	DMMDATA[5]/nMIBSPICS[0]	128	VCCP
21	OSCOUT	57	NHET[9]	93	DMMDATA[6]/ nMIBSPICS[1]	129	FRAYTX2
22	VSS	58	TEST	94	DMMDATA[7]/nMIBSPI5ENA	130	FRAYTXEN2
23	nMIBSPI1CS[0]	59	AD2EVT	95	DMMDATA[8]/MIBSPI5SIMO[0]	131	FRAYRX2
24	nMIBSPI1CS[1]	60	AD2IN[0]	96	DMMDATA[9]/ MIBSPI5SIMO[1]	132	VCCIO
25	nMIBSPI1CS[2]	61	AD2IN[1]	97	DMMDATA[10]/MIBSPI5SIMO[2]	133	VSSIO
26	NHET[13]	62	AD2IN[2]	98	DMMDATA[11]/MIBSPI5SIMO[3]	134	GIO[1]/INT[1]
27	GIO[6]/INT[6]	63	AD2IN[3]	99	DMMDATA[12]/MIBSPI5SOMI[0]	135	VCC
28	nPORRST	64	VSSAD	100	DMMDATA[13]/ MIBSPI5SOMI[1]	136	VSS
29	nTRST	65	ADREFLO	101	DMMDATA[14]/ MIBSPI5SOMI[2]	137	NHET[30]
30	TCK	66	ADDREFHI	102	DMMDATA[15]/ MIBSPI5SOMI[3]	138	NHET[14]
31	VCC	67	VCCAD	103	VSS	139	LIN2TX
32	VSS	68	ADSIN[15]	104	VCC	140	LIN2RX
33	TDO	69	ADSIN[14]	105	NHET[0]	141	GIO[2]/INT[2]
34	TDI	70	ADSIN[13]	106	NHET[28]	142	NHET[16]
35	RTCK	71	ADSIN[12]	107	VSSIO	143	nERROR
36	TMS	72	ADSIN[11]	108	VCCIO	144	GIO[3]/INT[3]

FIGURE 2. Terminal connections.

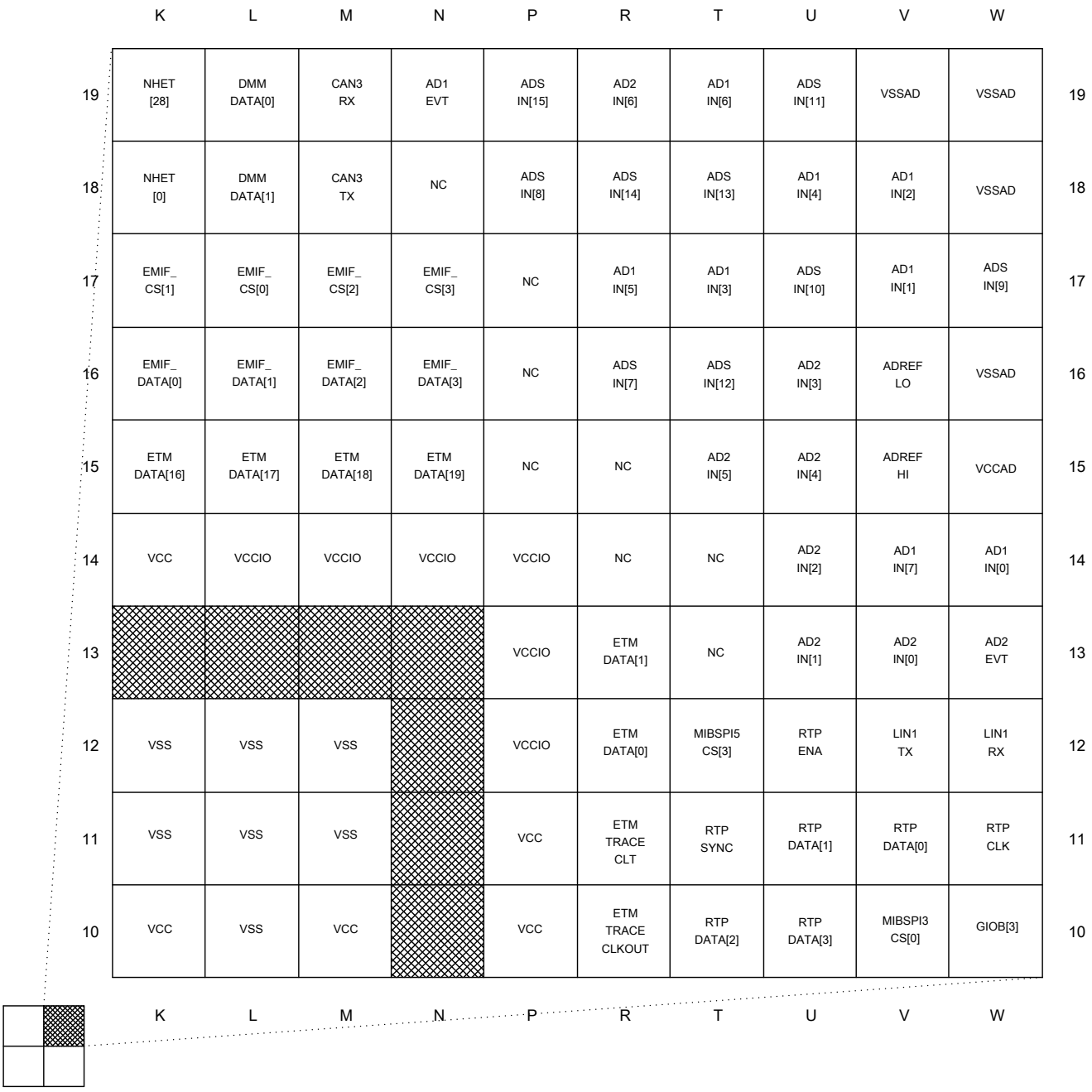
Case Y



	A	B	C	D	E	F	G	H	J	K	L	
19	VSS	VSS	TMS	NHET [10]	MIBSPI5 CS[0]	MIBSPI1 SIMO	MIBSPI1 ENA	MIBSPI1 CLK	MIBSPI5 SIMO[0]	NHET [28]	DMM DATA[0]	19
18	VSS	TCK	TDO	$\overline{\text{TRST}}$	NHET [08]	MIBSPI1 CLK	MIBSP15 SOMI	MIBSPI5 ENA	MIBSPI5 SOMI[0]	NHET [0]	DMM DATA[1]	18
17	TDI	$\overline{\text{RST}}$	EMIF_ ADDR[21]	EMIF _WE	MIBSPI5 SOM[1]	DMM CLK	MIBSPI5 SIMO[3]	MIBSPI5 SIMO[2]	NHET [31]	EMIF_ CS[1]	EMIF_ CS[0]	17
16	RTCK	FRAY TXEN1	EMIF_ ADDR[20]	EMIF_ BA[1]	MIBSPI5 SIMO[1]	DMM ENA	MIBSPI5 SOMI[3]	MIBSPI5 SOMI[2]	DMM SYNC	EMIF_ DATA[0]	EMIF_ DATA[1]	16
15	FRAY RX1	FRAY TX1	EMIF_ ADDR[19]	EMIF_ ADDR[18]	ETM DATA[06]	ETM DATA[05]	ETM DATA[04]	ETM DATA[03]	ETM DATA[02]	ETM DATA[16]	ETM DATA[17]	15
14	NHET [26]	$\overline{\text{ERROR}}$	EMIF_ ADDR[17]	EMIF_ ADDR[16]	ETM DATA[07]	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	14
13	NHET [17]	NHET [19]	EMIF_ ADDR[15]	EMIF_ BA[0]	ETM DATA[12]	VCCIO						13
12	ECLK	NHET [04]	EMIF_ ADDR[14]	EMIF_ OE	ETM DATA[13]	VCCIO		VSS	VSS	VCC	VSS	12
11	NHET [14]	NHET [30]	EMIF_ ADDR[13]	EMIF_ DQM[1]	ETM DATA[14]	VCCIO		VSS	VSS	VSS	VSS	11
10	CAN1 TX	CAN1 RX	EMIF_ ADDR[12]	EMIF_ DQM[0]	ETM DATA[15]	VCC		VCC	VSS	VSS	VSS	10
	A	B	C	D	E	F	G	H	J	K	L	

FIGURE 2. Terminal connections - Continued.

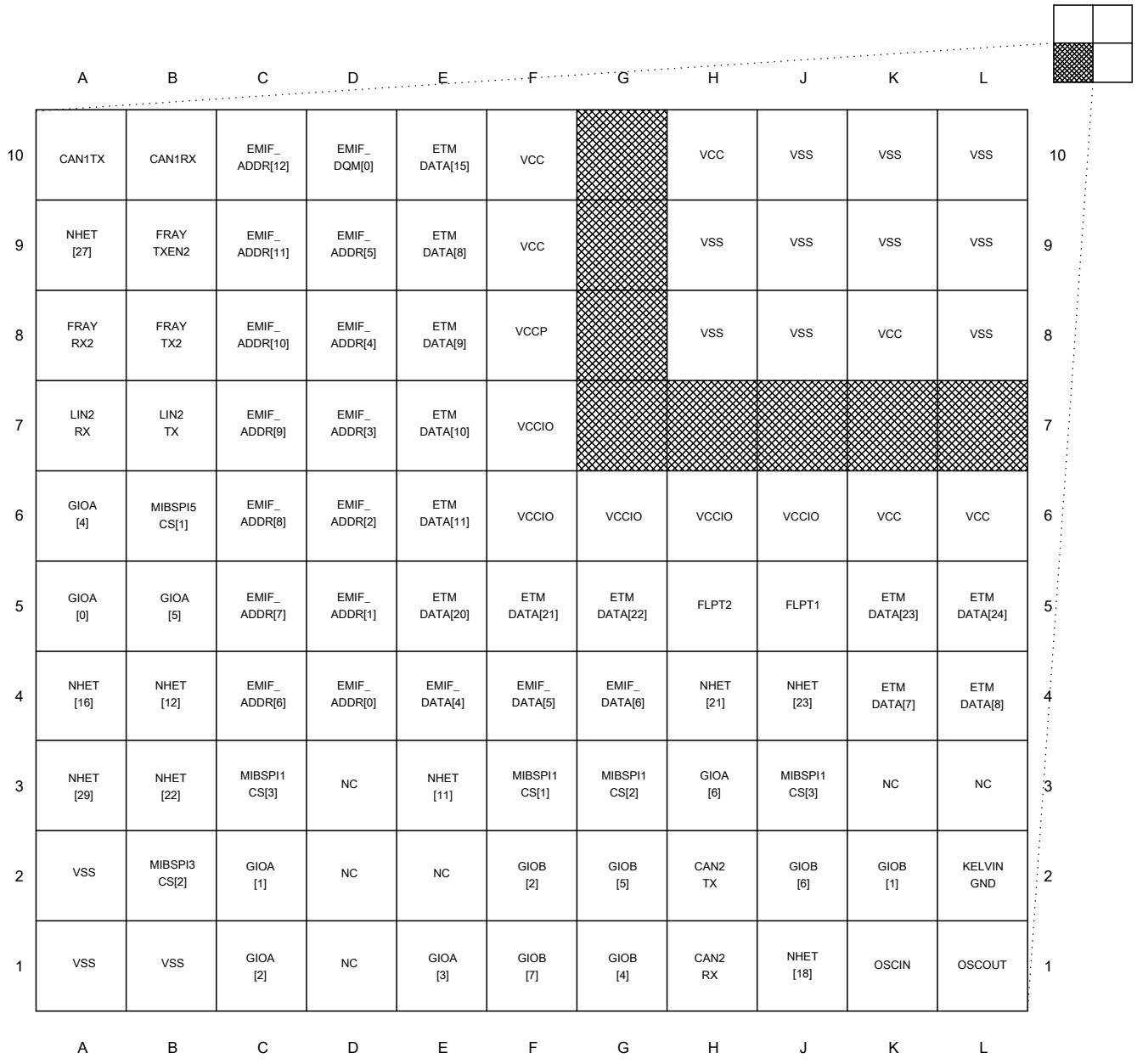
Case Y – Continued.



	K	L	M	N	P	R	T	U	V	W	
19	NHET [28]	DMM DATA[0]	CAN3 RX	AD1 EVT	ADS IN[15]	AD2 IN[6]	AD1 IN[6]	ADS IN[11]	VSSAD	VSSAD	19
18	NHET [0]	DMM DATA[1]	CAN3 TX	NC	ADS IN[8]	ADS IN[14]	ADS IN[13]	AD1 IN[4]	AD1 IN[2]	VSSAD	18
17	EMIF_ CS[1]	EMIF_ CS[0]	EMIF_ CS[2]	EMIF_ CS[3]	NC	AD1 IN[5]	AD1 IN[3]	ADS IN[10]	AD1 IN[1]	ADS IN[9]	17
16	EMIF_ DATA[0]	EMIF_ DATA[1]	EMIF_ DATA[2]	EMIF_ DATA[3]	NC	ADS IN[7]	ADS IN[12]	AD2 IN[3]	ADREF LO	VSSAD	16
15	ETM DATA[16]	ETM DATA[17]	ETM DATA[18]	ETM DATA[19]	NC	NC	AD2 IN[5]	AD2 IN[4]	ADREF HI	VCCAD	15
14	VCC	VCCIO	VCCIO	VCCIO	VCCIO	NC	NC	AD2 IN[2]	AD1 IN[7]	AD1 IN[0]	14
13					VCCIO	ETM DATA[1]	NC	AD2 IN[1]	AD2 IN[0]	AD2 EVT	13
12	VSS	VSS	VSS		VCCIO	ETM DATA[0]	MIBSPI5 CS[3]	RTP ENA	LIN1 TX	LIN1 RX	12
11	VSS	VSS	VSS		VCC	ETM TRACE CLT	RTP SYNC	RTP DATA[1]	RTP DATA[0]	RTP CLK	11
10	VCC	VSS	VCC		VCC	ETM TRACE CLKOUT	RTP DATA[2]	RTP DATA[3]	MIBSPI3 CS[0]	GIOB[3]	10
	K	L	M	N	P	R	T	U	V	W	

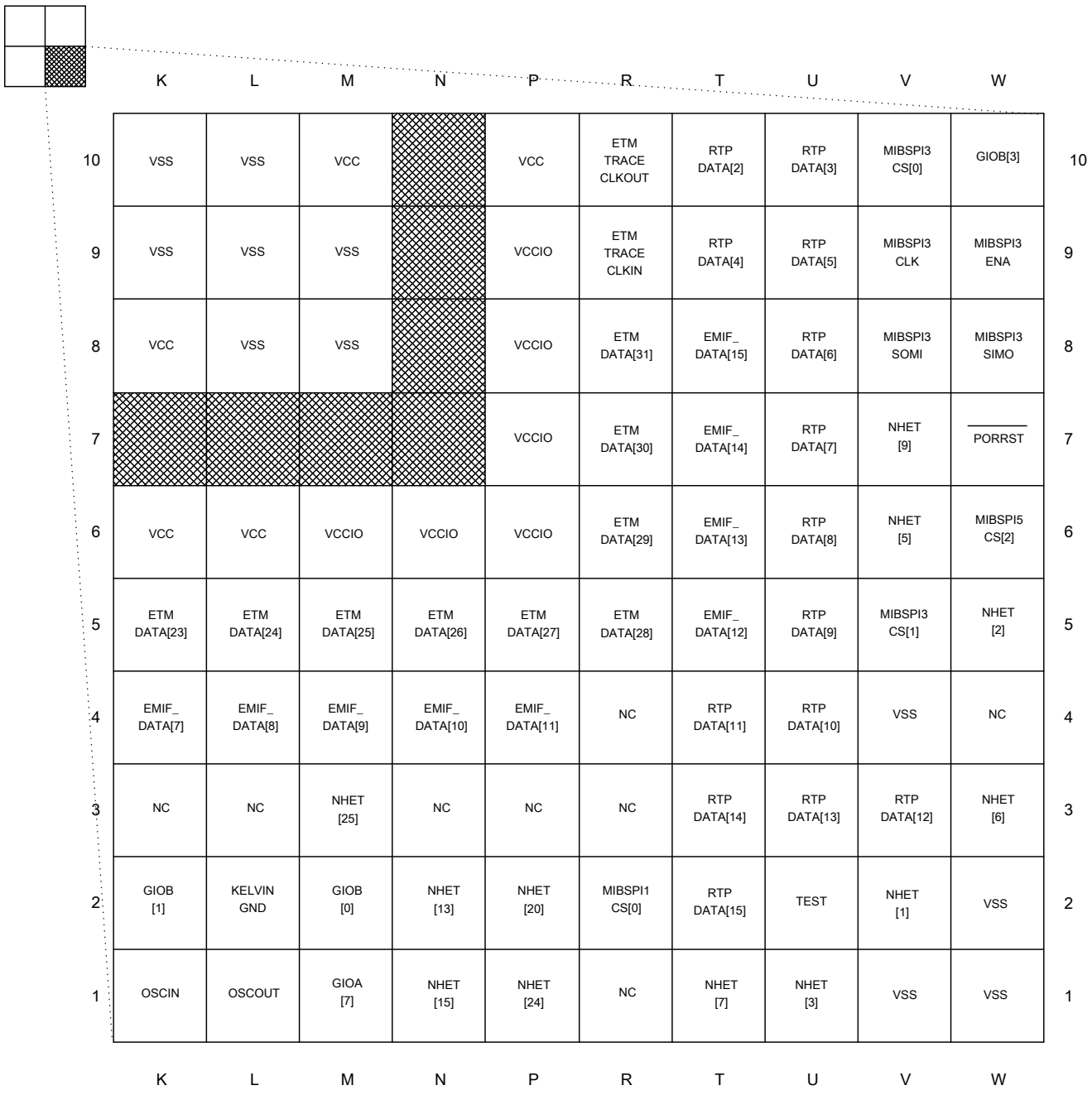
FIGURE 2. Terminal connections - Continued.

Case Y – Continued.



	A	B	C	D	E	F	G	H	J	K	L
10	CAN1TX	CAN1RX	EMIF_ ADDR[12]	EMIF_ DQM[0]	ETM DATA[15]	VCC		VCC	VSS	VSS	VSS
9	NHET [27]	FRAY TXEN2	EMIF_ ADDR[11]	EMIF_ ADDR[5]	ETM DATA[8]	VCC		VSS	VSS	VSS	VSS
8	FRAY RX2	FRAY TX2	EMIF_ ADDR[10]	EMIF_ ADDR[4]	ETM DATA[9]	VCCP		VSS	VSS	VCC	VSS
7	LIN2 RX	LIN2 TX	EMIF_ ADDR[9]	EMIF_ ADDR[3]	ETM DATA[10]	VCCIO					
6	GIOA [4]	MIBSPI5 CS[1]	EMIF_ ADDR[8]	EMIF_ ADDR[2]	ETM DATA[11]	VCCIO	VCCIO	VCCIO	VCCIO	VCC	VCC
5	GIOA [0]	GIOA [5]	EMIF_ ADDR[7]	EMIF_ ADDR[1]	ETM DATA[20]	ETM DATA[21]	ETM DATA[22]	FLPT2	FLPT1	ETM DATA[23]	ETM DATA[24]
4	NHET [16]	NHET [12]	EMIF_ ADDR[6]	EMIF_ ADDR[0]	EMIF_ DATA[4]	EMIF_ DATA[5]	EMIF_ DATA[6]	NHET [21]	NHET [23]	ETM DATA[7]	ETM DATA[8]
3	NHET [29]	NHET [22]	MIBSPI1 CS[3]	NC	NHET [11]	MIBSPI1 CS[1]	MIBSPI1 CS[2]	GIOA [6]	MIBSPI1 CS[3]	NC	NC
2	VSS	MIBSPI3 CS[2]	GIOA [1]	NC	NC	GIOB [2]	GIOB [5]	CAN2 TX	GIOB [6]	GIOB [1]	KELVIN GND
1	VSS	VSS	GIOA [2]	NC	GIOA [3]	GIOB [7]	GIOB [4]	CAN2 RX	NHET [18]	OSCIN	OSCOUT

FIGURE 2. Terminal connections - Continued.



	K	L	M	N	P	R	T	U	V	W	
10	VSS	VSS	VCC		VCC	ETM TRACE CLKOUT	RTP DATA[2]	RTP DATA[3]	MIBSPI3 CS[0]	GIOB[3]	10
9	VSS	VSS	VSS		VCCIO	ETM TRACE CLKIN	RTP DATA[4]	RTP DATA[5]	MIBSPI3 CLK	MIBSPI3 ENA	9
8	VCC	VSS	VSS		VCCIO	ETM DATA[31]	EMIF_ DATA[15]	RTP DATA[6]	MIBSPI3 SOMI	MIBSPI3 SIMO	8
7					VCCIO	ETM DATA[30]	EMIF_ DATA[14]	RTP DATA[7]	NHET [9]	$\overline{\text{PORRST}}$	7
6	VCC	VCC	VCCIO	VCCIO	VCCIO	ETM DATA[29]	EMIF_ DATA[13]	RTP DATA[8]	NHET [5]	MIBSPI5 CS[2]	6
5	ETM DATA[23]	ETM DATA[24]	ETM DATA[25]	ETM DATA[26]	ETM DATA[27]	ETM DATA[28]	EMIF_ DATA[12]	RTP DATA[9]	MIBSPI3 CS[1]	NHET [2]	5
4	EMIF_ DATA[7]	EMIF_ DATA[8]	EMIF_ DATA[9]	EMIF_ DATA[10]	EMIF_ DATA[11]	NC	RTP DATA[11]	RTP DATA[10]	VSS	NC	4
3	NC	NC	NHET [25]	NC	NC	NC	RTP DATA[14]	RTP DATA[13]	RTP DATA[12]	NHET [6]	3
2	GIOB [1]	KELVIN GND	GIOB [0]	NHET [13]	NHET [20]	MIBSPI1 CS[0]	RTP DATA[15]	TEST	NHET [1]	VSS	2
1	OSCIN	OSCOUT	GIOA [7]	NHET [15]	NHET [24]	NC	NHET [7]	NHET [3]	VSS	VSS	1
	K	L	M	N	P	R	T	U	V	W	

FIGURE 2. Terminal connections - Continued.

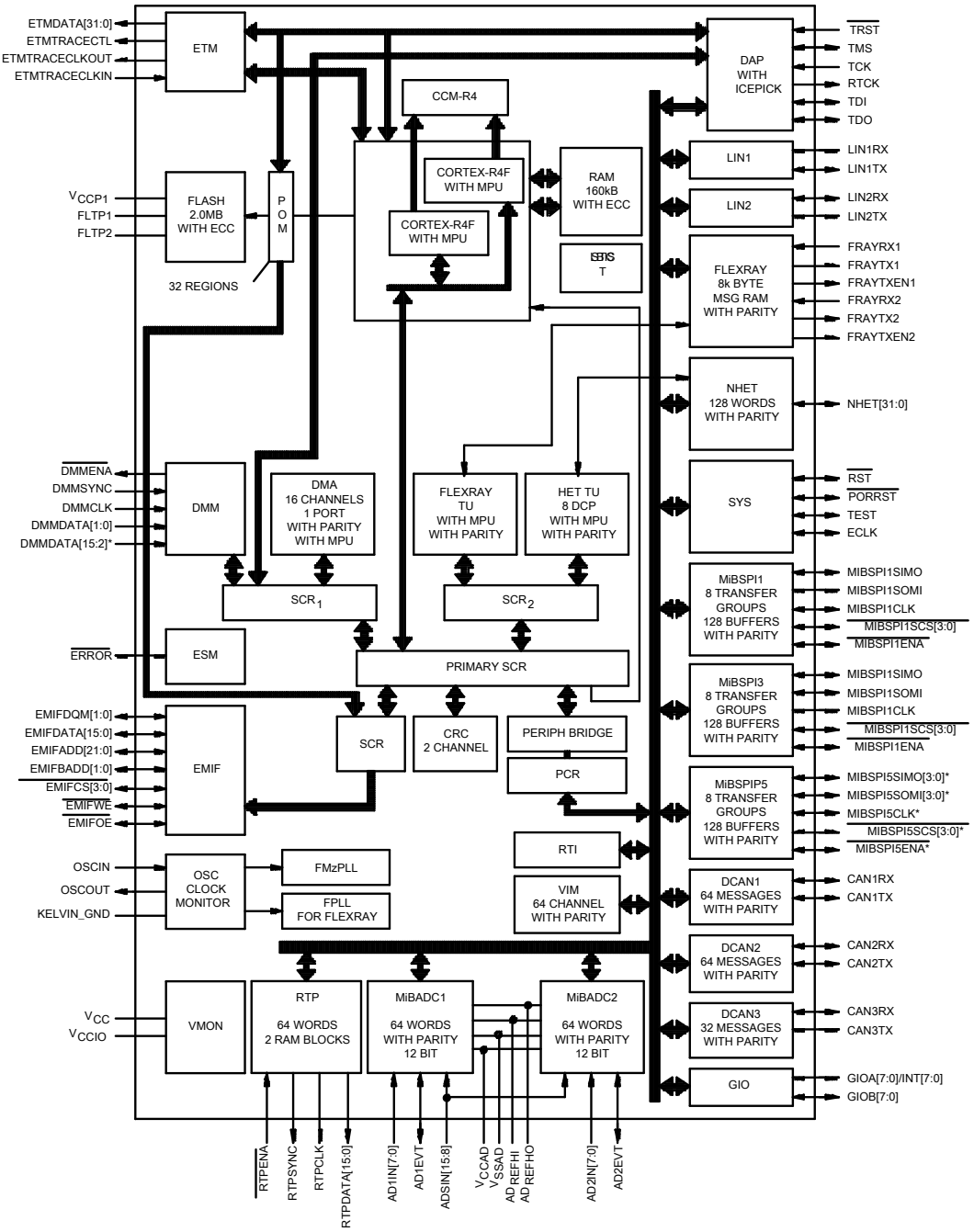


FIGURE 3. Functional block diagram.

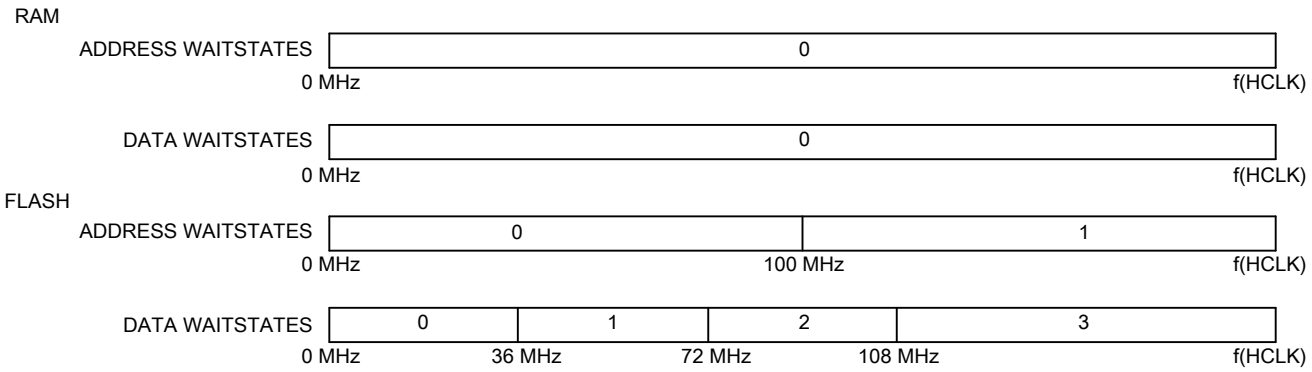


FIGURE 4. Wait states.

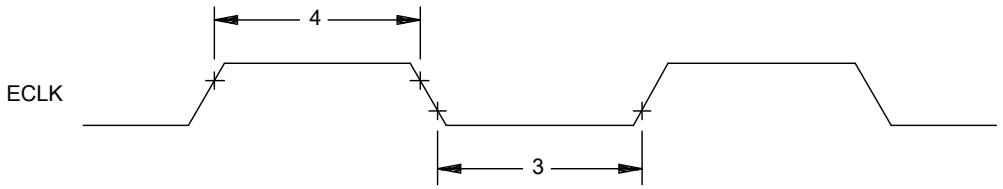


FIGURE 5. ECLK timing diagram.

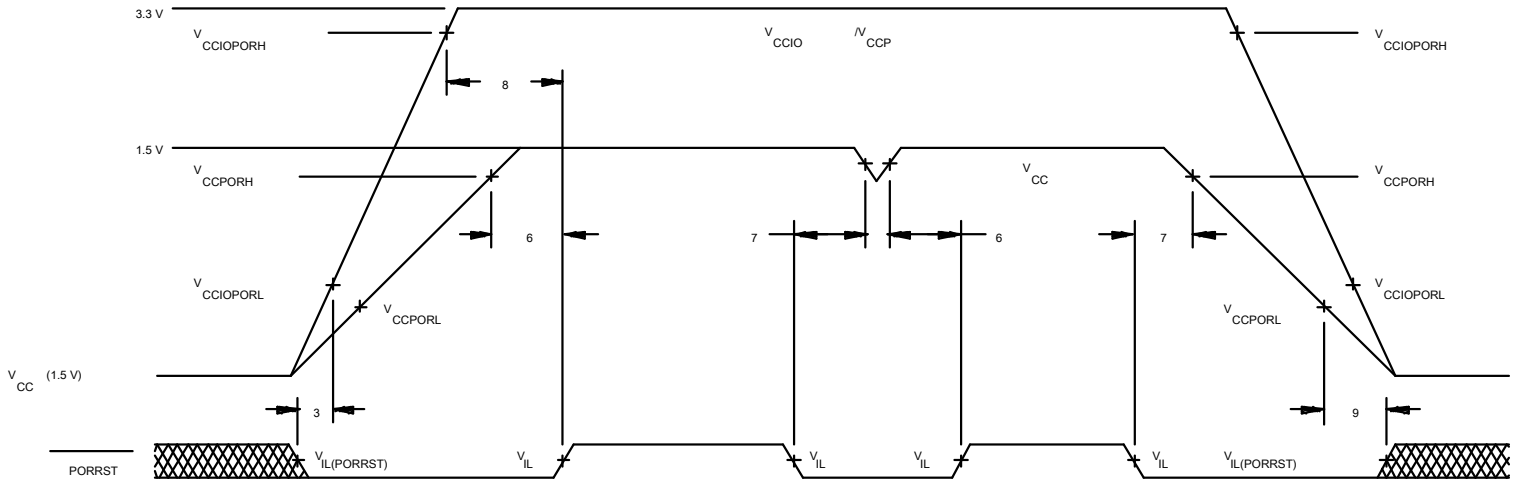


FIGURE 6. PORRST timing diagram.

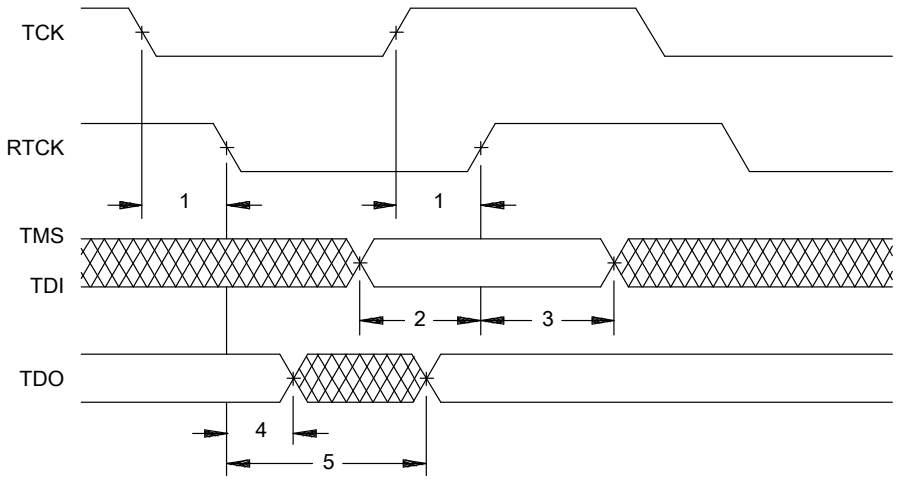


FIGURE 7. JTAG timing.

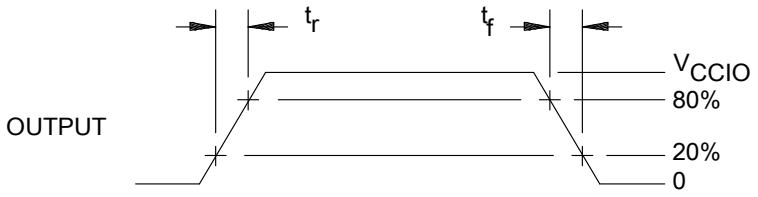


FIGURE 8. CMOS level outputs.

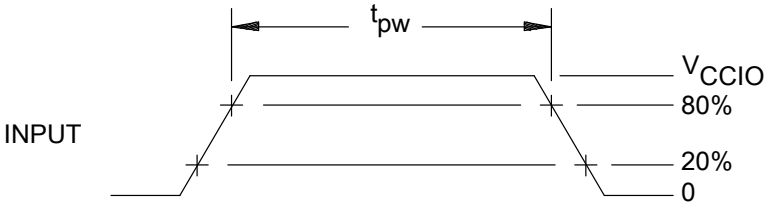


FIGURE 9. CMOS level inputs.

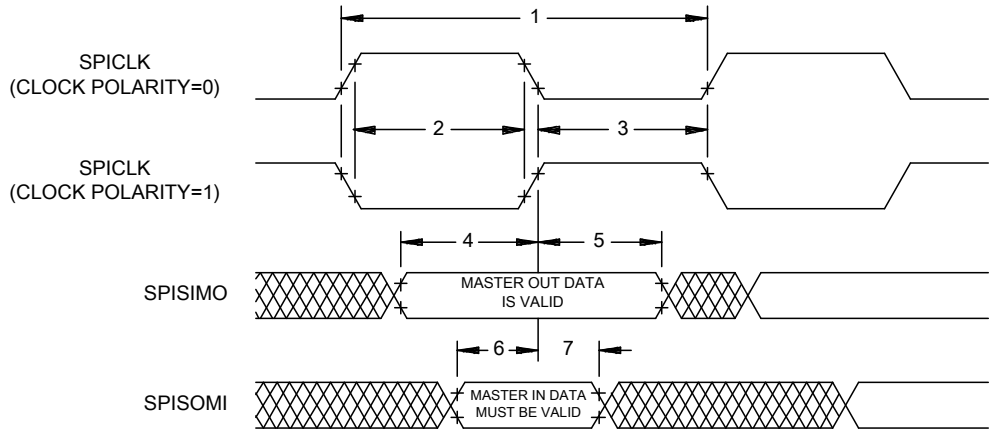


FIGURE 10. SPI Master mode external timing (Clock Phase = 0).

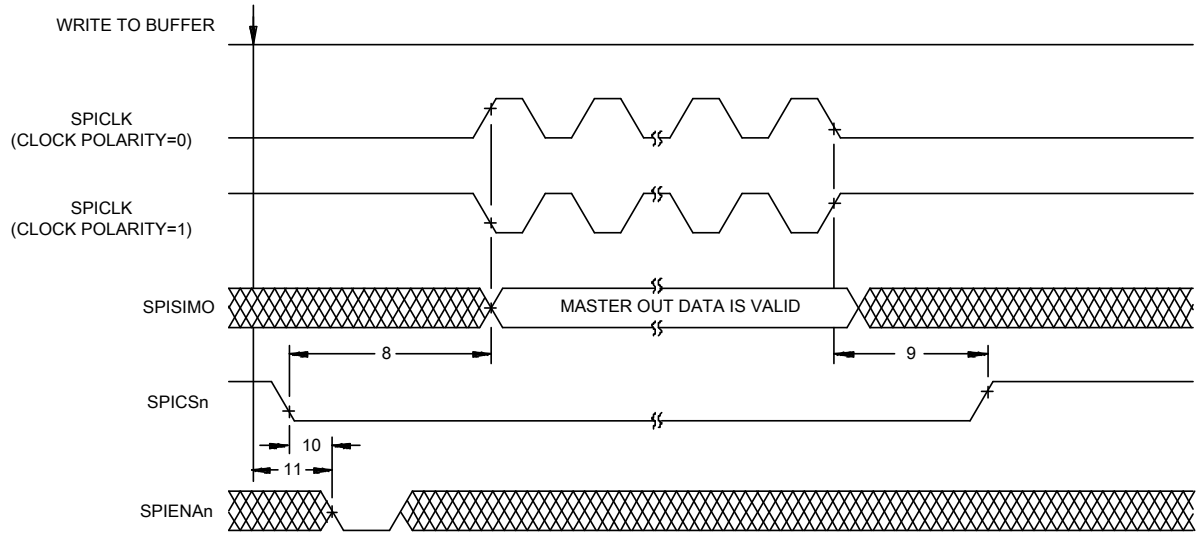


FIGURE 11. SPI Master mode chip select timing (Clock Phase = 0).

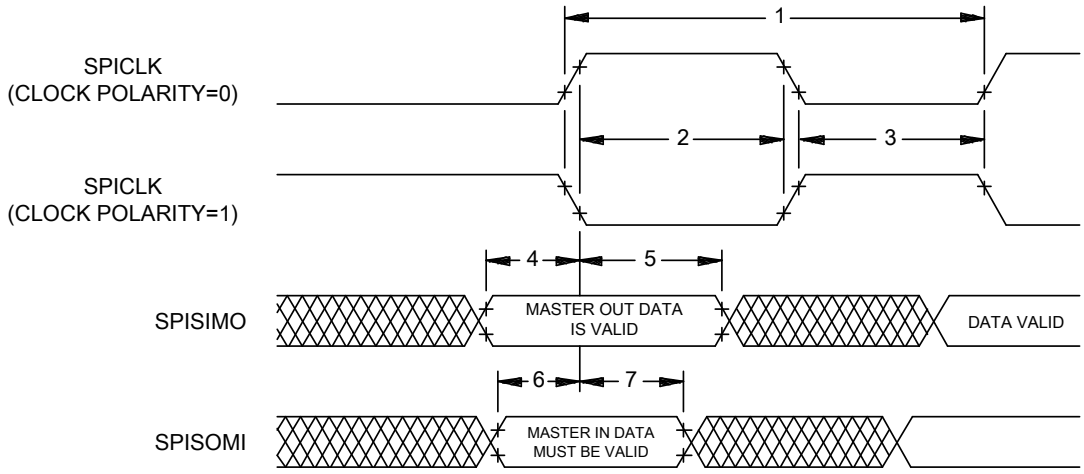


FIGURE 12. SPI Master mode external timing (Clock Phase = 1).

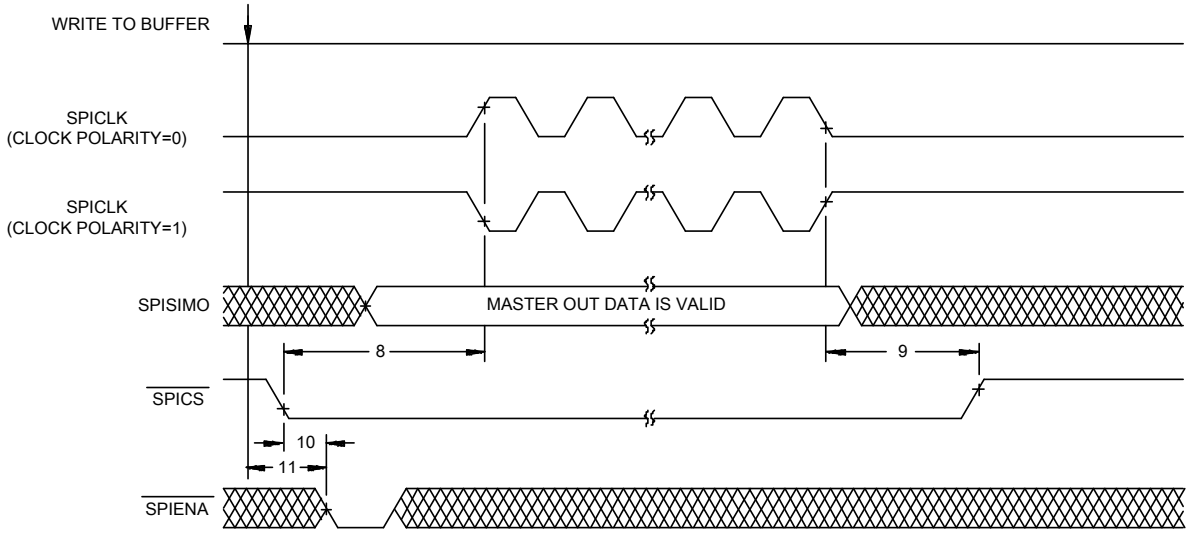


FIGURE 13. SPI Master mode chip select timing (Clock Phase = 1).

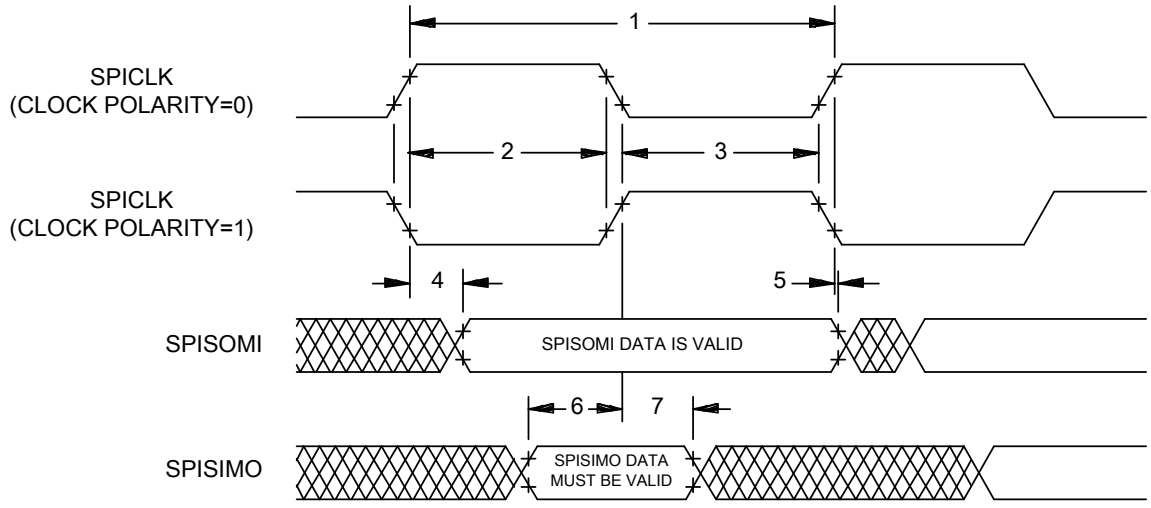


FIGURE 14. SPI Slave mode external timing (Clock Phase = 0).

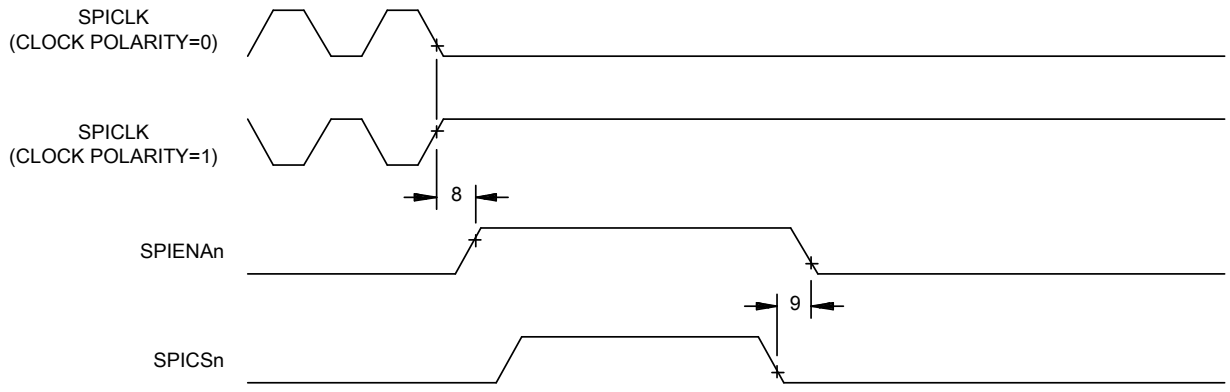


FIGURE 15. SPI Slave mode chip select timing (Clock Phase = 0).

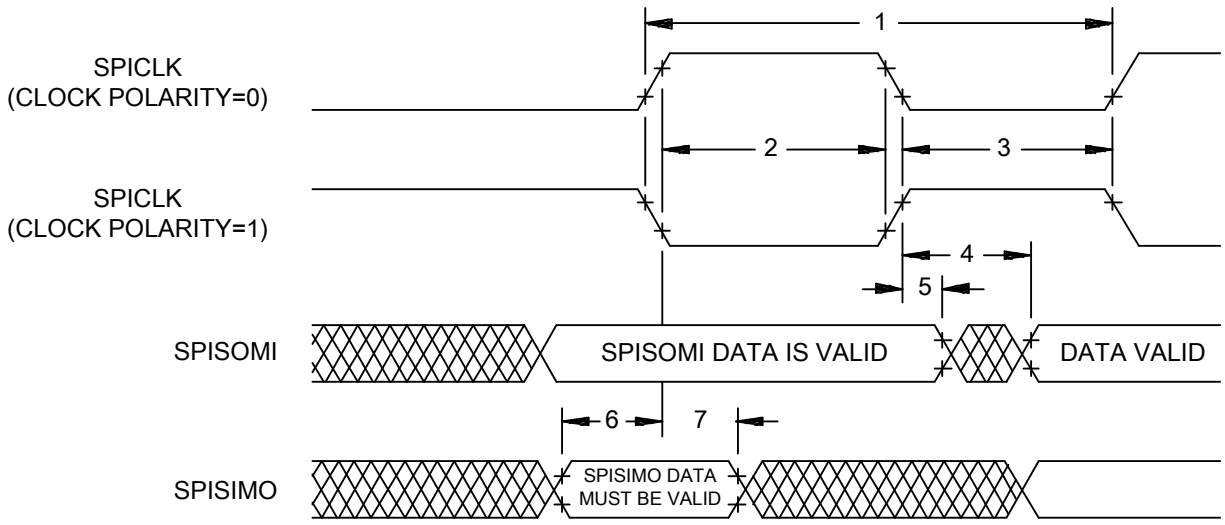


FIGURE 16. SPI Slave mode external timing (Clock Phase = 1).

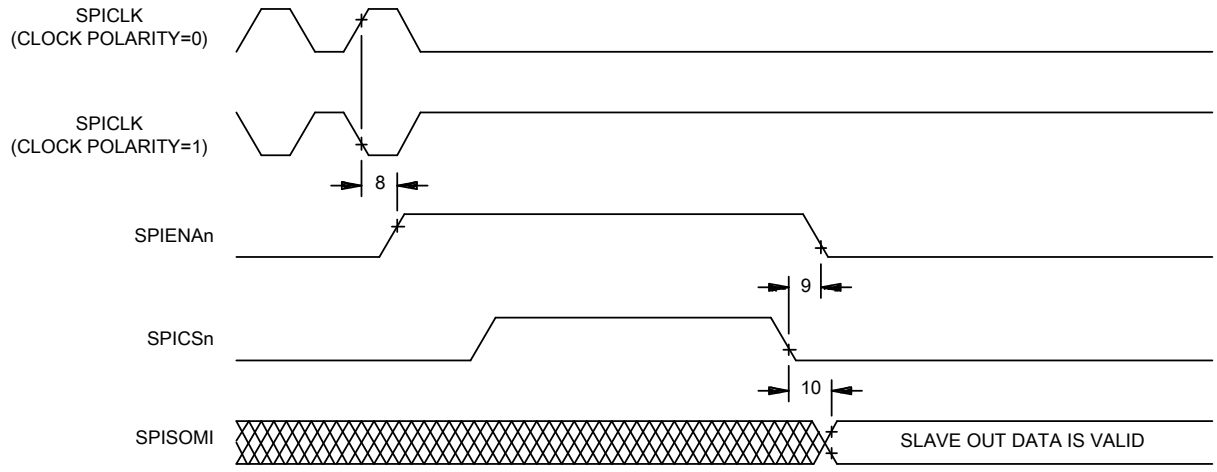


FIGURE 17. SPI Slave mode chip select timing (Clock Phase = 1).

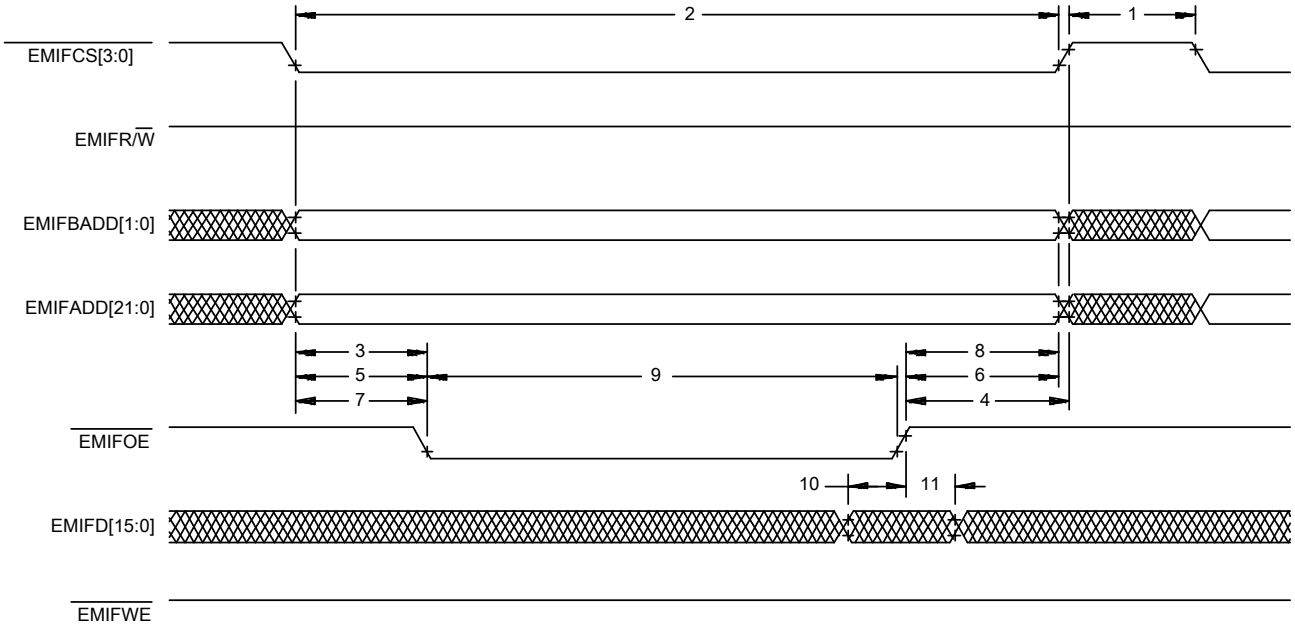


FIGURE 18. Asynchronous memory Read timing for EMIF.

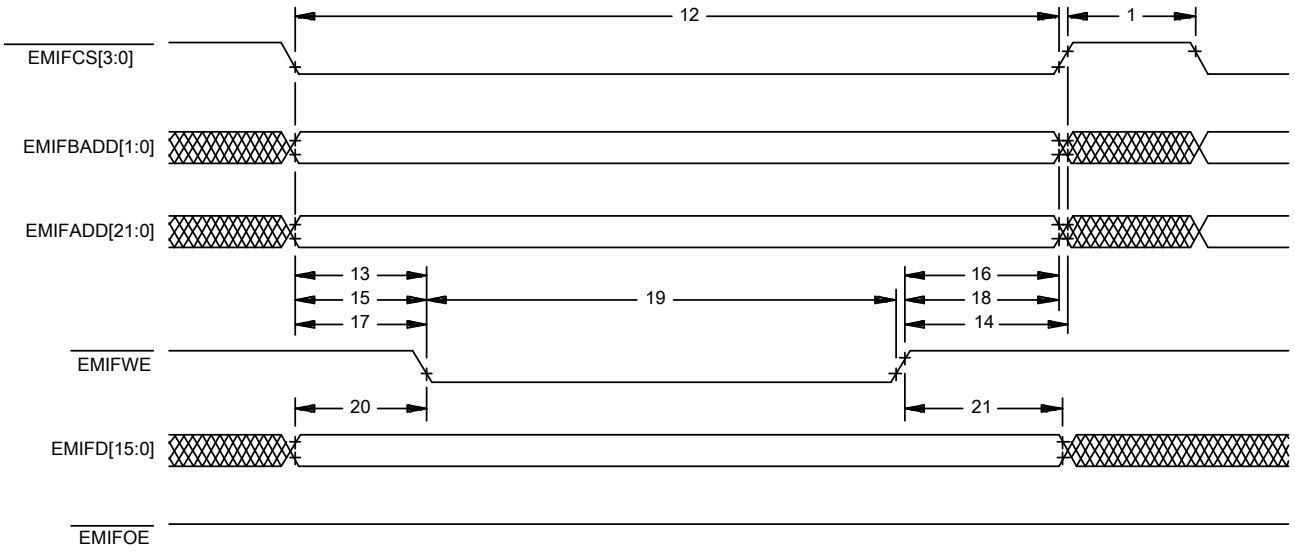


FIGURE 19. Asynchronous memory Write timing for EMIF.

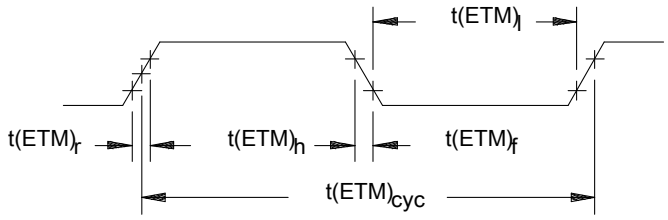


FIGURE 20. ETMTRACECLK timing.

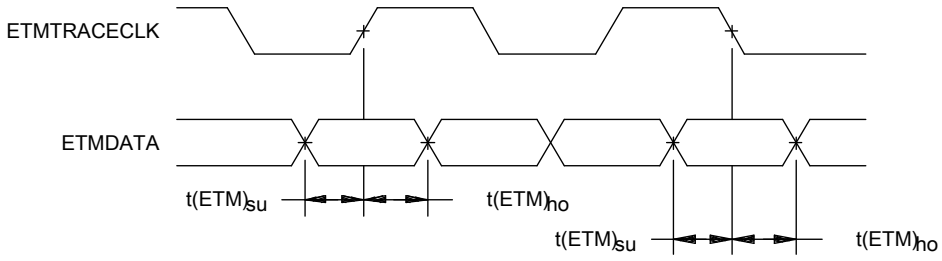


FIGURE 21. ETMDATA timing.

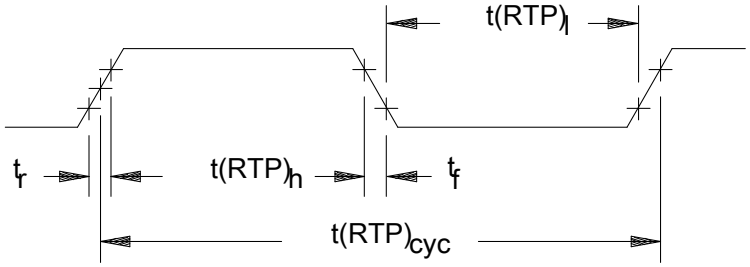


FIGURE 22. RTPCLK timing.

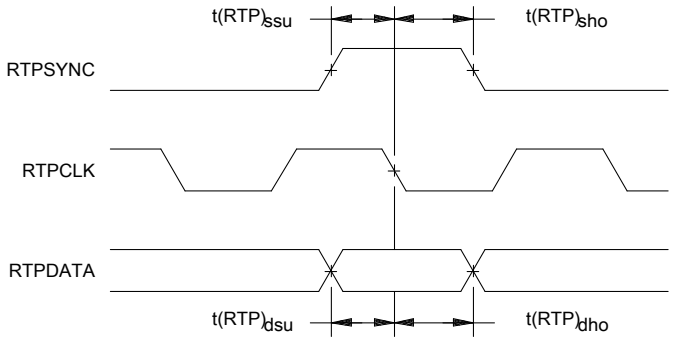


FIGURE 23. RTPDATA timing.

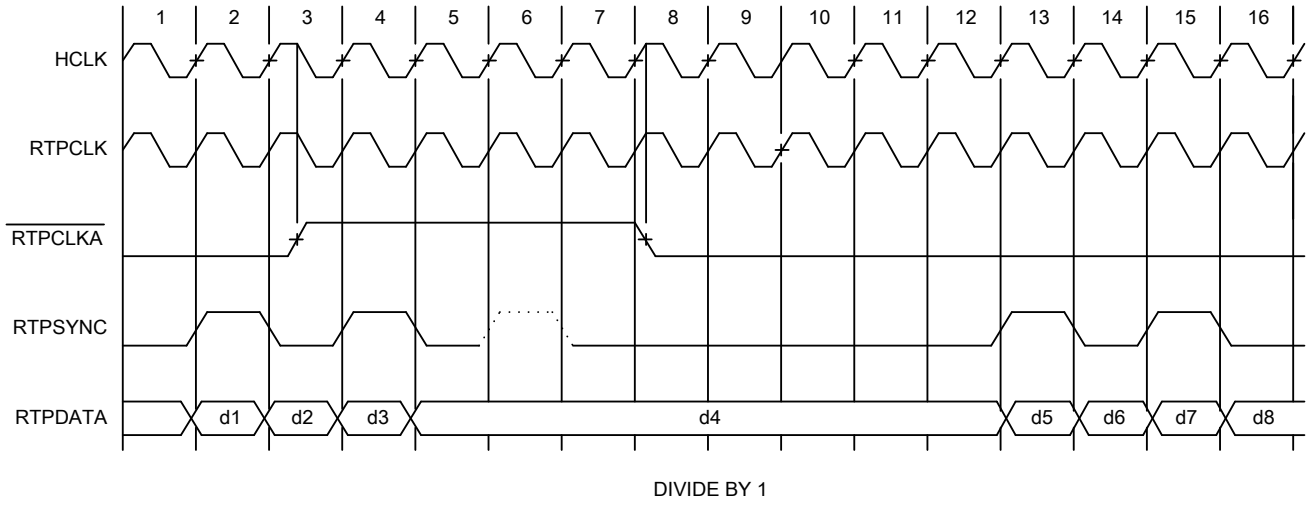


FIGURE 24. RTPENABLE timing.

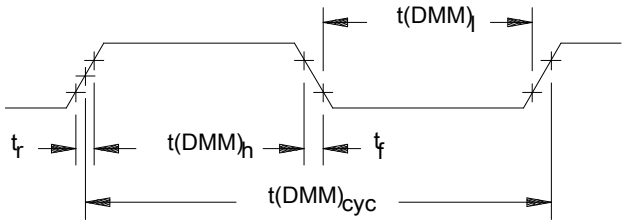


FIGURE 25. DMMCLK timing.

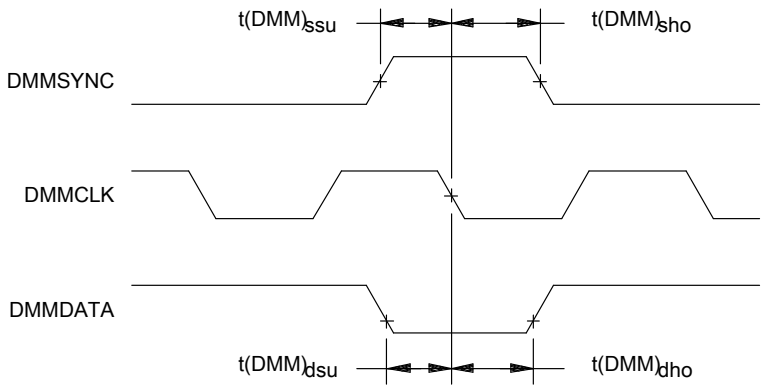


FIGURE 26. DMMDATA timing.

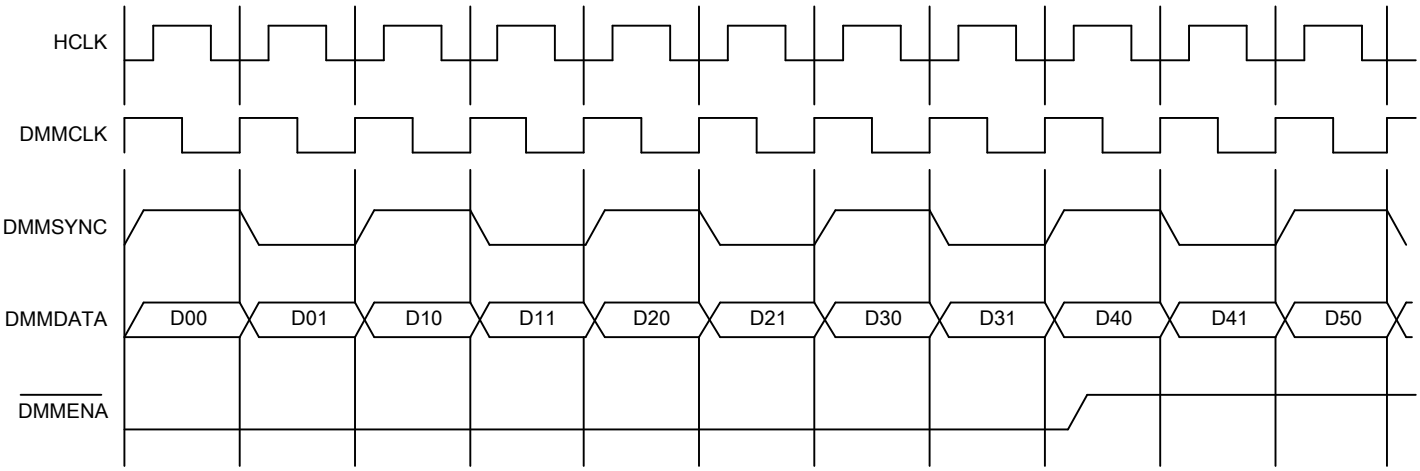


FIGURE 27. $\overline{\text{DMMENA}}$ timing

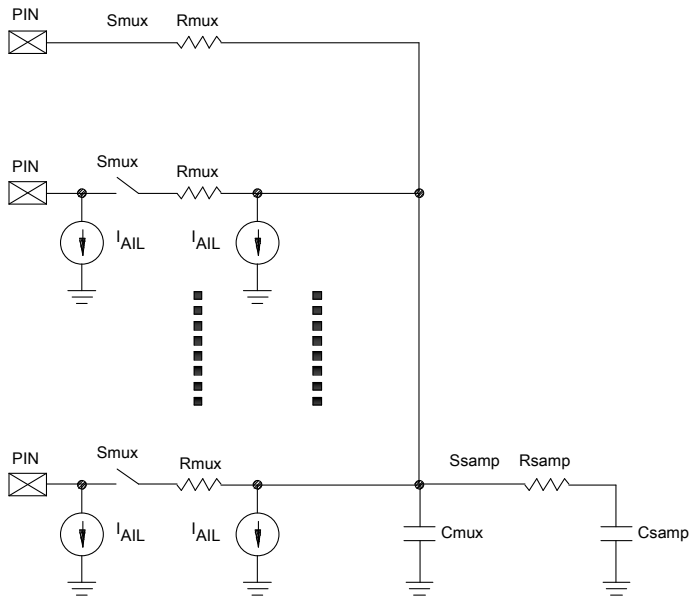


FIGURE 28. MibADC input equivalent circuit.

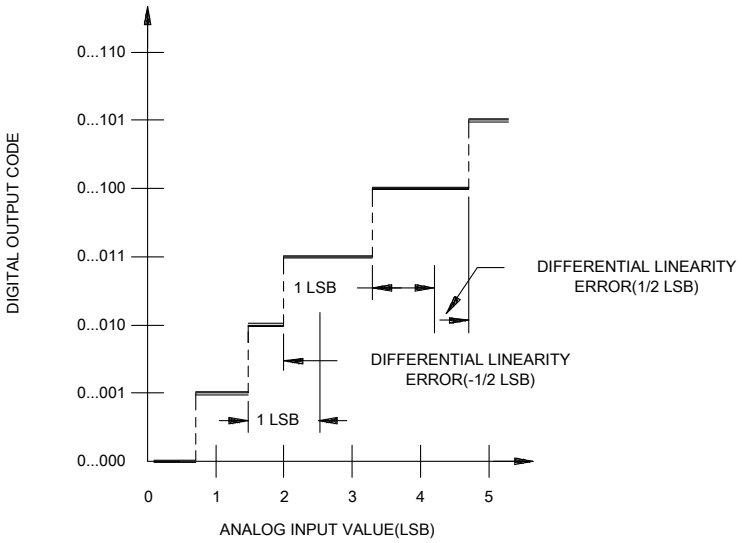


FIGURE 29. Differential Nonlinearity (DNL).

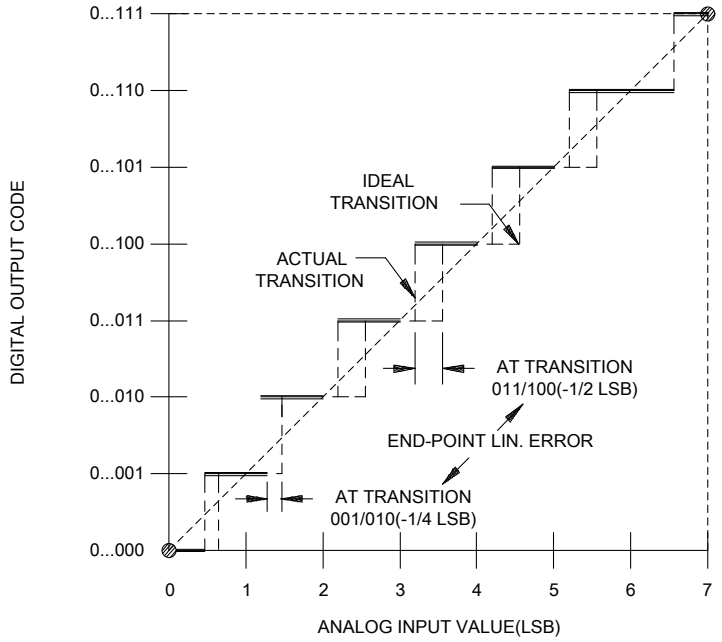


FIGURE 30. Integral Nonlinearity (INL) error.

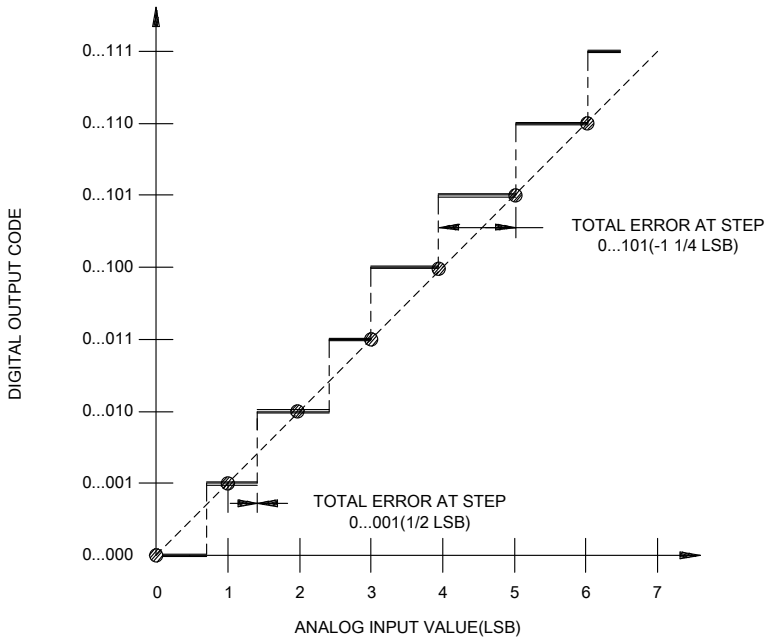


FIGURE 31. Absolute accuracy (Total) error.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12622-01XE	01295	S5LS20206ASPGEMEP
V62/12622-01YF 2/	01295	S5LS20206ASGWTMEP
V62/12622-02XE	01295	S5LS20216ASPGEMEP
V62/12622-02YF 2/	01295	S5LS20216ASGWTMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Devices listed on this drawing are supplied to lead finish "F". The solder ball material contains compositions of Sn= 63%, Pb=34.5%. Ag- 2.0% and Sb =0.5%.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243