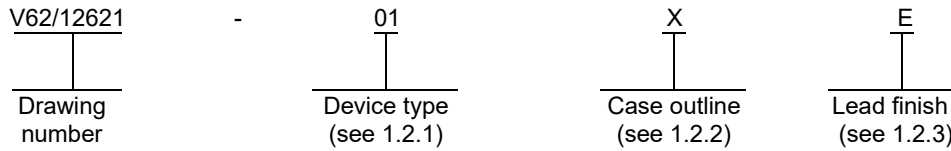




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontrollers microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	MSP430G2231-EP	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Voltage applied at V <sub>CC</sub> to V <sub>SS</sub> .....	-0.3 V to 4.1 V
Voltage applied to any pin .....	-0.3 V to V <sub>CC</sub> +0.3 V 2/
Diode current at any device terminal .....	±2 mA
Storage temperature: 3/	
Unprogrammed device .....	-55°C to 150°C
Programmed device .....	-55°C to 150°C

1.4 Recommended operating conditions.

Supply voltage, (V <sub>CC</sub> ):	
During program execution .....	1.8 V to 3.6 V
During flash program/erase .....	2.2 V to 3.6 V
Supply voltage, (V <sub>SS</sub> ) .....	0 V
Operating free air temperature, (T <sub>A</sub> ) .....	-40°C to 125°C
Processor frequency (Maximum MCLK frequency) 4/ 5/	
V <sub>CC</sub> = 1.8 V, Duty cycle = 50% ±10% .....	dc to 6 MHz
V <sub>CC</sub> = 2.7 V, Duty cycle = 50% ±10% .....	dc to 12 MHz
V <sub>CC</sub> = 3.3 V, Duty cycle = 50% ±10% .....	dc to 16 MHz

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- J-STD-020 – Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Copies of these documents are available online at <https://www.jedec.org>.)

- 
- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
  - 2/ All voltage values referenced to V<sub>SS</sub>. The JTAG fuse blow voltage, V<sub>FB</sub> is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse..
  - 3/ Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
  - 4/ The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
  - 5/ Modules might have different maximum input clock specification. See the specification from the manufacturer data sheet.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Safe operating area. The safe operating area shall be as shown in figure 5.

3.5.6 POR/Brownout Reset (BOR) vs Supply voltage. The POR/Brownout Reset (BOR) vs Supply voltage shall be as shown in figure 6.

3.5.7 V<sub>CC(drop)</sub> level with a Square voltage drop to generate a POR/Brownout signal. The V<sub>CC(drop)</sub> level with a Square voltage drop to generate a POR/Brownout signal shall be as shown in figure 7.

3.5.8 V<sub>CC(drop)</sub> level with a Triangle voltage drop to generate a POR/Brownout signal. The V<sub>CC(drop)</sub> level with a Triangle voltage drop to generate a POR/Brownout signal shall be as shown in figure 8.

3.5.9 DCO wake-up time from LPM3/4 vs DCO frequency. The DCO wake-up time from LPM3/4 vs DCO frequency waveforms shall be as shown in figure 9.

3.5.10 USI low level output voltage vs output current. The USI low level output voltage vs output current shall be as shown in figure 10.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/ 4/	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>Active mode supply current into V<sub>CC</sub> excluding external current</b>							
Active mode (AM) current (1 MHz)	I <sub>AM, 1MHz</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 1 MHz, f <sub>ACLK</sub> = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 0, SCG0 = 0 SCG1 = 0, OSCOFF = 0		2.2 V	220 TYP		μA
				3 V		390	μA
<b>Low power mode Supply current (into V<sub>CC</sub>) Excluding external current</b>							
Low power mode 0 (LPM0) current <u>5/</u>	I <sub>LPM0, 1MHz</sub>	f <sub>MCLK</sub> = 0 MHz, f <sub>SMCLK</sub> = f <sub>DCO</sub> = 1 MHz, f <sub>ACLK</sub> = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V	65 TYP		μA
Low power mode 2 (LPM2) current <u>6/</u>	I <sub>LPM2</sub>	f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz, f <sub>DCO</sub> = 1 MHz, f <sub>ACLK</sub> = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V	22 TYP		μA
			125°C			46	μA
Low power mode 3 (LPM3) current <u>6/</u>	I <sub>LPM3, LFXT1</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz, f <sub>ACLK</sub> = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		1.5	μA
			125°C			21	μA
Low power mode 3 (LPM3) current <u>6/</u>	I <sub>LPM3, VLO</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz, f <sub>ACLK</sub> = from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	μA
			125°C			9.3	μA
Low power mode 4 (LPM4) current <u>7/</u>	I <sub>LPM4</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz, f <sub>ACLK</sub> = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.5	μA
			85°C			1.5	μA
			125°C			7.1	μA

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>Schmitt Trigger inputs (Port Px) 42/</b>						
Positive going input threshold voltage	V <sub>IT+</sub>			0.45 V <sub>CC</sub>	0.75 V <sub>CC</sub>	V
			3 V	1.35	2.25	V
Negative going input threshold voltage	V <sub>IT-</sub>			0.25 V <sub>CC</sub>	0.55 V <sub>CC</sub>	V
			3 V	0.75	1.65	V
Input voltage hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )	V <sub>hys</sub>		3 V	0.3	1.0	V
Pullup/pulldown resistor	R <sub>Pull</sub>	For pullup: V <sub>IN</sub> = V <sub>SS</sub> For pulldown: V <sub>IN</sub> = V <sub>CC</sub>	3 V	20	50	kΩ
Input capacitance	C <sub>I</sub>	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>		5 TYP		pF
<b>Leakage current (Port Px)</b>						
High impedance leakage current	I <sub>Ikg(Px,y)</sub>	T <sub>A</sub> = 125°C 8/ 9/	3 V		+120	nA
		T <sub>A</sub> = -40°C to 105°C 8/ 9/			±50	nA
<b>Outputs (Port Px)</b>						
High level output voltage	V <sub>OH</sub>	I <sub>(OHmax)</sub> = -6 mA 10/	3 V	V <sub>CC</sub> - 0.3	TYP	V
Low level output voltage	V <sub>OL</sub>	I <sub>(OLmax)</sub> = 6 mA 10/	3 V	V <sub>CC</sub> + 0.3	TYP	V
<b>Output frequency (Port Px)</b>						
Port output frequency (with load)	f <sub>Px,y</sub>	Px.y, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ 11/ 12/	3 V	12	TYP	MHz
Clock output frequency	f <sub>Port°CLK</sub>	Px.y, C <sub>L</sub> = 20 pF 12/	3 V	16	TYP	MHz
<b>POR/Brownout reset (BOR) 13/ 42/</b>						
See figure 10	V <sub>CC(start)</sub>	dV <sub>CC</sub> /dt ≤ 3 V/s		0.7 x V <sub>(B_IT-)</sub>	TYP	V
See figure 10 through figure 12	V <sub>(B_IT-)</sub>	dV <sub>CC</sub> /dt ≤ 3 V/s		1.35	TYP	V
See figure 10	V <sub>hys(B_IT-)</sub>	dV <sub>CC</sub> /dt ≤ 3 V/s		130	TYP	mV
See figure 10	t <sub>d(BOR)</sub>				2000	μs
Pulse length needed at $\overline{\text{RST}}$ /NMI pin to accept reset internally	t <sub>(reset)</sub>		2.2V/3 V	2		μs

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>DCO frequency</b>						
Supply voltage	V <sub>CC</sub>	RSELx < 14		1.8	3.6	V
		RSELx = 14		2.2	3.6	V
		RSELx = 15		3.0	3.6	V
DCO frequency (0, 0)	f <sub>DCO(0,0)</sub>	RSELx = 0, DCOx = 0, MDDx = 0	3 V	0.096	TYP	MHz
DCO frequency (0, 3)	f <sub>DCO(0,3)</sub>	RSELx = 0, DCOx = 3, MDDx = 0	3 V	0.12	TYP	MHz
DCO frequency (1, 3)	f <sub>DCO(1,3)</sub>	RSELx = 1, DCOx = 3, MDDx = 0	3 V	0.15	TYP	MHz
DCO frequency (2, 3)	f <sub>DCO(2,3)</sub>	RSELx = 2, DCOx = 3, MDDx = 0	3 V	0.21	TYP	MHz
DCO frequency (3, 3)	f <sub>DCO(3,3)</sub>	RSELx = 3, DCOx = 3, MDDx = 0	3 V	0.30	TYP	MHz
DCO frequency (4, 3)	f <sub>DCO(4,3)</sub>	RSELx = 4, DCOx = 3, MDDx = 0	3 V	0.41	TYP	MHz
DCO frequency (5, 3)	f <sub>DCO(5,3)</sub>	RSELx = 5, DCOx = 3, MDDx = 0	3 V	0.58	TYP	MHz
DCO frequency (6, 3)	f <sub>DCO(6,3)</sub>	RSELx = 6, DCOx = 3, MDDx = 0	3 V	0.80	TYP	MHz
DCO frequency (7, 3)	f <sub>DCO(7,3)</sub>	RSELx = 7, DCOx = 3, MDDx = 0	3 V	0.80	1.50	MHz
DCO frequency (8, 3)	f <sub>DCO(8,3)</sub>	RSELx = 8, DCOx = 3, MDDx = 0	3 V	1.6	TYP	MHz
DCO frequency (9, 3)	f <sub>DCO(9,3)</sub>	RSELx = 9, DCOx = 3, MDDx = 0	3 V	2.3	TYP	MHz
DCO frequency (10, 3)	f <sub>DCO(10,3)</sub>	RSELx = 10, DCOx = 3, MDDx = 0	3 V	3.4	TYP	MHz
DCO frequency (11, 3)	f <sub>DCO(11,3)</sub>	RSELx = 11, DCOx = 3, MDDx = 0	3 V	4.25	TYP	MHz
DCO frequency (12, 3)	f <sub>DCO(12,3)</sub>	RSELx = 12, DCOx = 3, MDDx = 0	3 V	4.3	7.30	MHz
DCO frequency (13, 3)	f <sub>DCO(13,3)</sub>	RSELx = 13, DCOx = 3, MDDx = 0	3 V	7.8	TYP	MHz
DCO frequency (14, 3)	f <sub>DCO(14,3)</sub>	RSELx = 14, DCOx = 3, MDDx = 0	3 V	8.6	13.9	MHz
DCO frequency (15, 3)	f <sub>DCO(15,3)</sub>	RSELx = 15, DCOx = 3, MDDx = 0	3 V	15.25	TYP	MHz
DCO frequency (15, 7)	f <sub>DCO(15,7)</sub>	RSELx = 15, DCOx = 7, MDDx = 0	3 V	21	TYP	MHz
Frequency step between range RSEL and RSEL + 1	S <sub>RSEL</sub>	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	3 V	1.35	TYP	ratio
Frequency step between tap DCO and DCO + 1	S <sub>DCO</sub>	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	3 V	1.08	TYP	ratio
Duty cycle			3 V	50	TYP	%

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>Calibrated DCO frequencies – Tolerance</b> 42/						
1 MHz tolerance over temperature 14/		T <sub>A</sub> = -40°C to 105°C BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	3 V	-3	3	%
1 MHz tolerance over V <sub>CC</sub>		T <sub>A</sub> = 30°C BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	1.8 V to 3.6 V	-3	3	%
1 MHz tolerance overall		T <sub>A</sub> = -40°C to 105°C BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	1.8 V to 3.6 V	-6	6	%
<b>Wake up from Lower Power Models (LPM3/4)</b>						
DCO clock wake up time from LPM3/4 15/	t <sub>DCO,LPM3/4</sub>	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz,	3 V	1.5 P	TYP	µs
CPU wake up time from LPM3/4 16/	t <sub>CPU,LPM3/4</sub>			1 / f <sub>MCLK</sub> +	TYP	µs
<b>Crystal oscillator, XT1, low frequency mode</b> 17/ 42/						
LFXT1 oscillator crystal frequency, LF mode 0, 1	f <sub>LFXT1,LF</sub>	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V	32768	TYP	Hz
LFXT1 oscillator logic level square wave input frequency, LF mode	f <sub>LFXT1,LF,logic</sub>	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	50000	Hz
LFXT1 oscillator logic level square wave input frequency, LF mode	f <sub>LFXT1,LF,logic</sub>	XTS = 0, XCAPx = 0, LFXT1Sx = 3, T <sub>A</sub> = -40°C to 125°C	1.8 V to 3.6 V	32768	TYP	Hz
Oscillation allowance for LF crystals	O <sub>A,LF</sub>	XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF		500	TYP	kΩ
		XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF		200	TYP	kΩ
Integrated effective load capacitance, LF mode 18/	C <sub>L,eff</sub>	XTS = 0, XCAPx = 0		1	TYP	pF
		XTS = 0, XCAPx = 1		5.5	TYP	pF
		XTS = 0, XCAPx = 2		8.5	TYP	pF
		XTS = 0, XCAPx = 3		11	TYP	pF
Duty cycle, LF mode		XTS = 0, Measured at P2.0/ACLK, f <sub>LFXT1,LF</sub> = 32768 Hz	2.2 V	30	70	%
Oscillator fault frequency, LF mode 19/	f <sub>Fault,LF</sub>	XTS = 0, XCAPx = 0, LFXT1Sx = 3 20/	2.2 V	10	10000	Hz

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>Internal Very Low power Low frequency Oscillator (VLO)</b>						
VLO frequency	f <sub>VLO</sub>	T <sub>A</sub> = -40°C to 85°C	3 V	4	20	kHz
		T <sub>A</sub> = 125°C			23	kHz
VLO frequency temperature drift	df <sub>VLO</sub> /dT	T <sub>A</sub> = -40°C to 125°C	3 V	0.5	TYP	%/°C
VLO frequency supply voltage drift	df <sub>VLO</sub> /dV <sub>CC</sub>	T <sub>A</sub> = 25°C	1.8 V to 3.6 V	4	TYP	%/V
<b>Timer_A</b>						
Timer_A input clock frequency	f <sub>TA</sub>	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ±10%		f <sub>SYSTEM</sub>	TYP	MHz
Timer_A capture timing	f <sub>TA,cap</sub>	TA0, TA1	3 V	20		ns
<b>USI, Universal Serial Interface</b>						
USI clock frequency	f <sub>USI</sub>	External: SCLK, Duty cycle = 50% ±10% SPI slave mode		f <sub>SYSTEM</sub>	TYP	MHz
Low level output voltage on SDA and SCL	V <sub>OL,I2C</sub>	USI module in I <sup>2</sup> C mode, I <sub>(OL,max)</sub> = 1.5 mA	3 V	V <sub>SS</sub>	V <sub>SS</sub> + 0.4	V

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/ 3/ 4/</u>	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>10 Bit ADC, Power supply and input range conditions <u>21/</u></b>							
Analog supply voltage	V <sub>CC</sub>	V <sub>SS</sub> = 0			2.2	3.6	V
Analog input voltage <u>22/</u>	V <sub>AX</sub>	All Ax terminal, Analog inputs selected in ADC10AE register		3 V	0	V <sub>CC</sub>	V
ADC10 supply current <u>23/</u>	I <sub>ADC10</sub>	f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	-40°C to 125°C	3 v		1.64	mA
Reference supply current, reference buffer disabled	I <sub>REF+</sub>	f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	-40°C to 125°C	3 V		0.84	mA
<u>24/</u>		f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0		3 v		0.84	mA
Reference buffer supply current with ADC10SR = 0	I <sub>REFB,0</sub>	f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 0, REFON = 1,	-40°C to 125°C	3 V		3.8	mA
<u>24/</u>		REF2_5V = 0, REFOUT = 1, ADC10SR = 0	-40°C to 85°C			1.4	mA
Reference buffer supply current with ADC10SR = 1	I <sub>REFB,1</sub>	f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 0, REFON = 1,	-40°C to 125°C	3 v		0.9	mA
<u>24/</u>		REF2_5V = 0, REFOUT = 1, ADC10SR = 1	-40°C to 85°C			0.7	mA
Input capacitance	C <sub>i</sub>	Only one terminal Ax can be selected at one time	-40°C to 125°C	3 V		27	pF
Input MUX ON resistance	R <sub>i</sub>	0 V ≤ V <sub>AX</sub> ≤ V <sub>CC</sub>	-40°C to 125°C	3 v		2000	Ω

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>10 bit ADC, Built in voltage reference</b>						
Positive built in reference analog supply voltage range	V <sub>CC, REF+</sub>	I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 0		2.2		V
		I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 1		3		V
Positive built in reference voltage	V <sub>REF+</sub>	I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> max, REF2_5V = 0	3 V	1.4	1.59	V
		I <sub>VREF+</sub> ≤ I <sub>VREF+</sub> max, REF2_5V = 1		2.34	2.65	v
Maximum V <sub>REF+</sub> load current 44/ 45/	I <sub>LD, VREF+</sub>		3 V		±1	mA
V <sub>REF+</sub> load regulation 44/		I <sub>VREF+</sub> = 500 μA, Analog input voltage V <sub>AX</sub> ≠ 0.75 V, REF2_5V = 0	3 V		±2	LSB
		I <sub>VREF+</sub> = 500 μA ±100 μA Analog input voltage V <sub>AX</sub> ≠ 1.25 V, REF2_5V = 1			±2	LSB
V <sub>REF+</sub> load regulation response time 44/ 45/		I <sub>VREF+</sub> = 100 μA → 900 μA V <sub>AX</sub> ≠ 0.5 V x V <sub>REF+</sub> , Error conversion result ≤ 1 LSB, ADC10SR = 0	3 V		400	ns
Maximum capacitance at pin V <sub>REF+</sub> 44/ 45/	C <sub>VREF+</sub>	I <sub>VREF+</sub> ≤ 1 mA, REFON = 1, REFOUT = 1	3 V		100	pF
Temperature coefficient	T <sub>CREF+</sub>	I <sub>VREF+</sub> = const with 0 mA ≤ I <sub>VREF+</sub> ≤ 1 mA	3 V		±190	ppm/°C
Setting time of internal reference voltage to 99.9% V <sub>REF</sub> 44/ 45/	t <sub>REFON</sub>	I <sub>VREF+</sub> = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V		30	μs
Setting time of reference buffer to 99.9% V <sub>REF</sub> 44/ 45/	t <sub>REFBURST</sub>	I <sub>VREF+</sub> = 0.5 mA, REF2_5V = 1, REFON = 1 REFBURST = 1, ADC10SR = 0	3 V		2	μs
<b>10 Bit ADC, External reference 25/ 42/</b>						
Positive external reference input voltage range 26/	V <sub>REF+</sub>	V <sub>REF+</sub> > V <sub>REF-</sub> , SREF1 = 1, SREF0 = 0		1.4	V <sub>CC</sub>	V
		V <sub>REF-</sub> ≤ V <sub>REF+</sub> ≤ V <sub>CC</sub> - 0.15 V, SREF1 = 1, SREF0 = 1 27/		1.4	3	V
Negative external reference input voltage range 28/	V <sub>REF-</sub>	V <sub>REF+</sub> > V <sub>REF-</sub>		0	1.2	V
Differential external reference input voltage range, ΔV <sub>REF</sub> = V <sub>REF+</sub> - V <sub>REF-</sub>	ΔV <sub>REF</sub>	V <sub>REF+</sub> > V <sub>REF-</sub> 29/		1.4	V <sub>CC</sub>	V
Static input current into V <sub>REF+</sub>	I <sub>VREF+</sub>	0 V ≤ V <sub>REF+</sub> ≤ V <sub>CC</sub> , SREF1 = 1, SREF0 = 0	3 V	±1	TYP	μA
		0 V ≤ V <sub>REF+</sub> ≤ V <sub>CC</sub> - 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 27/	3 V	0	TYP	μA
Static input current into V <sub>REF-</sub>	I <sub>VREF-</sub>	0 V ≤ V <sub>REF-</sub> ≤ V <sub>CC</sub>	3 V	±1	TYP	μA

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit	
				Min	Max		
<b>10 Bit ADC, Timing parameters</b> 42/							
ADC10 input clock frequency	f <sub>ADC10CLK</sub>	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45	6.3	MHz
			ADC10SR = 1		0.45	1.5	
ADC10 built in oscillator frequency	f <sub>ADC10OSC</sub>	ADC10DIVx = 0, ADC10SSELx = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub>	3 V		3.7	6.3	MHz
Conversion time	t <sub>CONVERT</sub>	ADC10 built in oscillator, ADC10SSELx = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub>	3 V		2.06	3.51	μs
		f <sub>ADC10CLK</sub> from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 x ADC 1/f <sub>ADC10CLK</sub>	10DIV x	μs
Turn on setting time of the ADC	t <sub>ADC10ON</sub>	30/				100	ns
<b>10 Bit ADC, Linearity parameters</b> 42/							
Integral linearity error	E <sub>I</sub>		3 V			±1	LSB
Differential linearity error	E <sub>D</sub>		3 V			±1	LSB
Offset error	E <sub>O</sub>	Source impedance R <sub>s</sub> < 100 Ω	3 V			±1	LSB
Gain error	E <sub>G</sub>		3 V			±2	LSB
Total unadjusted error	E <sub>T</sub>		3 V			±5	LSB
<b>10 Bit ADC, Temperature sensor and built in V<sub>MID</sub></b> 42/							
Temperature sensor supply current 31/	I <sub>SENSOR</sub>	REFON = 0, INCHx = 0Ah, T <sub>A</sub> = 25°C	3 V		60	TYP	μA
	T <sub>CSENSOR</sub>	ADC10ON = 1 INCHx = 0Ah 32/	3 V		3.55	TYP	mV/°C
Sample time required if channel 10 is selected 33/	t <sub>Sensor(sample)</sub>	ADC10ON = 1 INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V		30		μs
Current into divider at channel 11	I <sub>V<sub>MID</sub></sub>	ADC10ON = 1 INCHx = 0Bh	3 V			34/	μA
V <sub>CC</sub> divider at channel 11	V <sub>MID</sub>	ADC10ON = 1 INCHx = 0Bh, V <sub>MID</sub> ≠ 0.5 x V <sub>CC</sub>	3 V		1.5	TYP	V
Sample time required if channel 11 is selected 35/	t <sub>V<sub>MID</sub>(sample)</sub>	ADC10ON = 1 INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V		1220		ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>Flash memory</b> 42/						
Program and erase supply voltage	V <sub>CC(PGM/ERASE)</sub>			2.2	3.6	V
Flash timing generator frequency	f <sub>FTG</sub>			257	476	kHz
Supply current from V <sub>CC</sub> during program	I <sub>PGM</sub>		3 V		5	mA
Supply current from V <sub>CC</sub> during erase	I <sub>ERASE</sub>		3 V		7	mA
Cumulative program time 36/	t <sub>CPT</sub>		2.2 V/3.6 V		10	ms
Cumulative mass erase time	t <sub>CMERASE</sub>		2.2 V/3.6 V	20		ms
Program/erase endurance		-40°C < T <sub>J</sub> < 105°C		10 <sup>4</sup>		cycles
Data retention duration	t <sub>Retention</sub>	T <sub>J</sub> = 25°C		15		years
Word or byte program time	t <sub>Word</sub>	37/		30	TYP	t <sub>FTG</sub>
Block program time for first byte or word	t <sub>Block, 0</sub>	37/		25	TYP	t <sub>FTG</sub>
Block program time for each additional byte or word	t <sub>Block, 1-63</sub>	37/		18	TYP	t <sub>FTG</sub>
Block program end sequence wait time	t <sub>Block, End</sub>	37/		6	TYP	t <sub>FTG</sub>
Mass erase time	t <sub>Mass Erase</sub>	37/		10593	TYP	t <sub>FTG</sub>
Segment erase time	t <sub>Seg Erase</sub>	37/		4819	TYP	t <sub>FTG</sub>
<b>RAM</b>						
RAM retention supply voltage 38/	V <sub>(RAMh)</sub>	CPU halted		1.6		V
<b>JTAG and Spy-Bi-Wire Interface</b>						
Spy-Bi-Wire input frequency	f <sub>SBW</sub>		2.2 V/3 V	0	20	MHz
Spy-Bi-Wire low clock pulse length	t <sub>SBW,Low</sub>		2.2 V/3 V	0.025	15	µs
Spy-Bi-Wire enable time (Test high to acceptance of first clock edge 39/)	t <sub>SBW,En</sub>		2.2 V/3 V		1	µs
Spy-Bi-Wire return to normal operation time	t <sub>SBW,Ret</sub>	T <sub>A</sub> = -40°C to 105°C	2.2 V/3 V	15	100	µs
TCK input frequency 40/	f <sub>TCK</sub>		2.2 V	0	5	MHz
			3 V	0	10	MHz
Internal pulldown resistance on TEST	R <sub>Internal</sub>	T <sub>A</sub> = -40°C to 105°C	2.2 V/3 V	25	90	kΩ

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>JTAG fuse</b> <u>41/</u> <u>43/</u>						
Supply voltage during fuse blow condition	V <sub>CC(FB)</sub>			2.5		V
Voltage level on TEST for fuse blow	V <sub>FB</sub>			6	7	V
Supply current into TEST during fuse blow	I <sub>FB</sub>				100	mA
Time to blow fuse	t <sub>FB</sub>				1	ms

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over recommended operating free air temperature range (unless otherwise noted).
- 3/ All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current.
- 4/ The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen closely match the required 9 pF.
- 5/ Current for brownout and WDT clocked by SMCLK included.
- 6/ Current for brownout and WDT clocked by ACLK included.
- 7/ Current for brownout included.
- 8/ The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.
- 9/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
- 10/ The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- 11/ A resistive divider with 2 x 0.5 kΩ resistors between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.
- 12/ The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.
- 13/ The current consumption of the brownout module is already included in the ICC current consumption data. The voltage level V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub> is ≤ 1.8 V.
- 14/ This is the frequency change from the measured frequency at 30°C over temperature.
- 15/ The DCO clock wake up time is measured from the edge of an external wake up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- 16/ Parameter applicable only if DCOCLK is used for MCLK.
- 17/ To improve EMI on the XT1 oscillator, the following guide lines should be observed.
- Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

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TABLE I. Electrical performance characteristics - Continued. 1/

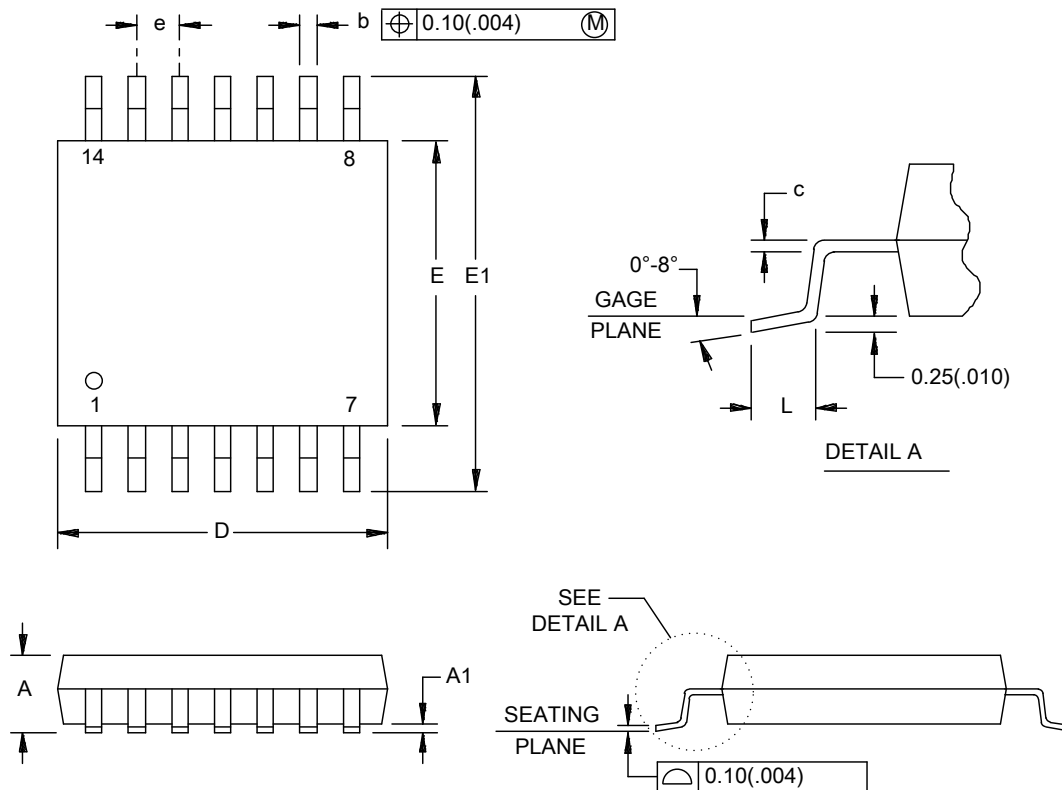
- 18/ Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct set up, the effective load capacitance should always match the specification of the used crystal.
- 19/ Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- 20/ Measured with logic level input frequency but also applies to operation with crystals.
- 21/ The leakage current is defined in the leakage current table with Px.y/Ax parameter.
- 22/ The analog input voltage range must be within the selected reference voltage range  $V_{R+}$  to  $V_{R-}$  for valid conversion result.
- 23/ The internal reference supply current is not included in current consumption parameter  $I_{ADC10}$ .
- 24/ The internal reference current is supplied by terminal  $V_{CC}$ . Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.
- 25/ The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance,  $C_i$ , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog source impedance to allow the charge to settle for 10 bit accuracy.
- 26/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- 27/ Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current  $I_{REFB}$ . The current consumption can be limited to the sample and conversion period with REBURST = 1.
- 28/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- 29/ The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- 30/ The condition is that the error in a conversion started after  $t_{ADC10ON}$  is less than  $\pm 0.5$  LSB. The reference and input signal are already settled.
- 31/ The sensor current  $I_{SENSOR}$  is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1,  $I_{SENSOR}$  is included in IREF+. When REFON = 0,  $I_{SENSOR}$  applies during conversion of the temperature sensor input (INCH = 0Ah).
- 32/ The following formula can be used to calculate the temperature sensor output voltage:  

$$V_{Sensor, typ} = TC_{Sensor} (273 + T[^\circ C]) + V_{Offset, sensor}[mV]$$
 or  

$$V_{Sensor, typ} = TC_{Sensor} T[^\circ C] + V_{Sensor}(T_A = 0^\circ C)[mV].$$
- 33/ The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor on time  $t_{SENSOR(on)}$ .
- 34/ No additional current is needed. The  $V_{MID}$  is used during sampling.
- 35/ The on time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.
- 36/ The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- 37/ These values are hardwired into the Flash controller state machine ( $t_{FTG} = 1/f_{FTG}$ ).
- 38/ This parameter defines the minimum supply voltage  $V_{CC}$  when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.
- 39/ Tools accessing the Spy-Bi-Wire interface need to wait for the maximum  $t_{SBW,En}$  time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
- 40/  $f_{TCK}$  may be restricted to meet the timing requirements of the module selected.
- 41/ Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.
- 42/ Over recommended ranges of supply voltage and up to operating free air temperature,  $T_A = 105^\circ C$  (unless otherwise noted).
- 43/ Over recommended ranges of supply voltage,  $T_A = 25^\circ C$  (unless otherwise noted).
- 44/ Minimum and maximum parameters are characterized up to  $T_A = 105^\circ C$  (unless otherwise noted).
- 45/ characterized at  $T_A = -40^\circ C$  to  $105^\circ C$  only.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65	BSC
c	0.15	NOM	L	0.50	0.75
D	4.90	5.10			

NOTES:

1. All linear dimensions are in millimeters (inches).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 0.15 each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
5. Fall within JEDEC MO-153

FIGURE 1. Case outline.

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Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DVCC	8	P1.6/TA0.1/A6/SDO/SCL/TDI/TCLK
2	P1.0/TA0CLK/ACLK/A0	9	P1.7/A7/SDI/SDA/TDO/TDI
3	P1.1/TA0.0/A1	10	$\overline{\text{RST}}$ /NMI/SBWT DIO
4	P1.2/TA0.1/A2	11	TEST/SBWTCK
5	P1.3/ADC10CLK/A3/VREF-/VEREF-	12	XOUT/P2.7
6	P1.4/SMCLK/A4/VREF+/VEREF+/TCK	13	XIN/P2.6/TA0.1
7	P1.5/TA0.0/A5/SCLK/TMS	14	DVSS

FIGURE 2. Terminal connections.

Terminal		I/O	Description
Name	No.		
P1.0/ TA0CLK/ ACLK A0	2	I/O	General purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output ADC10 analog input A0 <u>1/</u>
P1.1/ TA0.0/ A1	3	I/O	General purpose digital I/O pin Timer0_A, capture:CCI0A input, compare: Out0 output ADC10 analog input A1 <u>1/</u>
P1.2/ TA0.1/ A2	4	I/O	General purpose digital I/O pin Timer0_A, capture:CCI1A input, compare: Out1 output ADC10 analog input A2 <u>1/</u>
P1.3/ ADC10CLK/ A3/ VREF-/VEREF-	5	I/O	General purpose digital I/O pin ADC10, conversion clock output <u>1/</u> ADC10 analog input A3 <u>1/</u> ADC10 negative reference voltage <u>1/</u>
P1.4/ SMCLK/ A4/ VREF+/VEREF+/ TCK	6	I/O	General purpose digital I/O pin SMCLK signal output ADC10 analog input A4 <u>1/</u> ADC10 positive reference voltage <u>1/</u> JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ A5/ SCLK/ TMS	7	I/O	General purpose digital I/O pin Timer0_A, compare: Out0 output ADC10 analog input A5 USI: clock input in I2C mode; clock input/output in SPI mode JTAG test data input or test clock input during programming and test

See footnote at end of table.

FIGURE 3. Terminal function.

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Terminal		I/O	Description
Name	No.		
P1.6/ TA0.1/ A6/ SDO/ SCL/ TDI/TCLK	8	I/O	General purpose digital I/O pin Timer0_A, capture: CCI1A input, compare Out1 output ADC10 analog input A6 USI: Data output in SPI mode USI: I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/ A7/ SDI/ SDA/ TDO/TDI <u>2/</u>	9	I/O	General purpose digital I/O pin ADC10 analog input A7 <u>1/</u> USI: Data output in SPI mode USI: Data i2c in I2C mode JTAG test data output terminal or test data input during programming and test
XIN/ P2.6/ TA0.1	13	I/O	Input terminal of crystal oscillator <u>3/</u> General purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	12	I/O	Output terminal of crystal oscillator <u>3/</u> General purpose digital I/O pin
$\overline{\text{RST}}$ / NMI/ SBWTDIO	10	I	Reset input Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	11	I	Select test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test.
DVCC	1	N/A	Supply voltage
DVSS	14	N/A	Ground reference
QFN Pad		N/A	QFN package pad connection to V <sub>SS</sub> recommended.

1/ MSP430G2x31 only.

2/ TDO and TDI is selected via JTAG instruction.

3/ If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

FIGURE 3. Terminal function - Continued.

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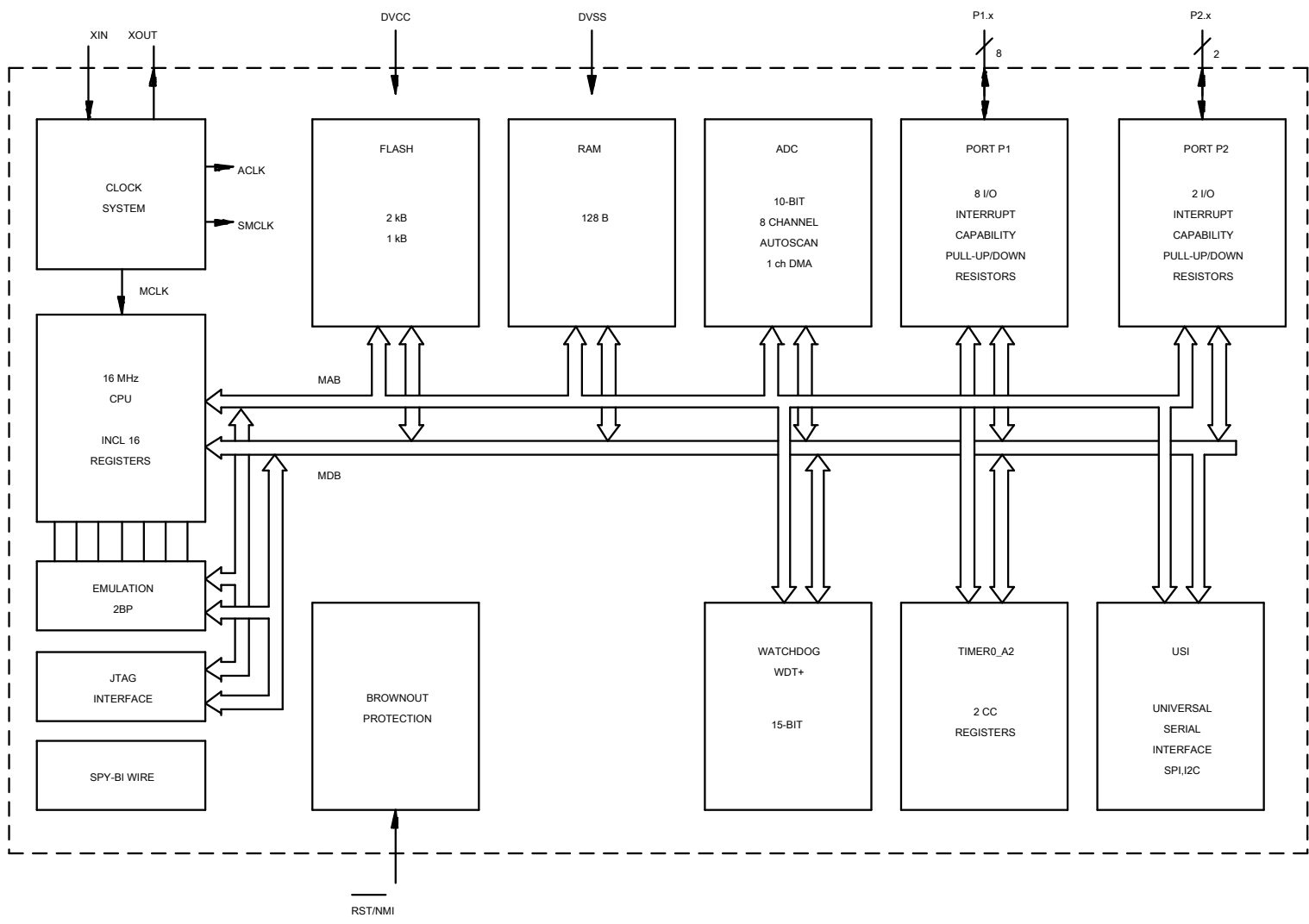
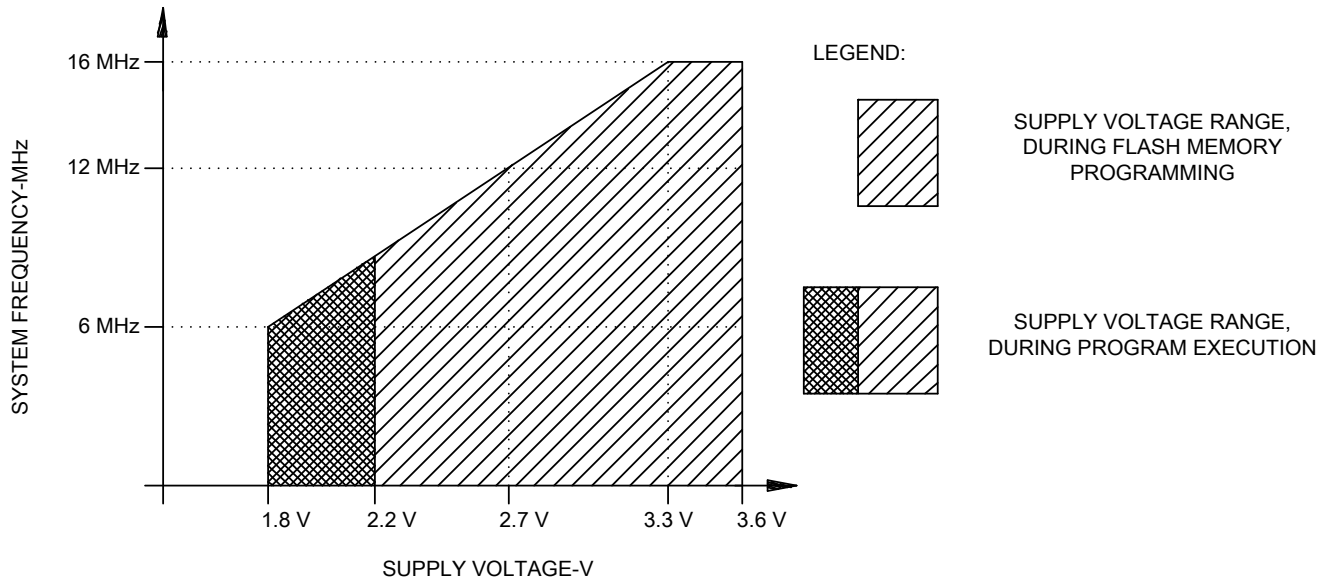


FIGURE 4. Functional block diagram.

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**NOTE:**

1. Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.2 V.

FIGURE 5. Safe operating area.

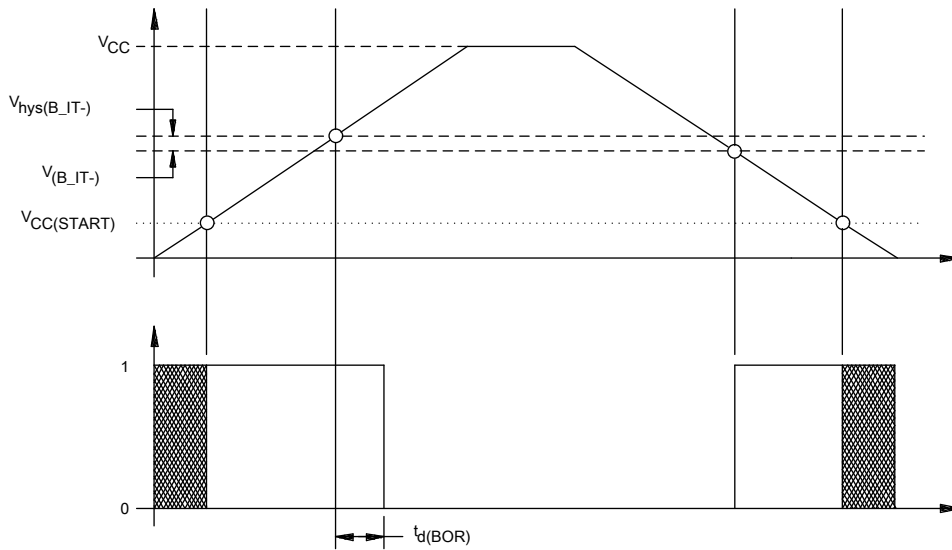


FIGURE 6. POR/Brownout Reset (BOR) vs Supply voltage.

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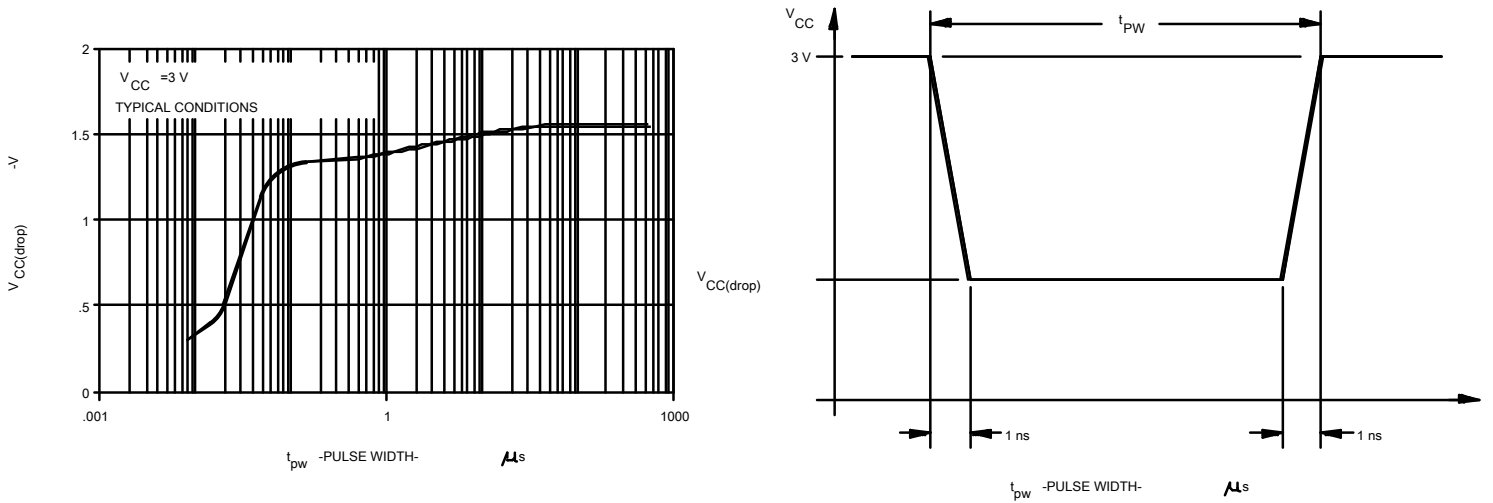


FIGURE 7.  $V_{CC(drop)}$  level with a Square voltage drop to generate a POR/Brownout signal.

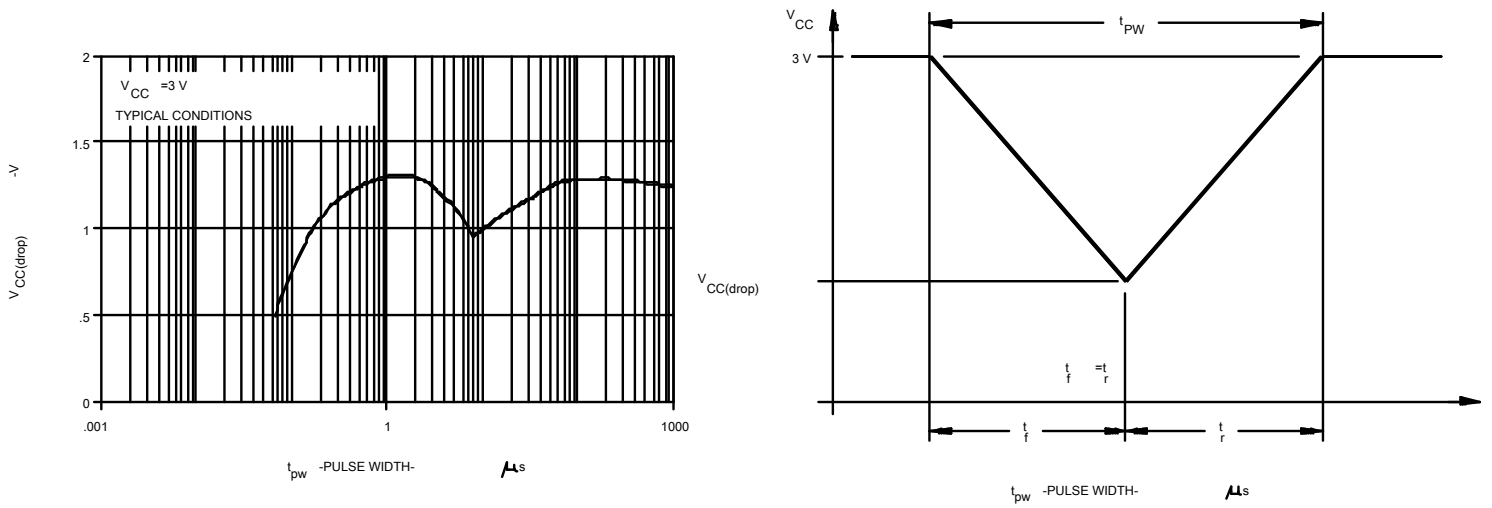


FIGURE 8.  $V_{CC(drop)}$  level with a Triangle voltage drop to generate a POR/Brownout signal.

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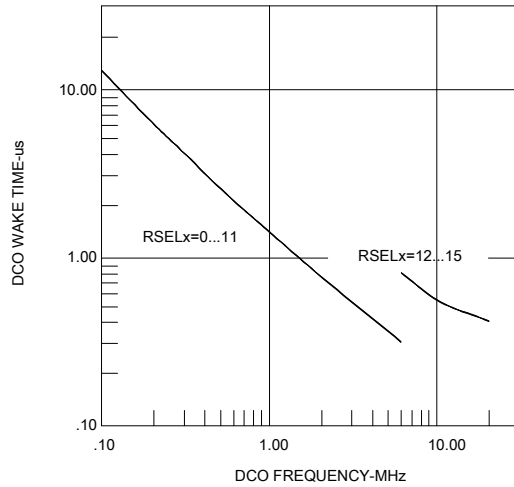


FIGURE 9. DCO wake-up time from LPM3/4 vs DCO frequency.

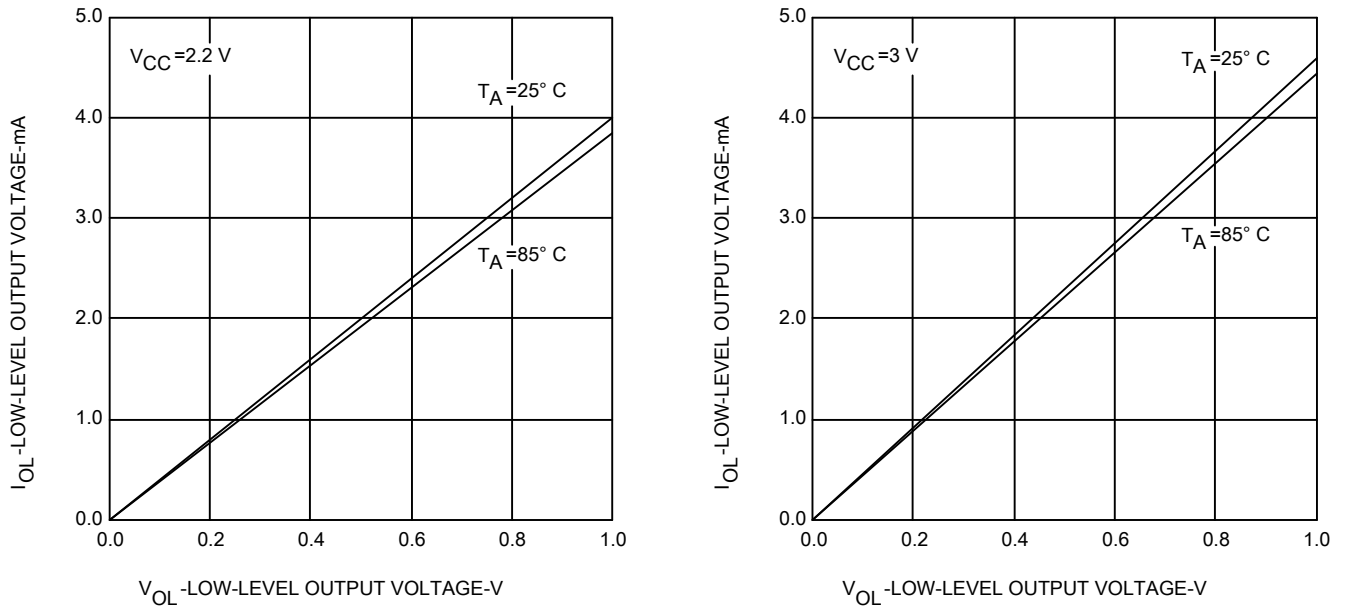


FIGURE 10. USI low level output voltage vs output current.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <sup>1/</sup>	Device manufacturer CAGE code	Top side marking	Transport media	Vendor part number
V62/12621-01XE	01295	G2231EP	Tape and reel	MSP430G2231QPW1REP
			Tube	MSP430G2231QPW1EP

<sup>1/</sup> The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CAGE CODE 16236</b>	<b>DWG NO. V62/09618</b>
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