REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-04-16	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-09-18	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

Original date of drawing

YY MM DD

12-12-14

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TITLE
MICROCIRCUIT, DIGITAL, MIXED SIGNAL MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/12620
REV B		PAGE 1 OF 12

AMSC N/A

5962-V155-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -40ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12620	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MSP430G2230-EP	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage applied at V_{CC} to V_{SS} ..... -0.3 V to 4.1 V
Voltage applied to any pin ..... -0.3 V to V_{CC} +0.3 V 2/
Diode current at any device terminal ..... ±2 mA
Storage temperature: 3/
Unprogrammed device ..... -55°C to 150°C
Programmed device ..... -40°C to 150°C

1.4 Recommended operating conditions.

Supply voltage, (V_{CC}):
During program execution ..... 1.8 V to 3.6 V
During flash program/erase ..... 2.2 V to 3.6 V
Supply voltage, (VSS) ..... 0 V
Operating free air temperature, (T_A) ..... -40°C to 125°C
Processor frequency (Maximum MCLK frequency) 4/ 5/
V_{CC} = 1.8 V, Duty cycle = 50% ±10% ..... dc to 6 MHz
V_{CC} = 2.7 V, Duty cycle = 50% ±10% ..... dc to 12 MHz
V_{CC} = 3.3 V, Duty cycle = 50% ±10% ..... dc to 16 MHz

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices
J-STD-020 – Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.
(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values referenced to V_{SS}. The JTAG fuse blow voltage, V_{FB} is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse..
3/ Higher temperature may be applied during board soldering according to the current JEDEC J STD 020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
4/ The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
5/ Modules might have different maximum input clock specification. See the specification from the manufacturer data sheet.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Safe operating area. The safe operating area shall be as shown in figure 5.

3.5.6 POR/Brownout Reset (BOR) vs Supply voltage. The POR/Brownout Reset (BOR) vs Supply voltage shall be as shown in figure 6.

3.5.7 $V_{CC(drop)}$ level with a Square voltage drop to gernerate a POR/Brownout signal. The $V_{CC(drop)}$ level with a Square voltage drop to gernerate a POR/Brownout signal shall be as shown in figure 7.

3.5.8 $V_{CC(drop)}$ level with a Triangle voltage drop to gernerate a POR/Brownout signal. The $V_{CC(drop)}$ level with a Triangle voltage drop to gernerate a POR/Brownout signal shall be as shown in figure 8.

3.5.9 DCO wake-up time from LPM3/4 vs DCO frequency. The DCO wake-up time from LPM3/4 vs DCO frequency waveforms shall be as shown in figure 9.

3.5.10 USI low level output voltage vs output current. The USI low level output voltage vs output current shall be as shown in figure 10.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	T_A	V_{CC}	Limits		Unit
					Min	Max	
Active mode supply current into V_{CC} excluding external current							
Active mode (AM) current (1 MHz)	$I_{AM, 1MHz}$	$f_{DCO} = f_{MCLK}$ = 1 MHz, f_{ACLK} = 0 Hz, Program executes in flash,		2.2 V	220	TYP	µA
		BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 0, SCG0 = 0 SCG1 = 0, OSCOOFF = 0		3 V		390	µA
Low power mode Supply current (into V_{CC}) Excluding external current							
Low power mode 0 (LPM0) current 3/	$I_{LPM0, 1MHz}$	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{CDO}$ = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V	65	TYP	µA
Low power mode 2 (LPM2) current 4/	I_{LPM2}	$f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{CDO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHz,	25°C	2.2 V		29	µA
		DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	125°C			46	µA
Low power mode 3 (LPM3) current 4/	$I_{LPM3, VLO}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1,	25°C	2.2 V		0.7	µA
		SCG1 = 1, OSCOFF = 0	125°C			9.3	µA
Low power mode 4 (LPM4) current 5/	I_{LPM4}	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1,	25°C	2.2 V		0.5	µA
		SCG1 = 1, OSCOFF = 1	85°C			1.5	µA
		T_A = 125°C $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1		2.2 V		7.1	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits		Unit
				Min	Max	
Schmitt Trigger inputs (Port P1)						
Positive going input threshold voltage	V_{IT+}			0.45 V_{CC}	0.75 V_{CC}	V
			3 V	1.35	2.25	V
Negative going input threshold voltage	V_{IT-}			0.25 V_{CC}	0.55 V_{CC}	V
			3 V	0.75	1.65	V
Input voltage hysteresis (V_{IT+} - V_{IT-})	V_{hys}		3 V	0.3	1.0	V
Pullup/pulldown resistor	R_{Pull}	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	50	kΩ
Input capacitance	C_I	$V_{IN} = V_{SS}$ or V_{CC}		5 TYP		pF
Leakage current (Port P1)						
High impedance leakage current	$I_{lkg(Px.y)}$	6/ 7/	3 V		±120	nA
Outputs (Port P1)						
High level output voltage	V_{OH}	$I_{(OHmax)}$ = -6 mA 8/	3 V	V_{CC} – 0.3 TYP		V
Low level output voltage	V_{OL}	$I_{(OLmax)}$ = 6 mA 8/	3 V	V_{SS} + 0.3 TYP		V
Output frequency (Port P1)						
Port output frequency (with load)	$f_{Px.y}$	C_L = 20 pF, R_L = 1 kΩ 9/ 10/	3 V	12 TYP		MHz
Clock output frequency	$f_{Port°CLK}$	C_L = 20 pF 10/	3 V	16 TYP		MHz
POR/Brownout reset (BOR) 11/						
See figure 10	$V_{CC(start)}$	$dV_{CC}/dt \le 3$ V/s		0.7 x $V_{(B\_IT-)}$ TYP		V
See figure 10 through figure 12	$V_{(B\_IT-)}$	$dV_{CC}/dt \le 3$ V/s			1	V
See figure 10	$V_{hys(B\_IT-)}$	$dV_{CC}/dt \le 3$ V/s		140 TYP		mV
See figure 10	$t_{d(BOR)}$	34/			2000	µs
Pulse length needed at $\overline{RST}$/NMI pin to accept reset internally	$t_{(reset)}$	34/	3 V	2		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits		Unit
				Min	Max	
DCO frequency						
		RSELx < 14		1.8	3.6	V
Supply voltage	V_{CC}	RSELx = 14		2.2	3.6	V
		RSELx = 15		3.0	3.6	V
DCO frequency (0, 0)	$f_{DCO(0,0)}$	RSELx = 0, DCOx = 0, MDDx = 0	3 V	0.096	TYP	MHz
DCO frequency (0, 3)	$f_{DCO(0,3)}$	RSELx = 0, DCOx = 3, MDDx = 0	3 V	0.12	TYP	MHz
DCO frequency (1, 3)	$f_{DCO(1,3)}$	RSELx = 1, DCOx = 3, MDDx = 0	3 V	0.15	TYP	MHz
DCO frequency (2, 3)	$f_{DCO(2,3)}$	RSELx = 2, DCOx = 3, MDDx = 0	3 V	0.21	TYP	MHz
DCO frequency (3, 3)	$f_{DCO(3,3)}$	RSELx = 3, DCOx = 3, MDDx = 0	3 V	0.30	TYP	MHz
DCO frequency (4, 3)	$f_{DCO(4,3)}$	RSELx = 4, DCOx = 3, MDDx = 0	3 V	0.41	TYP	MHz
DCO frequency (5, 3)	$f_{DCO(5,3)}$	RSELx = 5, DCOx = 3, MDDx = 0	3 V	0.58	TYP	MHz
DCO frequency (6, 3)	$f_{DCO(6,3)}$	RSELx = 6, DCOx = 3, MDDx = 0	3 V	0.80	TYP	MHz
DCO frequency (7, 3)	$f_{DCO(7,3)}$	RSELx = 7, DCOx = 3, MDDx = 0	3 V	0.80	1.50	MHz
DCO frequency (8, 3)	$f_{DCO(8,3)}$	RSELx = 8, DCOx = 3, MDDx = 0	3 V	1.6	TYP	MHz
DCO frequency (9, 3)	$f_{DCO(9,3)}$	RSELx = 9, DCOx = 3, MDDx = 0	3 V	2.3	TYP	MHz
DCO frequency (10, 3)	$f_{DCO(10,3)}$	RSELx = 10, DCOx = 3, MDDx = 0	3 V	3.4	TYP	MHz
DCO frequency (11, 3)	$f_{DCO(11,3)}$	RSELx = 11, DCOx = 3, MDDx = 0	3 V	4.25	TYP	MHz
DCO frequency (12, 3)	$f_{DCO(12,3)}$	RSELx = 12, DCOx = 3, MDDx = 0	3 V	4.3	7.30	MHz
DCO frequency (13, 3)	$f_{DCO(13,3)}$	RSELx = 13, DCOx = 3, MDDx = 0	3 V	7.8	TYP	MHz
DCO frequency (14, 3)	$f_{DCO(14,3)}$	RSELx = 14, DCOx = 3, MDDx = 0	3 V	8.6	13.9	MHz
DCO frequency (15, 3)	$f_{DCO(15,3)}$	RSELx = = 15, DCOx = 3, MDDx = 0	3 V	15.25	TYP	MHz
DCO frequency (15, 7)	$f_{DCO(15,7)}$	RSELx = 15, DCOx = 7, MDDx = 0	3 V	21	TYP	MHz
Frequency step between range RSEL and RSEL + 1	S_{RESL}	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V	1.35	TYP	ratio
Frequency step between tap DCO and DCO + 1	S_{DCO}	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V	1.08	TYP	ratio
Duty cycle			3 V	50	TYP	%

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Conditions 2/	T_A	V_{CC}	Limits		Unit
				Min	Max	
Calibrated DCO frequencies – Tolerance over temperature -40°C to 125°C						
1 MHz tolerance over temperature	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	3	%
8 MHz tolerance over temperature	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	3	%
12 MHz tolerance over temperature	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	3	%
16 MHz tolerance over temperature	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, calibrated at 30°C and 3 V	-40°C to 125°C	3 V	-3	3	%
Calibrated DCO frequencies – Tolerance over supply voltage V_{CC}						
1 MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	25°C	1.8 V to 3.6 V	-3	3	%
8 MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, calibrated at 30°C and 3 V	25°C	1.8 V to 3.6 V	-3	3	%
12 MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, calibrated at 30°C and 3 V	25°C	2.2 V to 3.6 V	-3	3	%
16 MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, calibrated at 30°C and 3 V	25°C	3 V to 3.6 V	-6	3	%
Calibrated DCO frequencies – Overall tolerance						
1 MHz tolerance overall	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, calibrated at 30°C and 3 V	-40°C to 85°C	1.8 V to 3.6 V	-5	+5	%
8 MHz tolerance overall	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, calibrated at 30°C and 3 V	-40°C to 85°C	1.8 V to 3.6 V	-5	+5	%
12 MHz tolerance overall	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, calibrated at 30°C and 3 V	-40°C to 85°C	2.2 V to 3.6 V	-5	+5	%
16 MHz tolerance overall	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, calibrated at 30°C and 3 V	-40°C to 85°C	3.0 V to 3.6 V	-6	+6	%

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits		Unit
				Min	Max	
Wake up from Lower Power Models (LPM3/4)						
DCO clock wake up time from LPM3/4 12/	$t_{DCO,LPM3/4}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz,	2.2 V/ 3 V	2 TYP		µs
		BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz,		1.5 TYP		µs
		BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz,		1 TYP		µs
		BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz,	3 V	1 TYP		µs
CPU wake up time from LPM3/4 13/	$t_{CPU,LPM3/4}$			$1 / f_{MCLK} + t_{Clock,LPM3/4}$ TYP		µs
Internal Very Low power Low frequency Oscillator (VLO)						
VLO frequency	f_{VLO}	T_A = -40°C to 85°C	3 V	4	20	kHz
		T_A = 125°C			23	
VLO frequency temperature drift 14/	df_{VLO}/d_T	T_A = -40°C to 85°C	3 V	0.5 TYP		%/°C
VLO frequency supply voltage drift 15/	df_{VLO}/dV_{CC}	T_A = 25°C	1.8 V to 3.6 V	4 TYP		%/V
Timer_A						
Timer_A clock frequency	f_{TA}	Internal: SMCLK External: TACLK, INCLK Duty cycle = 50% ±10%		f_{SYSTEM} TYP		MHz
Timer_A capture timing	$f_{TA,cap}$	TAx	3 V	20		ns
USI, Universal Serial Interface						
USI clock frequency	f_{USI}	External: SCLK, Duty cycle = 50% ±10% SPI slave mode USI module in I^2C mode, $I_{(OLmax)}$ = 1.5 mA		f_{SYSTEM} TYP		MHz
Loe level output voltage on SDA and SCL	$V_{OL,I2C}$		3 V	V_{SS}	V_{SS} + 0.4	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits		Unit
				Min	Max	
10 Bit ADC, Power supply and input range conditions						
Analog supply voltage	V_{CC}	V_{SS} = 0		2.2	3.6	V
Analog input voltage 17/	VAx	All Ax terminal, Analog inputs selected in ADC10AE register	3 V	0	V_{CC}	V
ADC10 supply current 18/	I_{ADC10}	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	3 v	0.6	TYP	mA
Reference supply current, reference buffer disabled	I_{REF+}	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	3 V	0.25	TYP	mA
19/		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0	3 v	0.25	TYP	mA
Reference buffer supply current with ADC10SR = 0 19/	$I_{REFB,0}$	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	3 V	1.1	TYP	mA
Reference buffer supply current with ADC10SR = 1 19/	$I_{REFB,1}$	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 0, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	3 v	0.5	TYP	mA
Input capacitance	C_I	Only one terminal Ax can be selected at one time	3 V		27	pF
Input MUX ON resistance	R_I	0 V ≤ V_{AX} ≤ V_{CC}	3 v	1000	TYP	Ω

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits		Unit
				Min	Max	
10 bit ADC, Built in voltage reference 35/						
Positive built in reference analog	$V_{CC, REF+}$	$I_{VREF+} \le 1$ mA, REF2_5V = 0		2.2		V
supply voltage range		$I_{VREF+} \le 1$ mA, REF2_5V = 1		3.0		V
Positive built in reference voltage	V_{REF+}	$I_{VREF+} \le I_{VREF+}$ max, REF2_5V = 0	3 V	1.4	1.59	V
		$I_{VREF+} \le I_{VREF+}$ max, REF2_5V = 1		2.34	2.65	V
Maximum V_{REF+} load current	$I_{LD,VREF+}$	34/	3 V		±1	mA
VREF+ load regulation		I_{VREF+} = 500 µA ±100 µA, Analog input voltage $V_{Ax} \ne 0.75$ V, REF2_5V = 0	3 V		±2	LSB
		I_{VREF+} = 500 µA ±100 µA Analog input voltage $V_{Ax} \ne 1.25$ V, REF2_5V = 1			±2	LSB
VREF+ load regulation response time		I_{VREF+} = 100 µA → 900 µA $V_{Ax} \ne 0.5$ V x VREF+, Error conversion result ≤ 1 LSB, ADC10SR = 0	3 V		400	ns
Maximum capacitance at pin VREF+	C_{VREF+}	$I_{VREF+} \le 1$ mA, REFON = 1, REFOUT = 1	3 V		100	pF
Temperature coefficient	TC_{REF+}	I_{VREF+} = const with 0 mA ≤ I_{VREF+} ≤ 1 mA	3 V		±190	ppm/°C
Setting time of internal reference voltage to 99.9% VREF	t_{REFON}	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V		30	µs
Setting time of reference buffer to 99.9% VREF	$t_{REFBURST}$	I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1 REFBURST = 1, ADC10SR = 0	3 V		2	µs
10 Bit ADC, External reference 20/ 36/						
Positive external reference input voltage range 21/	VEREF+	VEREF+ > VEREF-, SREF1 = 1, SREF0 = 0		1.4	V_{CC}	V
		VEREF- ≤ VEREF+ ≤ V_{CC} – 0.15 V, SREF1 = 1, SREF0 = 1 22/		1.4	3	V
Negative external reference input voltage range 23/	VEREF-	VEREF+ > VEREF-		0	1.2	V
Differential external reference input voltage range, ΔVEREF = VEREF+ - VEREF-	ΔVEREF	VEREF+ > VEREF- 24/		1.4	V_{CC}	V
Static input current into VEREF+	I_{VEREF+}	0 V ≤ VEREF+ ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 0	3 V	±1 TYP		µA
		0 V ≤ VEREF+ ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 22/	3 V	0 TYP		µA
Static input current into VEREF-	I_{VEREF-}	0 V ≤ VEREF- ≤ V_{CC}	3 V	±1 TYP		µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/		V_{CC}	Limits Min	Limits Max	Unit
10 Bit ADC, Timing parameters 36/							
ADC10 input clock frequency	$f_{ADC10CLK}$	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45	6.3	MHz
			ADC10SR = 1		0.45	1.5	MHz
ADC10 built in oscillator frequency	$f_{ADC10OSC}$	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7	6.3	MHz
Conversion time	$t_{CONVERT}$	ADC10 built in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06	3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 x ADC10DIV x $1/f_{ADC10CLK}$		µs
Turn on setting time of the ADC	$t_{ADC10ON}$	25/				100	ns
10 Bit ADC, Linearity parameters 36/							
Integral linearity error	E_I			3 V		±1	LSB
Differential linearity error	E_D			3 V		±1	LSB
Offset error	E_O	Source impedance R_S < 100 Ω		3 V		±1	LSB
Gain error	E_G			3 V		±2	LSB
Total unadjusted error	E_T			3 V		±5	LSB
10 Bit ADC, Temperature sensor and built in V_{MID} 36/							
Temperature sensor supply current 26/	I_{SENSOR}	REFON = 0, INCHx = 0Ah, T_A = 25°C		3 V	60 TYP		µA
	TC_{SENSOR}	ADC10ON = 1 INCHx = 0Ah 27/		3 V	3.55 TYP		mV/°C
Sample time required if channel 10 is selected 28/	$t_{Sensor(sample)}$	ADC10ON = 1 INCHx = 0Ah, Error of conversion result ≤ 1 LSB		3 V	30		µs
Current into divider at channel 11	I_{VMID}	ADC10ON = 1 INCHx = 0Bh		3 V		29/	µA
V_{CC} divider at channel 11	V_{MID}	ADC10ON = 1 INCHx = 0Bh, $V_{MID} \neq 0.5 \times V_{CC}$		3 V	1.5 TYP		V
Sample time required if channel 11 is selected 30/	$t_{VMID(sample)}$	ADC10ON = 1 INCHx = 0Bh, Error of conversion result ≤ 1 LSB		3 V	1220		ns
RAM							
RAM retention supply voltage 31/	$V_{(RAMh)}$	CPU halted			1.6		V

See footnote at end of table.

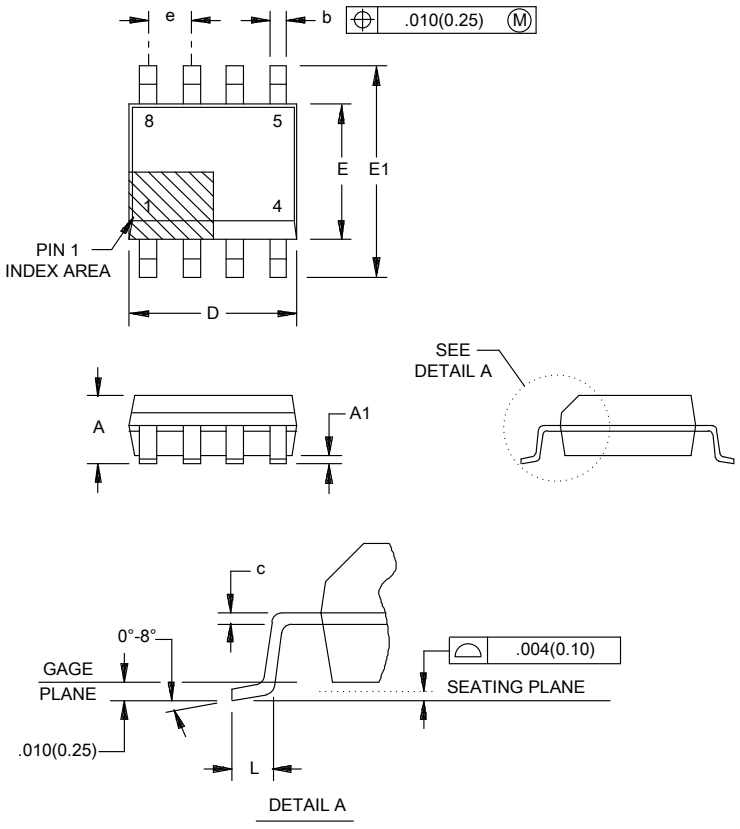
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	V_{CC}	Limits		Unit
				Min	Max	
Spy-Bi-Wire interface						
Spy-Bi-Wire input frequency	f_{SBW}		2.2 V/3 V	0	20	MHz
Spy-Bi-Wire low clock pulse length	$t_{SBW,Low}$		2.2 V/3 V	0.025	15	µs
Spy-Bi-Wireenable time (Test high to acceptance of first clock edge 32/)	$t_{SBW,En}$	T_A = -40°C to 105°C	2.2 V/3 V		1	µs
Spy-Bi-Wire return to normal operation time	$t_{SBW,Ret}$		2.2 V/3 V	15	100	µs
Internal pulldown resistance on TEST	$R_{Internal}$	T_A = -40°C to 105°C	2.2 V/3 V	25	90	kΩ
JTAG fuse 33/ 37/						
Supply voltage during fuse blow condition	$V_{CC(FB)}$			2.5		V
Voltage level on TEST for fuse blow	V_{FB}			6	7	V
Supply current into TEST during fuse blow	I_{FB}				100	mA
Time to blow fuse	t_{FB}				1	ms

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended operating free air temperature range (unless otherwise noted). All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3/ Current for brownout and WDT clocked by SMCLK included.
4/ Current for brownout and WDT clocked by ACLK included.
5/ Current for brownout included.
6/ The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
7/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
8/ The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
9/ A resistive divider with two 0.5 kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
10/ The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
11/ The current consumption of the brownout module is already included in the ICC current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
12/ The DCO clock wake up time is measured from the edge of an external wake up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
13/ Parameter applicable only if DCOCLK is used for MCLK.
14/ Calculated using the box method: (MAX(-40°C to 85°C) - MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C – (-40°C)).
15/ Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / Min(1.8 to 3.6 V) / (3.6 V – 1.8 V).
16/ The leakage current is defined in the leakage current table with Px.y/Ax parameter.

17/ The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion result.
18/ The internal reference supply current is not included in current consumption parameter I_{ADC10}.
19/ The internal reference current is supplied by terminal VCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.
20/ The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog source impedance to allow the charge to settle for 10 bit accuracy.
21/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
22/ Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
23/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
24/ The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
25/ The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
26/ The sensor current I_{SENSOR} is consuimed if (ADC10ON = 1 and REFON = 1) or (ADC10ON =1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in IREF+. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
27/ The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor, typ} = TC_{Sensor} (273 + T[°C] + V_{Offset,sensor}[mV]$ or
$V_{Sensor, typ} = TC_{Sensor}\ T[°C] + V_{Sensor}(T_A = 0°C)[mV]$.
28/ The typical equivalent is impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
29/ No additional current is needed. The V_{MID} is used during sampling.
30/ The on time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
31/ This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.
32/ Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
33/ Once the fuse is blown, no further access to the JATG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.
34/ Minimum and maximum parameters are characterized up to T_A = 105°C unless otherwise noted.
35/ Over recommended operating free air temperature range unless otherwise noted.
36/ Over recommended ranges of supply voltage and up to operating free air temperature T_A = 105°C (unless otherwise noted).
37/ T_A = 25°C, over recommended ranges of supply voltage (unless otherwise noted).

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.069		1.75	E	.150	.157	3.80	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.012	.020	0.31	0.51	e	.050 BSC		1.27 BSC	
c	.005	.010	0.13	0.25	L	.016	.050	0.40	1.27
D	.189	.197	4.80	5.00					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0.15) each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0.43) each side.
5. Reference JEDEC MS-012.

FIGURE 1. Case outline.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DVCC	5	DVSS
2	P1.2/TA0.1/A2	6	TEST/SBWTCK
3	P1.5/TA0.0/A5/SCLK	7	$\overline{\text{RST}}$/NMI/SBWTDIO
4	P1.6/TA0.1/A6/SDO/SCL	8	P1.7/A7/SDI/SDA

FIGURE 2. Terminal connections.

Terminal		I/O	Description
Name	No.		
P1.2/ TA0.1/ A2	2	I/O	General purpose digital I/O pin Timer_A, capture: CCI1A input, compare Out1 output ADC10 analog input A2
P1.5/ TA0.0/ A5/ SCLK	3	I/O	General purpose digital I/O pin Timer_A, compare Out0 output ADC10 analog input A5 USI: clock input in I2C mode; clock input/output in SPI mode
P1.6/ TA0.1/ A6/ SDO/ SCL	4	I/O	General purpose digital I/O pin Timer_A, capture: CCI1B input, compare Out1 output ADC10 analog input A6 USI: Data output in SPI mode USI: I2C clock in I2C mode
P1.7/ A7/ SDI/ SDA	5	I/O	General purpose digital I/O pin ADC10 analog input A7 USI: Data output in SPI mode USI: Data input in I2C mode
$\overline{\text{RST}}$/ NMI/ SBWTDIO	6	I	Reset imput Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	7	I	Select test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test.
DVCC	1		Digital supply voltage
DVSS	8		Digital ground reference

The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented but not available on the device pinout. To avoid floating inputs, these digital I/Os should be properly configured. The pullup or pulldown resistors of the unbounded P1.x GPIOs should be enabled, and the VLO should be selected as the ACLK source. (See manufacturer for more information).

FIGURE 3. Terminal function.

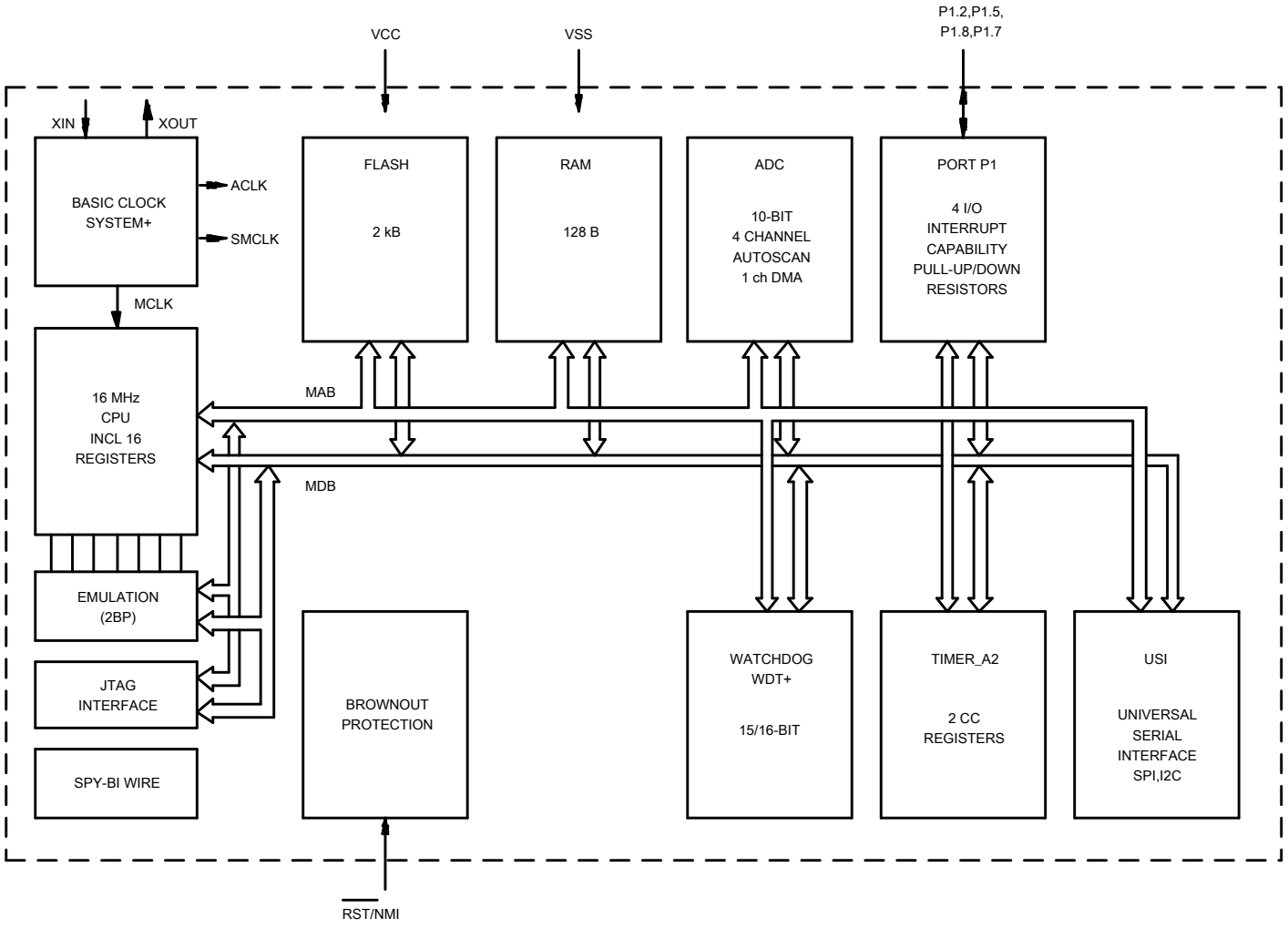
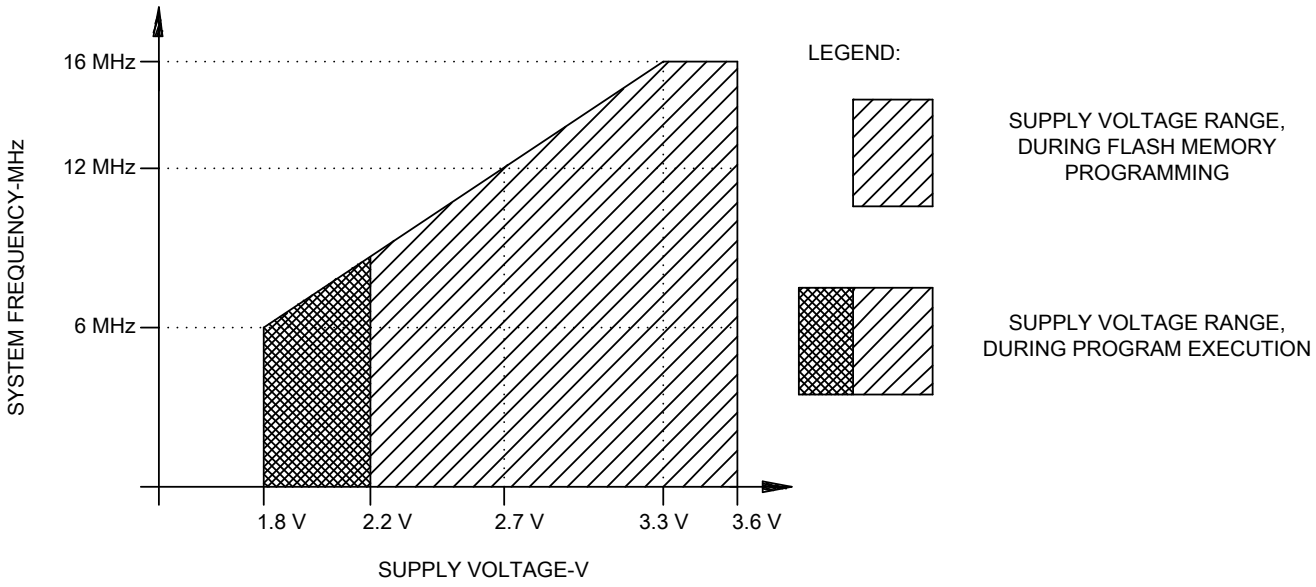


FIGURE 4. Functional block diagram.



NOTE:
1. Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

FIGURE 5. Safe operating area.

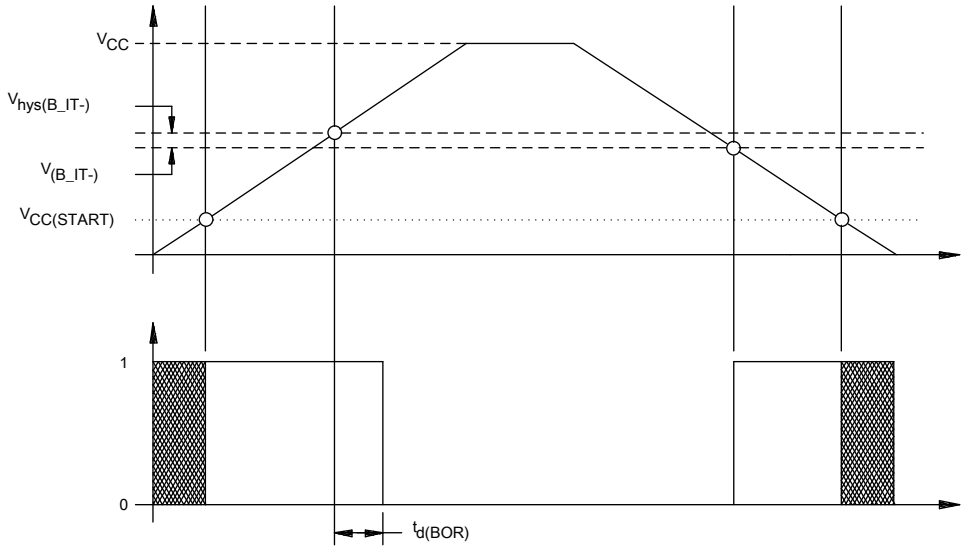


FIGURE 6. POR/Brownout Reset (BOR) vs Supply voltage.

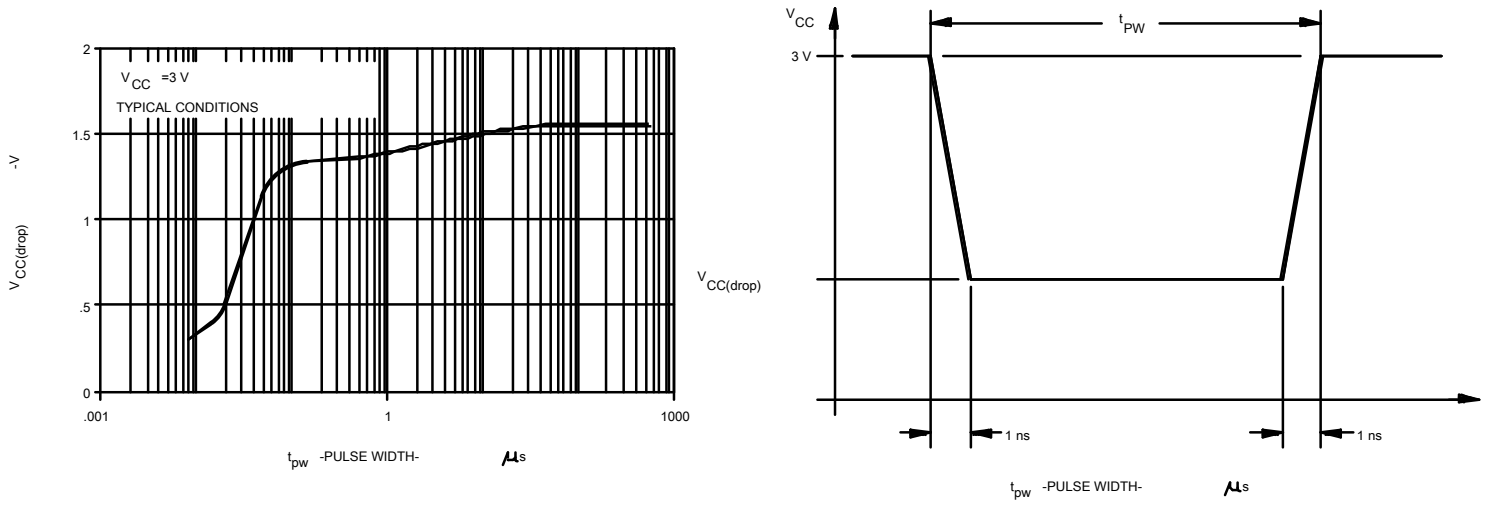


FIGURE 7. $V_{CC(drop)}$ level with a Square voltage drop to generate a POR/Brownout signal.

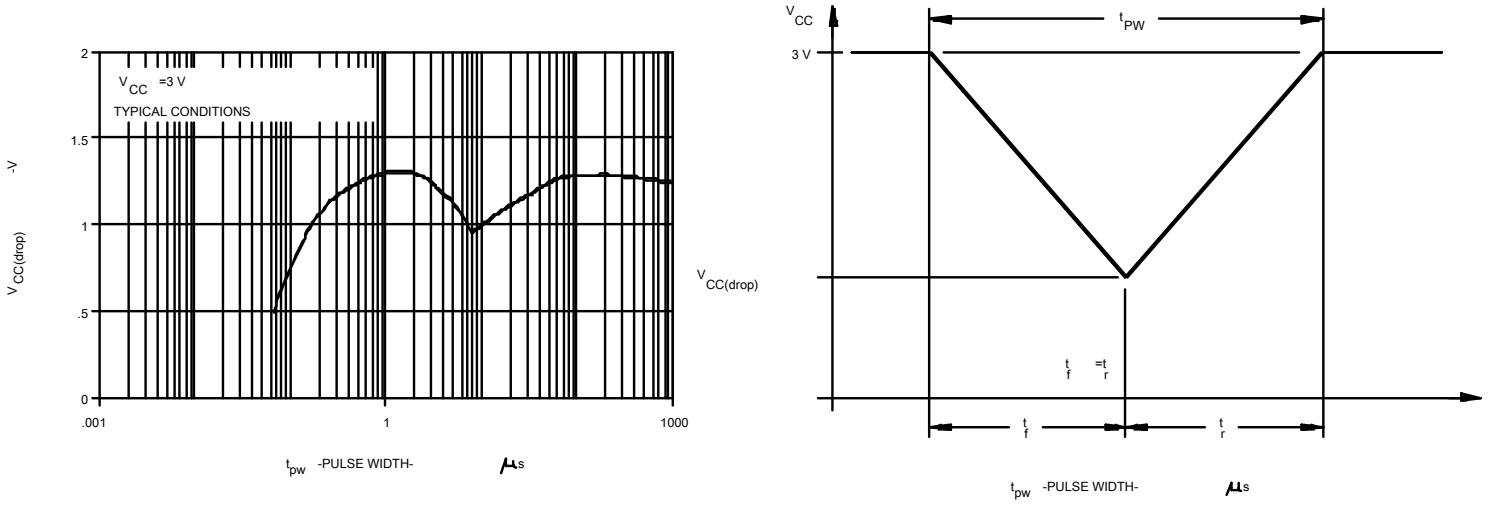


FIGURE 8. $V_{CC(drop)}$ level with a Triangle voltage drop to generate a POR/Brownout signal.

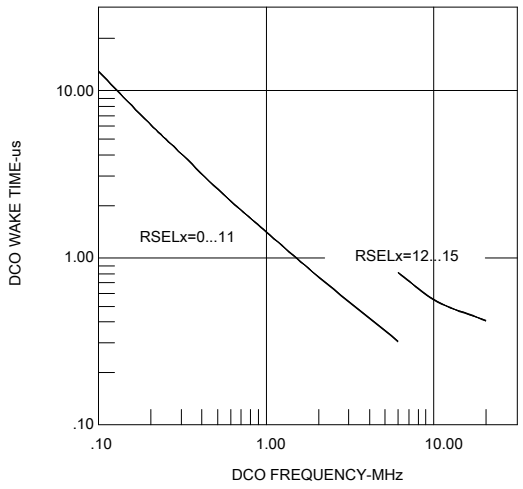


FIGURE 9. DCO wake-up time from LPM3/4 vs DCO frequency.

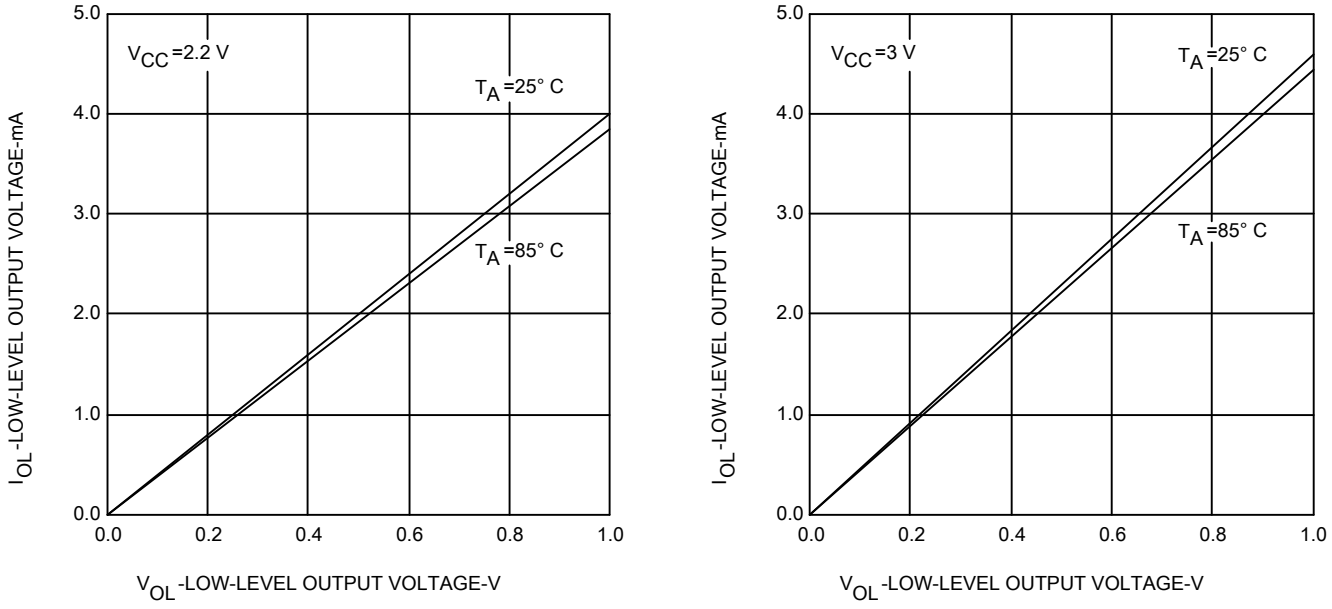


FIGURE 10. USI low level output voltage vs output current.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Transport media	Vendor part number
V62/12620-01XE	01295	G230EP	Tape and real	MSP430G2230QDREP
			Tube	MSP430G2230QREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243