

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update document paragraphs to current requirements. - ro	18-08-09	C. SAFFLE
B	Add ANSI SEMI standard G30-88 reference to paragraph 2.0. Under Table I, add typical limits to Vos, PSRR, Ib, Ios, CMRR, AoL, ISD, and Iq test parameters. Update document to requirements. - ro	24-01-10	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

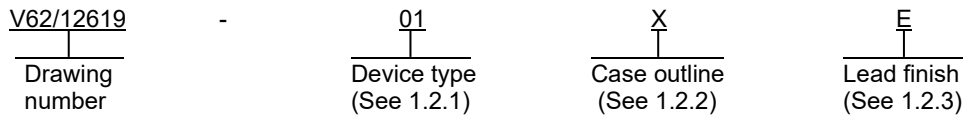
REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B									
SHEET	1	2	3	4	5	6	7	8	9	10	11									

PMIC N/A Original date of drawing YY-MM-DD 12-07-31	PREPARED BY RICK OFFICER		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime	
	CHECKED BY RAJESH PITHADIA		TITLE MICROCIRCUIT, LINEAR, OPERATIONAL AMPLIFIER, LOW POWER, PRECISION, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE		DWG NO. V62/12619	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power precision operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	OPA211-EP	Low power precision operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MO-187-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage (VS = +V - -V)	40 V
Input voltage (VIN)	-V – 0.5 V to +V + 0.5 V
Input current (any pin except power supply pins)	±10 mA
Output short circuit	Continuous 2/
Storage temperature range (TSTG)	-65°C to +150°C
Junction temperature range (TJ)	200°C
Electrostatic discharge (ESD) ratings:	
Human body model (HBM)	3000 V
Charged device model (CDM)	1000 V

1.4 Recommended operating conditions. 3/

Supply voltage	±2.25 V to ±18 V
Operating free-air temperature range (TA)	-55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient 4/	θ_{JA}	184.9	°C/W
Thermal resistance, junction-to-case (top) 5/	$\theta_{JC(TOP)}$	71.2	°C/W
Thermal resistance, junction-to-board 6/	θ_{JB}	104.9	°C/W
Characterization parameter, junction-to-top 7/	ψ_{JT}	11.5	°C/W
Characterization parameter, junction-to-board 8/	ψ_{JB}	103.4	°C/W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Short circuit to VS / 2 (ground in symmetrical dual supply setups), one amplifier per package.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 4/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- 5/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- 6/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.
- 7/ Characterization parameter, junction-to-top (ψ_{JT}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- 8/ Characterization parameter, junction-to-board (ψ_{JB}) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

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2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available from <https://www.ansi.org>.)

JEDEC Solid State Technology Association

- EIA/JESD 51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- EIA/JESD 51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u> VS = ±2.25 V to ±18 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Offset voltage section.							
Input offset voltage	VOS	VS = ±15 V	+25°C	01		±100	μV
					±20 typical		
			-55°C to +125°C			±180	
Input offset voltage drift	$\Delta V_{OS} / \Delta T$		-55°C to +125°C	01	0.35	typical	μV/°C
Input offset voltage versus power supply	PSRR	VS = ±2.25 V to ±18 V	+25°C	01		0.5	μV/V
					0.1 typical		
			-55°C to +125°C			3	
Input bias current section.							
Input bias current	IB	VCM = 0 V	-55°C to +125°C	01		±200	nA
						±50 typical	
Offset current	IOS	VCM = 0 V	-55°C to +125°C	01		±150	nA
						±20 typical	
Noise section.							
Input voltage noise	en	f = 0.1 Hz to 10 Hz	+25°C	01	80	typical	nVPP
Input voltage noise density	en	f = 10 Hz	+25°C	01	2	typical	nV / √Hz
		f = 100 Hz			1.4	typical	
		f = 1 kHz			1.1	typical	
Input current noise density	In	f = 10 Hz	+25°C	01	3.2	typical	nV / √Hz
		f = 1 kHz			1.7	typical	
Input voltage range.							
Common mode voltage range	VCM	VS ≥ ±5 V	+25°C	01	(-V) + 1.8	(+V) - 1.4	V
		VS < ±5 V			(-V) + 2	(+V) - 1.4	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> VS = ±2.25 V to ±18 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit	
					Min	Max		
Input voltage range - continued.								
Common mode rejection ratio	CMRR	VS ≥ ±5 V, (-V) + 2 V ≤ VCM (+V) - 2 V	-55°C to +125°C	01	114		dB	
					120 typical			
		VS < ±5 V, (-V) + 2 V ≤ VCM (+V) - 2 V			108			
					120 typical			
Input impedance.								
Differential		<u>3/</u>	+25°C	01	20k 8 typical		Ω pF	
Common mode		<u>3/</u>	+25°C	01	10 ⁹ 2 typical		Ω pF	
Open loop gain.								
Open loop voltage gain	AOL	(-V) + 0.2 V ≤ VO ≤ (+V) - 0.2 V, RL = 10 kΩ	-55°C to +125°C	01	114		dB	
					130 typical			
		(-V) + 0.6 V ≤ VO ≤ (+V) - 0.6 V, RL = 600 Ω			+25°C	110		
					114 typical			
Open loop gain over temperature	AOL	(-V) + 0.6 V ≤ VO ≤ (+V) - 0.6 V, IO ≤ 15 mA	-55°C to +125°C	01	110		dB	
					(-V) + 0.6 V ≤ VO ≤ (+V) - 0.6 V, 15 mA < IO < 30 mA	103		
Frequency response.								
Gain bandwidth product	GBW	G = 100	+25°C	01	80 typical		MHz	
		G = 1			45 typical			
Slew rate	SR		+25°C	01	27 typical		V/μs	
Settling time, 0.01%	ts	VS = ±15 V, G = -1, 10 V step, CL = 100 pF	+25°C	01	400 typical		ns	
Settling time, 0.0015% (16 bit)	ts	VS = ±15 V, G = -1, 10 V step, CL = 100 pF	+25°C	01	700 typical		ns	
Overload recovery time		G = -10	+25°C	01	500 typical		ns	
Total harmonic distortion + noise	THD + N	G = +1, f = 1 kHz, VO = 3 VRMS, RL = 600 Ω	+25°C	01	0.000015 typical		%	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> Vs = ±2.25 V to ±18 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Output							
Voltage output	VOUT	RL = 10 kΩ, AOL ≥ 114 dB	-55°C to +125°C	01	(-V) + 0.2	(+V) - 0.2	V
		RL = 600 Ω, AOL ≥ 110 dB	+25°C		(-V) + 0.6	(+V) - 0.6	
		IO < 15 mA, AOL ≥ 110 dB	-55°C to +125°C		(-V) + 0.6	(+V) - 0.6	
Short circuit current	ISC		+25°C	01	+30/-45 typical		mA
Open loop output impedance	ZO	f = 1 MHz	+25°C	01	5 typical		Ω
Shutdown.							
Shutdown pin input <u>4/</u> voltage		Device disabled (shutdown)	+25°C	01	(+V) - 0.35		V
		Device enabled				(+V) - 3	
Shutdown pin leakage current			+25°C	01	1 typical		μA
Turn on time			+25°C	01	2 typical		μs
Turn off time			+25°C	01	3 typical		μs
Shutdown current	ISD	Shutdown (disabled)	+25°C	01		20	μA
					1 typical		
Power supply.							
Specified voltage	Vs		+25°C	01	±2.25	±18	V
Quiescent current (per channel)	IQ	IOUT = 0 A	+25°C	01		4.5	mA
					3.6 typical		
			-55°C to +125°C			6	
Temperature range.							
Operating range	TA			01	-55	+125	°C
Thermal resistance	θJA		+25°C	01	200 typical		°C/W

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, RL = 10 kΩ connected to midsupply and VCM = VOUT = midsupply.

3/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

4/ When disabled, the output assumes a high impedance state.

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Case X

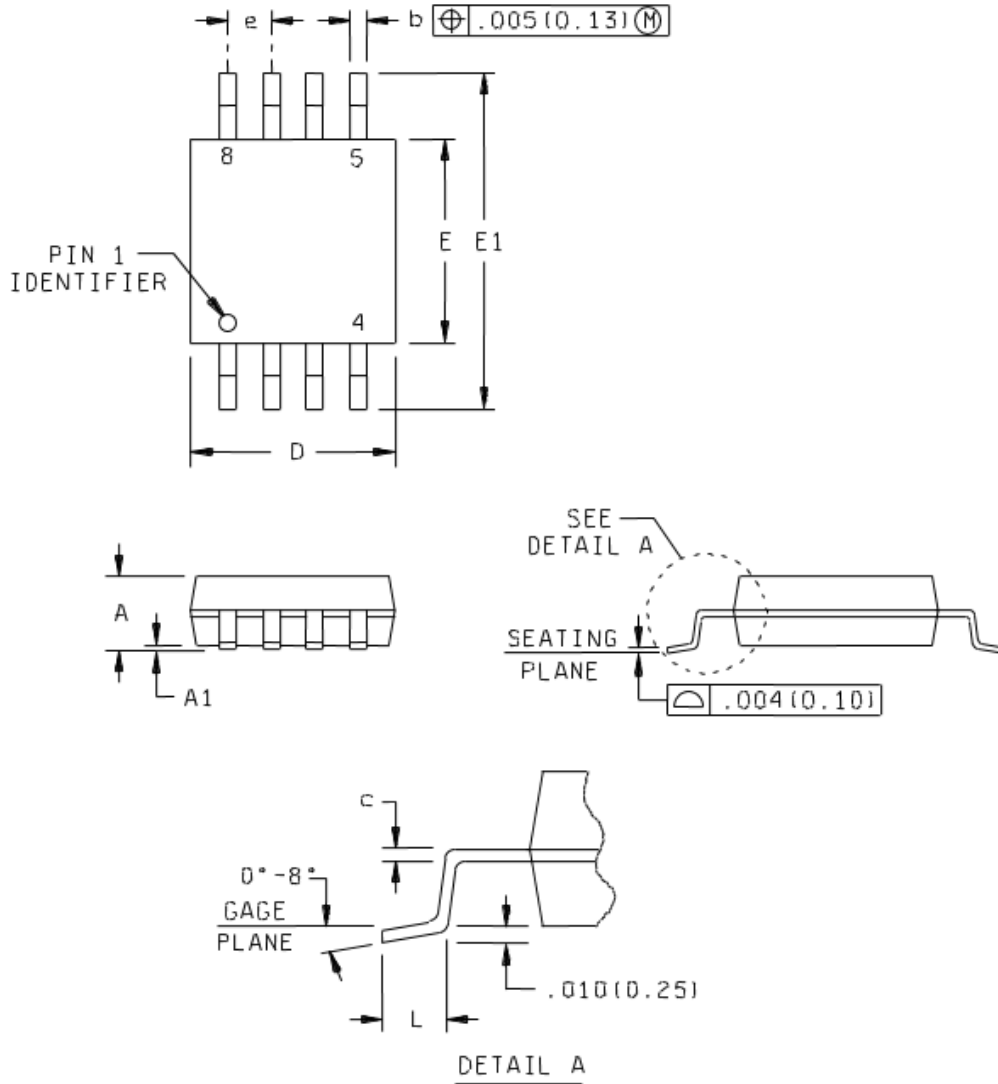


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.043	---	1.10
A1	0.001	0.006	0.05	0.15
b	0.010	0.014	0.25	0.38
c	0.005	0.009	0.13	0.23
D	0.114	0.122	2.90	3.10
E	0.114	0.122	2.90	3.10
E1	0.187	0.199	4.75	5.05
e	0.026 BSC		0.65 BSC	
L	0.015	0.027	0.40	0.70

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.50 mm (0.019 inch) per side.
4. Falls with JEDEC MO-187-AA, except interlead flash.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	NC SEE NOTE 1
2	-INPUT
3	+INPUT
4	-V
5	NC SEE NOTE 1
6	OUTPUT
7	+V
8	SHUTDOWN SEE NOTE 2

NOTES:

1. NC denotes no internal connection.
2. Shutdown function: Device enabled: $(-V) \leq V_{SHUTDOWN} \leq (+V) - 3 V$
 Device disabled: $V_{SHUTDOWN} \geq (+V) - 0.35 V$

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/ 2/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/12619-01XE	01295	OBCM	OPA211MDGKTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer’s data sheet.

CAGE code

01295

Source of supply

Texas Instruments, Incorporated
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243

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