REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add top side marking in section 6.3.-phn	13-03-21	Thomas M. Hess
B	Correct part number in section 6.3. - phn	14-05-05	Thomas M. Hess
C	Corret the operating temperature range in Section 1.1 and 1.4. Update boilerplate to current MIL-PRF-38535 requirements. - PHN	19-02-05	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		C	C	C	C	C	C	C	C	C	C	C	C							
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12							

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY MM DD 12-04-24	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, 200 MHz GENERAL PURPOSE CLOCK BUFFER, PCI-X COMPLIANT, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12618**
	REV **C**	**PAGE** 1 **OF** 12

AMSC N/A

5962-V038-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 200 MHz general purpose clock buffer, PCI-X compliant microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12618	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	CDCV304-EP	200 MHz general purpose clock buffer, PCI-X compliant

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{DD}) ..... -0.5 V to 4.3 V
Input voltage range, (V_I) ..... -0.5 V to V_{DD} + 0.5 V 2/ 3/
Output voltage range, (V_O) ..... -0.5 V to V_{DD} + 0.5 V 2/ 3/
Input clamp current, (I_{IK}) (v_I < 0 or V_I > V_{DD}) ..... ±50 mA
Output clamp current, (I_{OK}) (V_O < 0 or V_O >V_{DD}) ..... ±50 mA
Continuous total output current, (I_O) (V_O = 0 to V_{DD}) ..... ±50 mA
Storage temperature range (Tstg) ..... -65°C to 150°C

Thermal information 4/

Case X		Unit
Junction to ambient thermal resistance (θ_{JA}) 5/	157.8	°C/W
Junction to case (top) thermal resistance (θ_{JA}) 6/	61.8	
Junction to board thermal resistance (θ_{JA}) 7/	104.3	
Junction to top characterization parameter (Ψ_{JT}) 8/	7.7	
Junction to board characterization parameter (Ψ_{JB}) 9/	102.6	

1.4 Recommended operating conditions.

Supply voltage, (V_{DD}) ..... 2.3 V to 3.6 V
Low level input voltage, (V_{IL}) ..... 0.3 x V_{DD} V maximum
High level input voltage, (V_{IH}) ..... 0.7 x V_{DD} V minimum
High level output current, (I_{OH}):
V_{DD} = 2.5 V ..... -12 mA maximum
V_{DD} = 3.3 V ..... -24 mA maximum
Low level output current, (I_{OL}):
V_{DD} = 2.5 V ..... 12 mA maximum
V_{DD} = 3.3 V ..... 24 mA maximum
Operating free air temperature, (T_A) ..... -40°C to 105°C
Clock frequency (f_{clk}) ..... 0 to 200 MHz

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
3/ This value is limited to 4.6 V maximum.
4/ For more information about tradition and new thermal metrics, see manufacturer data.
5/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC standard, high K board, as specified in JESD51-7, in an environment described in JESD51-2a.
6/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard exists, but a close description can be found in the ANSI SEMI standard G30-88.
7/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
8/ The Junction to top characterization parameter , Ψ_{JT}, estimates the junction temperature of a device in a real system and in extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a.
9/ The Junction to board characterization parameter , Ψ_{JB}, estimates the junction temperature of a device in a real system and in extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Junction-to-board thermal resistance Theta-JB or RθJB.

Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Terminal function. The terminal function shall be as shown in figure 4.

3.5.5 Test load circuit. The test load circuit shall be as shown in figure 5.

3.5.6 Voltage waveforms propagation delay (t_{pd}) measurements. The Voltage waveforms propagation delay (t_{pd}) measurements shall be as shown in figure 6.

3.5.7 Output skew. The output skew shall be as shown in figure 7.

3.5.8 Clock waveform. The clock waveform shall be as shown in figure 8.

3.5.9 Supply current vs frequency. The supply current vs frequency shall be as shown in figure 9.

3.5.10 High level output voltage vs high level output current. The high level output voltage vs high level output current shall be as shown in figure 10.

3.5.11 Low level output voltage vs low level output current. The low level output voltage vs low level output current shall be as shown in figure 11.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Input voltage	V_{IK}	V_{DD} = 3 V, I_I = -18 mA		-1.2	V
High level output voltage	V_{OH}	V_{DD} = 2.3 V, I_{OH} = -8 mA	1.78		V
		V_{DD} = min to max, I_{OH} = -1 mA	V_{DD} – 0.3		
		V_{DD} = 3 V, I_{OH} = -24 mA	1.9		
		V_{DD} = 3 V, I_{OH} = -12 mA	2.3		
Low level output voltage	V_{OH}	V_{DD} = 2.3 V, I_{OL} = 8 mA		0.51	V
		V_{DD} = min to max, I_{OL} = 1 mA		0.2	
		V_{DD} = 3 V, I_{OL} = 24 mA		0.84	
		V_{DD} = 3 V, I_{OL} = 12 mA		0.60	
High level output current	I_{OH}	V_{DD} = 3 V, V_O = 1 V	-45		mA
		V_{DD} = 3.3 V, V_O = 1.65 V	-55 TYP		
Low level output current	I_{OL}	V_{DD} = 3 V, V_O = 2 V	54		
		V_{DD} = 3.3 V, V_O = 1.65 V	70 TYP		
Input current	I_I	V_I = V_O or V_{DD}		±5	µA
Dynamic current, See Figure 9.	I_{DD}	f = 67 MHz, V_{DD} = 2.7 V		28	mA
		f = 67 MHz, V_{DD} = 3.6 V		37	
Input capacitance	C_I	V_{DD} = 3.3 V, V_O = 0 V or V_{DD}	3 TYP		pF
Output capacitance	C_O	V_{DD} = 3.3 V, V_O = 0 V or V_{DD}	3.2 TYP		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Switching characteristics for V_{DD} = 2.5 V ±10%, C_L = 10 pF (unless otherwise noted)					
Low to high propagation delay	t_{PLH}	See figure	2	4.5	ns
High to low propagation delay	t_{PHL}		2	4.5	
Output skew 3/	$t_{sk(o)}$	See figure		150	ps
Output rise slew rate	t_r		1	4	V/ns
Output fall slew rate	t_f		1	4	
Switching characteristics for V_{DD} = 3.3±10%, C_L = 10 pF (unless otherwise noted)					
Low to high propagation delay	t_{PLH}	See figure	1.8	3.8	ns
High to low propagation delay	t_{PHL}		1.8	3.8	
Output skew 3/	$t_{sk(o)}$	See figure		100	ps
Additive phase jitter from input to output 1Y0	t_{jitter}	12 kHz to 5 MHz, f_{out} = 30.72 MHz	63 TYP		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz	56 TYP		
Pulse skew	$t_{sk(p)}$		180 TYP		ps
Process skew	$t_{sk(pr)}$		0.2 TYP		ns
Part to part skew	$t_{sk(pp)}$		0.25 TYP		
Clock high time, See figure 8.	t_{high}	66 MHz	6		
		140 MHz	2.2		
Clock low time, See figure 8.	t_{low}	66 MHz	6		
		140 MHz	3		
Output rise slew rate 4/	t_r	V_O = 0.4 V to 2 V	1.5	4	V/ns
Output rise fall rate 4/	t_f	V_O = 2 V to 0.4 V	1.5	4	

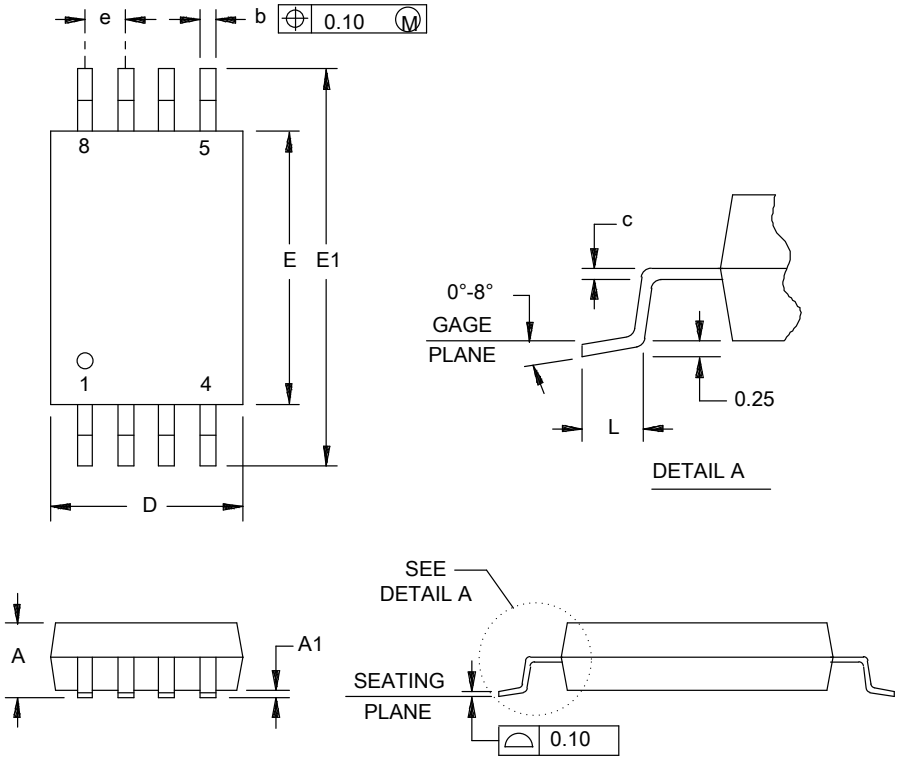
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating free air temperature range (unless otherwise noted). All typical values are with respect to nominal V_{DD} and T_A = 25°C.

3/ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs and T_A = -40°C to 85°C

4/ This symbol is according to PCI-X terminology.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	2.90	3.10			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side
5. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CLKIN	5	1Y1
2	OE	6	VDD
3	1Y0	7	1Y2
4	GND	8	1Y3

FIGURE 2. Terminal connections.

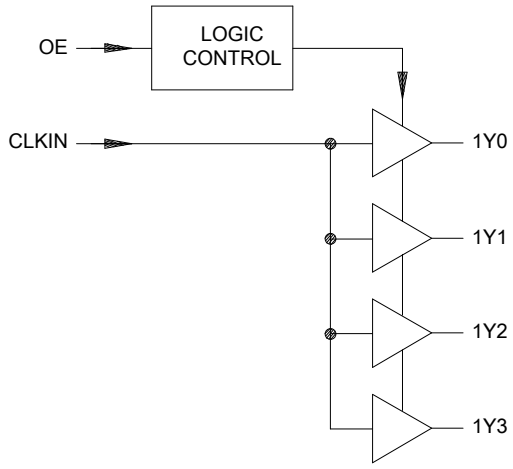


FIGURE 3. Functional block diagram.

Terminal		I/O	Description
Name	No.		
1Y[0:3]	3, 5, 7, 8	O	Buffered output clocks
CLKIN	1	I	Input reference frequency
GND	4	Power	Ground
OE	2	I	Output enable control
V_{DD}	6	Power	Supply

FIGURE 4. Terminal function.

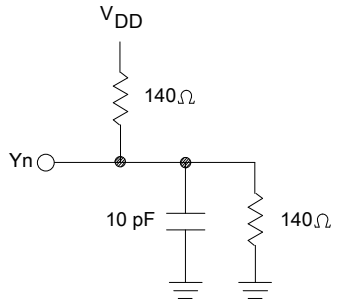


FIGURE 5. Test load circuit.

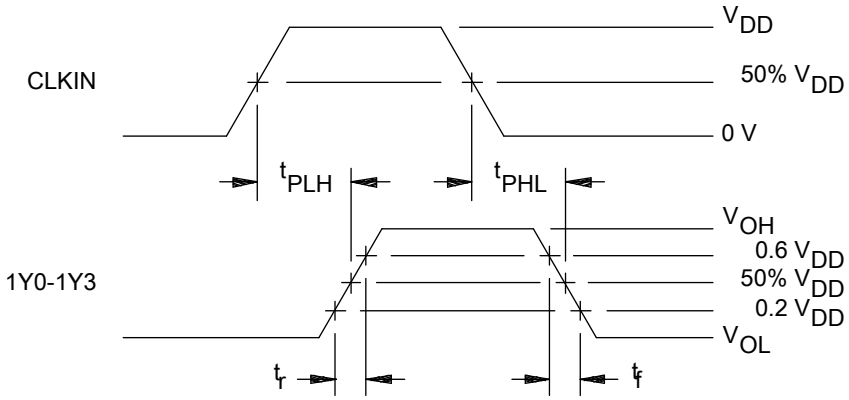


FIGURE 6. Voltage waveforms propagation delay (t_{pd}) measurements.

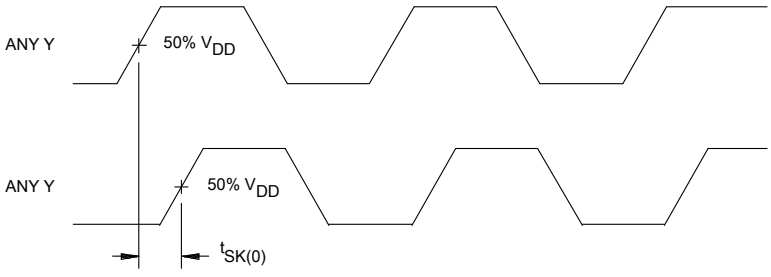
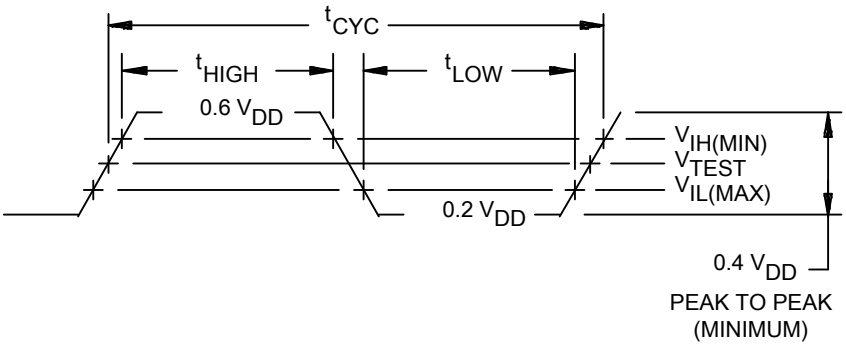


FIGURE 7. Output skew

PARAMETER	VALUE	UNIT
$V_{IH(MIN)}$	0.5 V_{DD}	V
$V_{IL(MAX)}$	0.35 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V



NOTE:
1. All parameters in this figure are according to PCI-X 1.0 specifications.

FIGURE 8. Clock waveform.

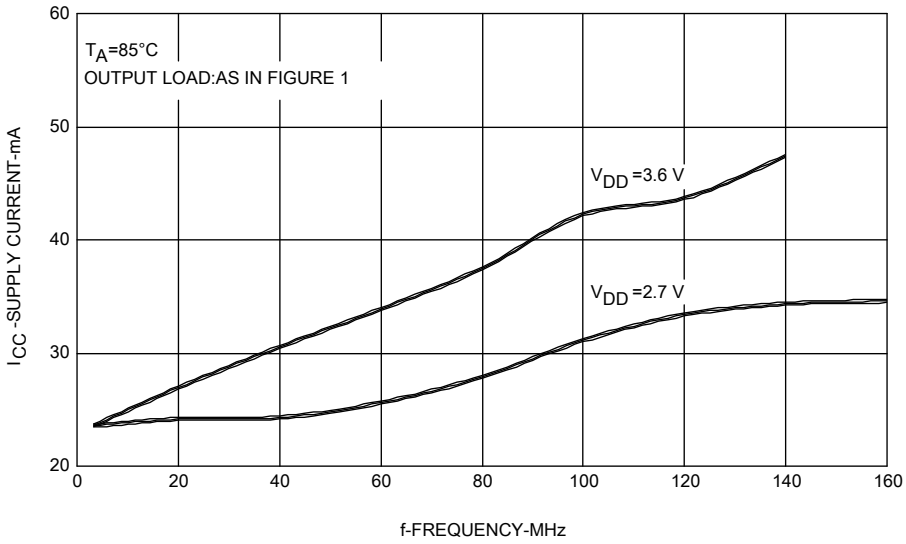


FIGURE 9. Supply current vs Frquency.

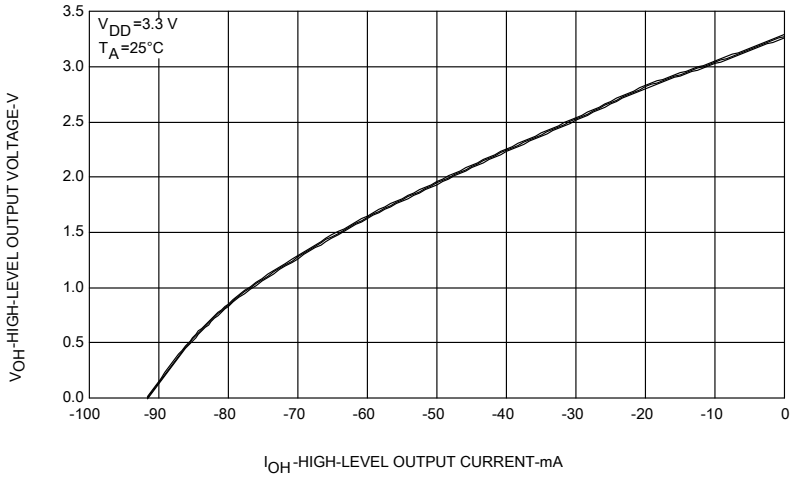


FIGURE 10. High level output voltage vs high level output current.

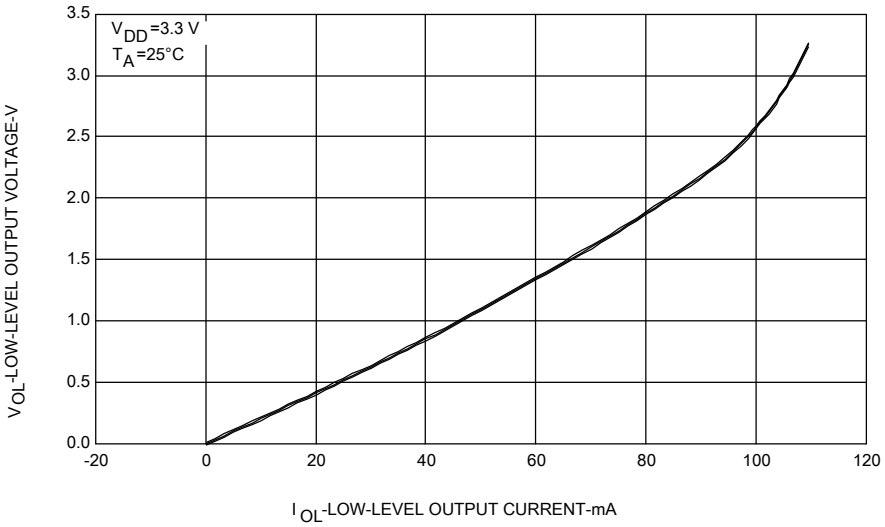


FIGURE 11. Low level output voltage vs low level output current.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/12618-01XE	01295	CDCV304TPWREP	CDCV304-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243