

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct the operating temperature range in section 1.3 and the pin out in section 1.2.2. - phn	12-09-20	Thomas M. Hess
B	Add lead finish "E" to the devices. - PHN	18-03-08	Thomas M. Hess
C	Under Table I, make correction by deleting temperature range condition of -40°C to +125°C and replacing with -55°C to +125°C. Under Table I, add conditions to both Input current tests. Under Table I, with condition of VDD = 12 V; make corrections to condition column for RFLAT(ON), IS(Off), IS(Off), IS(On), ID(On) tests. Update document paragraphs to current requirements. - ro	23-06-15	James R. Eschmeyer



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

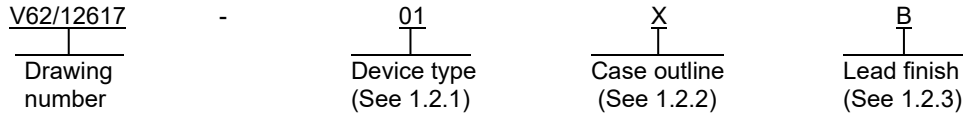
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15					

PMIC N/A Original date of drawing 12-04-09	PREPARED BY Phu H. Nguyen					DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime									
	CHECKED BY Phu H. Nguyen					TITLE MICROCIRCUIT, DIGITAL, LOW CAPACITANCE, LOW CHARGE INJECTION, ±15 V / +12 V iCMOS QUAD SPST SWITCHES, MONOLITHIC SILICON									
	APPROVED BY Thomas M. Hess					DWG NO. V62/12617									
	SIZE A		CAGE CODE 16236			PAGE 1 OF 15									
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low capacitance, low charge injection, $\pm 15\text{ V} / +12\text{ V}$ industrial complementary metal oxide semiconductor (iCMOS) quad single pole single throw (SPST) switches microcircuit, with an operating temperature range of -55°C to $+125^{\circ}\text{C}$.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADG1212-EP	Low capacitance, low charge injection, $\pm 15\text{ V} / +12\text{ V}$ iCMOS quad SPST switches

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MO-153-AB	Lead thin shrink small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Positive power supply (VDD) to Negative power supply (VSS)	35 V
VDD to GND	-0.3 V to +35 V
VSS to GND	+0.3 V to -25 V
Analog inputs	VSS - 0.3 V to VDD + 0.3 V 2/ or 30 mA which ever occurs first
Digital inputs	GND - 0.3 V to VDD + 0.3 V 2/ or 30 mA which ever occurs first
Peak current, Source (S) or Drain (D)	100 mA (pulsed at 1 ms, 10% duty cycles max)
Continuous current per channel, S or D	25 mA
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
16 lead TSSOP, θ_{JA} Thermal impedance (4 layer board)	112°C/W
Lead temperature, soldering	As per JEDEC J-STD 020

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- J-STD-020 – Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Copies of these documents are available online at <https://www.jedec.org>.)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Off leakage. The off leakage shall be as shown in figure 6.

3.5.7 On leakage. The on leakage shall be as shown in figure 7.

3.5.8 Off Isolation. The Off isolation shall be as shown in figure 8.

3.5.9 Channel-to-channel crosstalk. The channel-to-channel crosstalk shall be as shown in figure 9.

3.5.10 On Resistance. The on resistance shall be as shown in figure 10.

3.5.11 Bandwidth. The bandwidth shall be as shown in figure 11.

3.5.12 THD + Noise. The THD + Noise shall be as shown in figure 12.

3.5.13 Switching times. The switching times shall be as shown in figure 13.

3.5.14 Charge injection. The charge injection shall be as shown in figure 14.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits						Unit
			25°C		-40°C to +85°C		-55°C to +125°C		
			Min	Max	Min	Max	Min	Max	
Analog switch									
Analog signal range							VDD	to VSS	V
On Resistance	RON	VS = ±10 V, IS = -1 mA, see Figure 10, VDD = +13.5 V, VSS = -13.5 V	120	TYP					Ω
				190		230		260	
On Resistance match between channel	ΔRON	VS = ±10 V, IS = -1 mA	2.5	TYP					Ω
				6		10		11	
On Resistance flatness	RFLAT(ON)	VS = -5 V / 0 V / +5 V; IS = -1 mA	20	TYP					Ω
				57		72		79	
Leakage currents (VDD = +16.5 V, VSS = -16.5 V)									
Source off leakage	IS(Off)	VS = ±10 V, VD = ±10 V, see Figure 6	±0.02	TYP					nA
				±0.1		±0.6		±1	
Drain off leakage	ID(Off)	VS = ±10 V, VD = ±10 V, see Figure 6	±0.02	TYP					nA
				±0.1		±0.6		±1	
Channel on leakage	ID, IS (On)	VS = VD = ±10 V, see Figure 7	±0.02	TYP					nA
				±0.1		±0.6		±1	
Digital inputs									
Input high voltage	VINH						2.0		V
Input low voltage	VINL							0.8	V
Input current	IINL or IINH	VIN = VINL or VINH	0.005	TYP				±0.1	μA
Digital input capacitance	CIN		2.5	TYP					pF
Dynamic characteristics 3/									
Switch on time	tON	RL = 300 Ω, CL = 35 pF, VS = 10 V, see Figure 13	65	TYP					ns
				80		95		110	
Switch off time	tOFF	RL = 300 Ω, CL = 35 pF, VS = 10 V, see Figure 13	80	TYP					ns
				100		115		135	
Charge injection		VS = 0 V, RS = 0 Ω, CL = 1 nF, see Figure 14	-0.3	TYP					pC
Off isolation		RL = 50 Ω, CL = 5 pF, f = 1 MHz, see figure 8	80	TYP					dB
Channel to channel crosstalk		RL = 50 Ω, CL = 5 pF, f = 1 MHz, see figure 9	90	TYP					dB
Total harmonic distortion + Noise		RL = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz, see figure 12	0.15	TYP					%
-3 dB bandwidth		RL = 50 Ω, CL = 5 pF, see Figure 11	1000	TYP					MHz

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Limits						Unit
			25°C		-40°C to +85°C		-55°C to +125°C		
			Min	Max	Min	Max	Min	Max	
Dynamic characteristics - continued. <u>3/</u>									
Source off capacitance	CS(Off)	V _S = 0 V, f = 1 MHz		1.1					pF
Drain off capacitance	CD(Off)	V _S = 0 V, f = 1 MHz		1.2					pF
Drain on capacitance, Source on capacitance	CD, Cs (On)	V _S = 0 V, f = 1 MHz		3					pF
Power requirements (V _{DD} = +16.5 V, V _{SS} = -16.5 V)									
Positive supply current	I _{DD}	Digital inputs = 0 V or V _{DD}	0.001	TYP		1.0			μA
	I _{DD}	Digital inputs = 5 V	220	TYP		420			μA
Negative supply current	I _{SS}	Digital inputs = 0 V or V _{DD}	0.001	TYP		1.0			μA
	I _{SS}	Digital inputs = 5 V	0.001	TYP		1.0			μA

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 4/	Limits						Unit
			25°C		-40°C to +85°C		-55°C to +125°C		
			Min	Max	Min	Max	Min	Max	
Analog switch									
Analog signal range							0 V to	V _{DD}	V
On Resistance	R _{ON}	V _S = 0 V to 10 V, I _S = -1 mA, see Figure 10 V _{DD} = 10.8 V, V _{SS} = 0 V	300 TYP						Ω
				475		567		625	
On Resistance match between channel	ΔR _{ON}	V _S = 0 V to 10 V, I _S = -1 mA	4.5 TYP						Ω
				12		26		27	
On Resistance flatness	R _{FLAT(ON)}	V _S = 3 V / 6 V / 9 V, I _S = -1 mA	60 TYP						Ω
Leakage currents (V _{DD} = 13.2 V, V _{SS} = 0 V)									
Source off leakage	I _{S(Off)}	V _S = 1 V / 10 V, V _D = 10 V / 1 V, see Figure 6	±0.02 TYP						nA
				±0.1		±0.6		±1	
Drain off leakage	I _{D(Off)}	V _S = 1 V / 10 V, V _D = 10 V / 1 V, see Figure 6	±0.02 TYP						nA
				±0.1		±0.6		±1	
Channel on leakage	I _D , I _S (On)	V _S = V _D = 1 V or 10 V, see Figure 7	±0.02 TYP						nA
				±0.1		±0.6		±1	
Digital inputs									
Input high voltage	V _{INH}						2.0		V
Input low voltage	V _{INL}							0.8	V
Input current	I _{INL} or I _{INH}	V _{IN} = V _{INL} or V _{INH}	0.001 TYP					±0.1	μA
Digital input capacitance	C _{IN}		3 TYP						pF
Dynamic characteristics 3/									
Switch on time	t _{ON}	R _L = 300 Ω, C _L = 35 pF, V _S = 8 V, see Figure 13	80 TYP						ns
				105		125		140	
Switch off time	t _{OFF}	R _L = 300 Ω, C _L = 35 pF, V _S = 8 V, see Figure 13	90 TYP						ns
				115		140		165	
Charge injection		V _S = 6 V, R _S = 0 Ω, C _L = 1 nF, see Figure 14	0 TYP						pC
Off isolation		R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see figure 8	80 TYP						dB
Channel to channel crosstalk		R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, see figure 9	90 TYP						dB
-3 dB bandwidth		R _L = 50 Ω, C _L = 5 pF, see Figure 11	900 TYP						MHz

See footnote at end of table.

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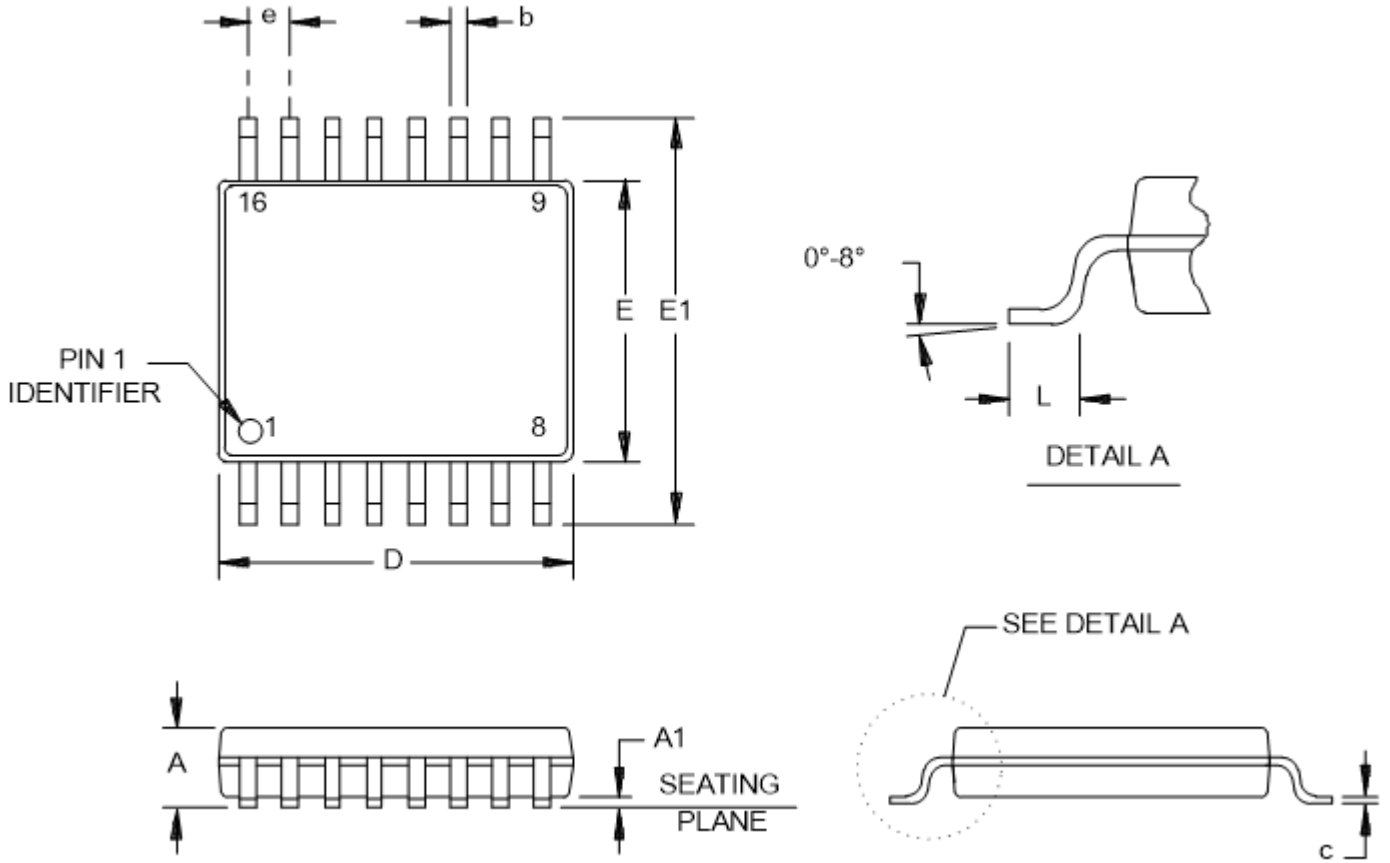
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>4/</u>	Limits						Unit
			25°C		-40°C to +85°C		-55°C to +125°C		
			Min	Max	Min	Max	Min	Max	
Dynamic characteristics - continued. <u>3/</u>									
Source off capacitance	CS(Off)	V _S = 6 V, f = 1 MHz		1.4					pF
Drain off capacitance	CD(Off)	V _S = 6 V, f = 1 MHz		1.5					pF
Drain on capacitance, Source on capacitance	CD, CS (On)	V _S = 6 V, f = 1 MHz		3.9					pF
Power requirements (V _{DD} = +13.2 V)									
Positive supply current	I _{DD}	Digital inputs = 0 V or V _{DD}	0.001	TYP		1.0			μA
Negative supply current	I _{SS}	Digital inputs = 5 V	220	TYP		420			μA

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ V_{DD} = 15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V, unless otherwise noted.
- 3/ Guaranteed by design, not subject to production test.
- 4/ V_{DD} = 12 V ±10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40	BSC
b	0.19	0.30	e	0.65	BSC
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:

1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-15-AB3.

FIGURE 1. Case outline.

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Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IN1	9	IN3
2	D1	10	D3
3	S1	11	S3
4	VSS	12	NC
5	GND	13	VDD
6	S4	14	S2
7	D4	15	D2
8	IN4	16	IN2

NOTES:

1. NC = No Connect. Do not connect to this pin.

FIGURE 2. Terminal connections.

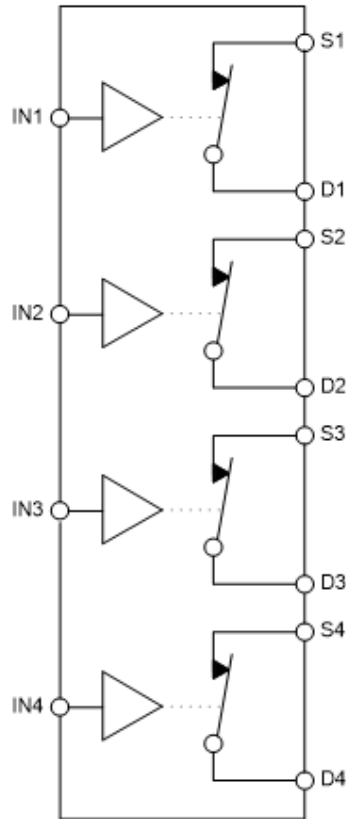
Case outline X		
Terminal		Description
Number	Mnemonic	
1	IN1	Logic control input.
2	D1	Drain terminal. This pin can be an input or output.
3	S1	Source terminal. This pin can be an input or output.
4	VSS	Most negative power supply potential.
5	GND	Ground (0 V) reference.
6	S4	Source terminal. This pin can be an input or output.
7	D4	Drain terminal. This pin can be an input or output.
8	IN4	Logic control input.
9	IN3	Logic control input.
10	D3	Drain terminal. This pin can be an input or output.
11	S3	Source terminal. This pin can be an input or output.
12	NC	No connection.
13	VDD	Most positive power supply potential.
14	S2	Source terminal. This pin can be an input or output.
15	D2	Drain terminal. This pin can be an input or output.
16	IN2	Logic control input.

FIGURE 3. Terminal function.

Input INx	Switch condition
1	On
0	Off

FIGURE 4. Truth table

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NOTES:

1. Switches shown are for logic 1 input.

FIGURE 5. Functional block diagram.

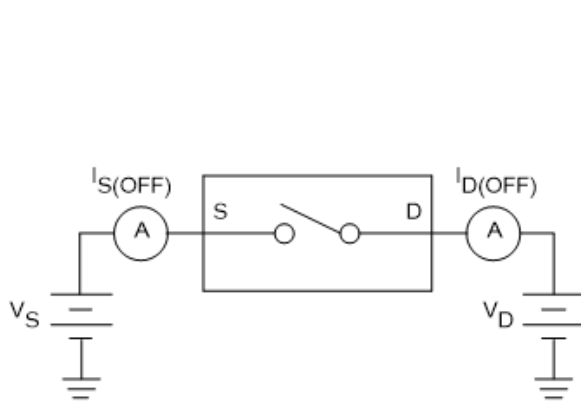


FIGURE 6. Off Leakage.

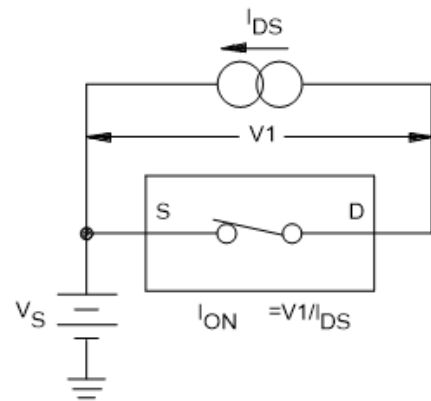
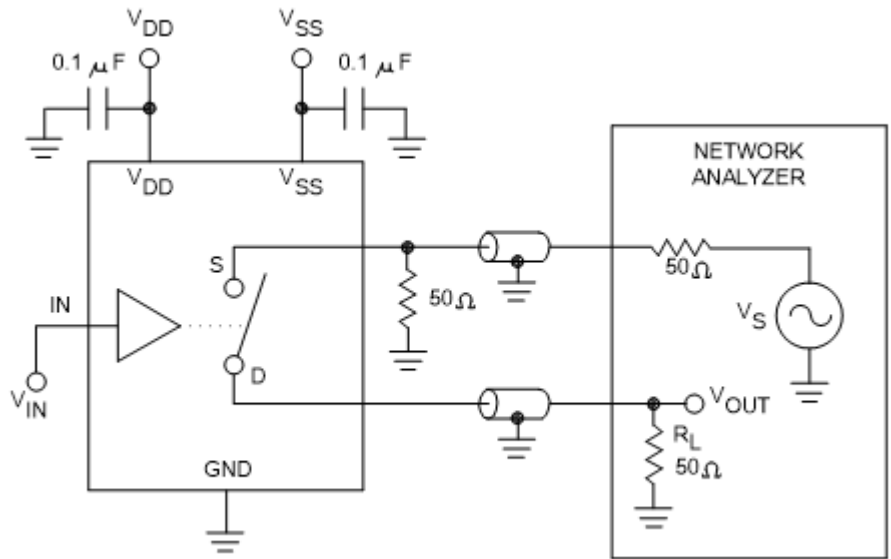


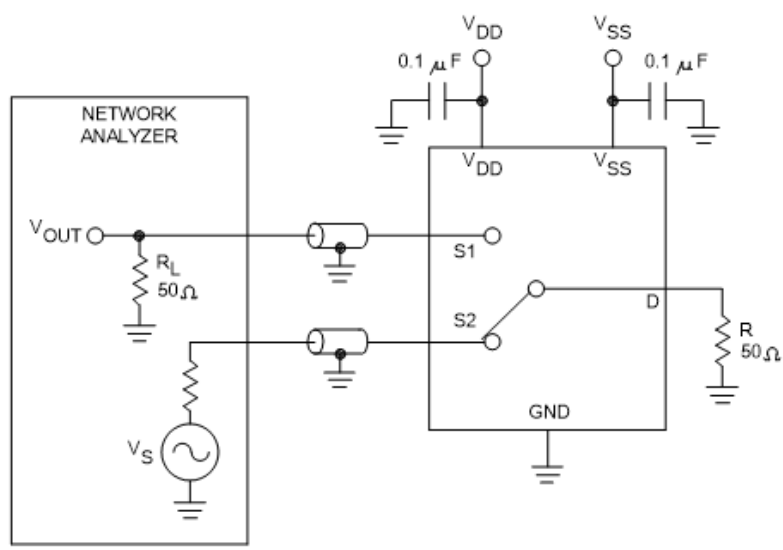
FIGURE 7. On Leakage

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$$\text{Off Isolation} = 20 \log \frac{V_{OUT}}{V_S}$$

FIGURE 8. Off isolation.



$$\text{Channel-to-channel crosstalk} = 20 \log \frac{V_{OUT}}{V_S}$$

FIGURE 9. Channel-to-channel crosstalk.

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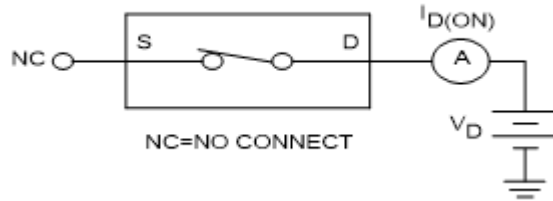
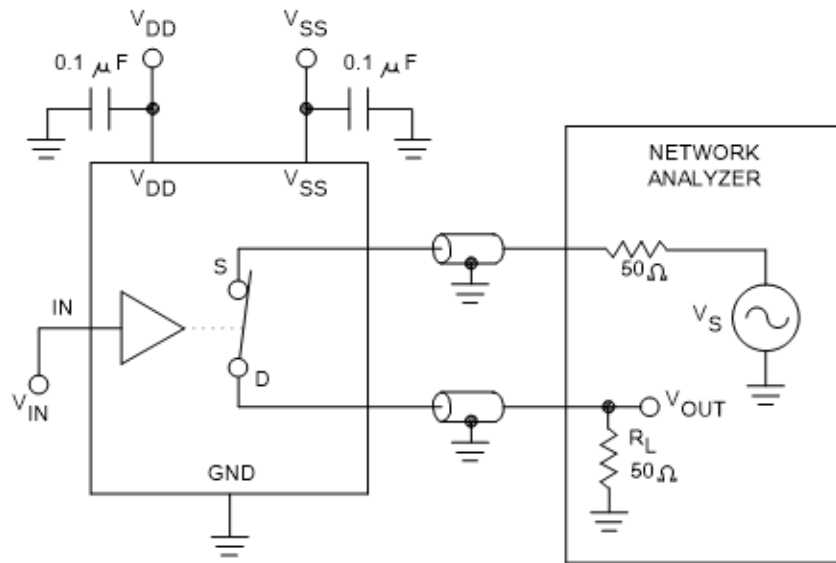


FIGURE 10. On resistance.



$$\text{Insertion loss} = 20 \log \frac{V_{\text{OUT WITH Switch}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

FIGURE 11. Bandwidth.

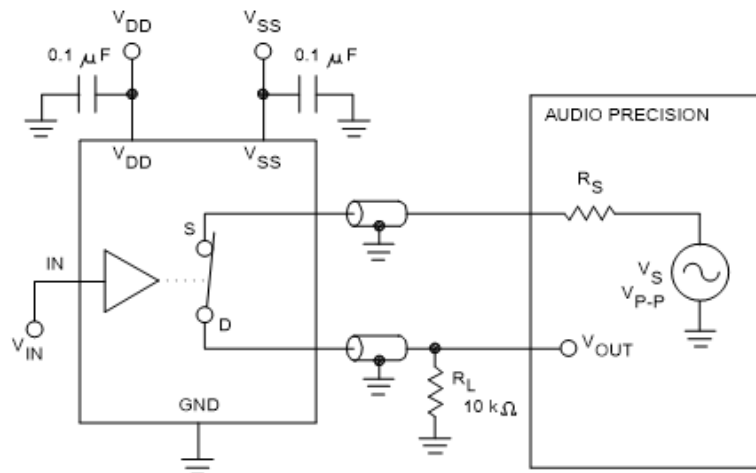


FIGURE 12. THD + Noise.

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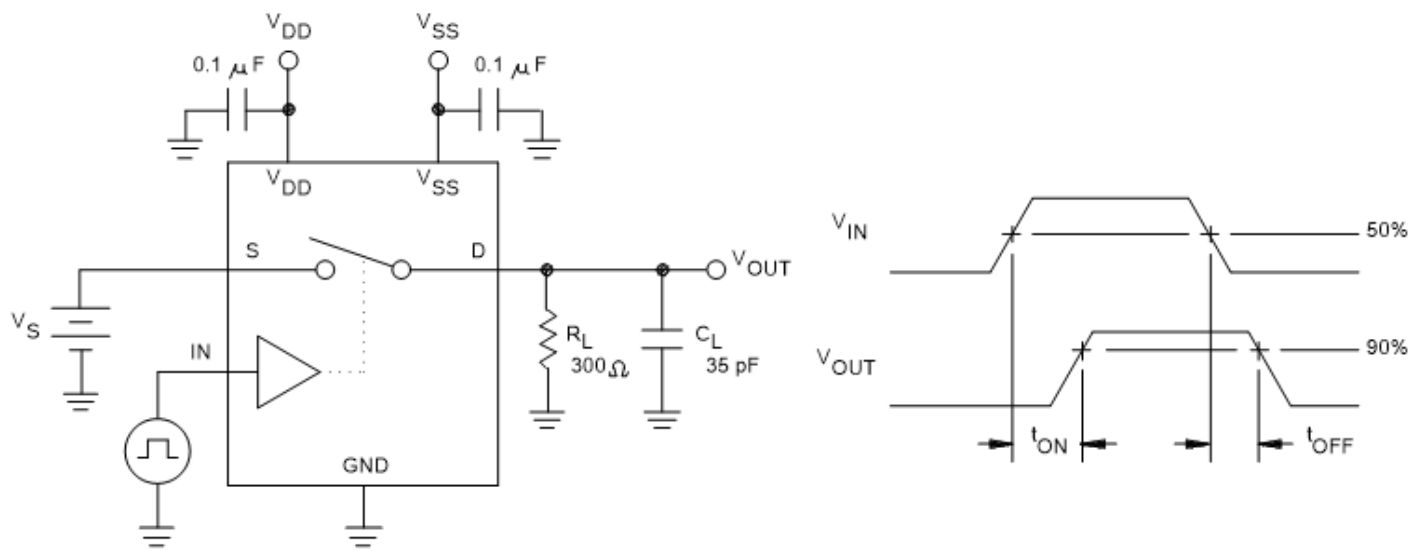


FIGURE 13. Switching times.

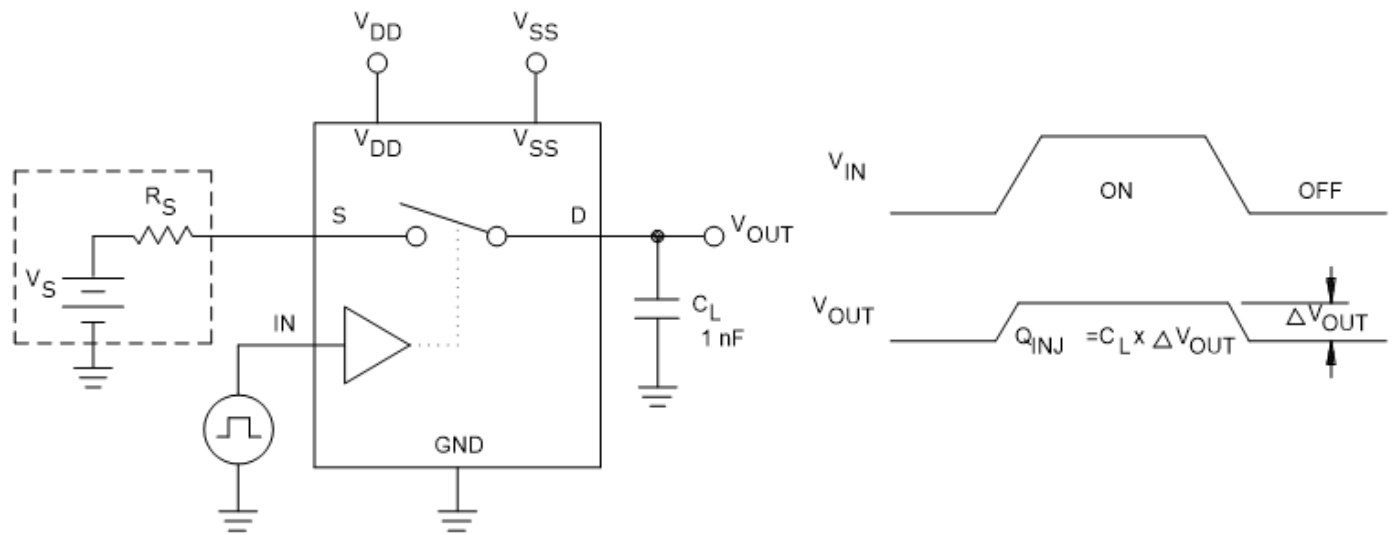


FIGURE 14. Charge injection.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number ^{1/}	Device manufacturer CAGE code	Vendor part number
V62/12617-01XB	24355	ADG1212SRU-EP-RL7
V62/12617-01XE	24355	ADG1212SRUZ-EP-RL7

^{1/} The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: 20 Alpha Road
 Chelmsford, MA 01824-4123

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