REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add lead finish “E” to the devices. - PHN	18-02-15	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - DRH	24-02-23	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	REV		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15				

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime
Original date of drawing YY MM DD 12-04-09	CHECKED BY Phu H. Nguyen APPROVED BY Thomas M. Hess	TITLE MICROCIRCUIT, DIGITAL, 1024-POSITION, DIGITAL POTENTIOMETER WITH MAXIMUM ±1% R-TOLERANCE ERROR AND 20-TP MEMORY, MONOLITHIC SILICON
	SIZE A / CODE IDENT. NO. 16236	DWG NO. V62/12616
	REV B	PAGE 1 OF 15

AMSC N/A

5962-V040-24

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1024-position, digital potential meter with maximum ±1% R-tolerance error and 20-TP memory microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12616	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5292-EP	1024-position, digital potential meter with maximum ±1% R-tolerance error and 20-TP memory

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MO-153-AB	Lead thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND ..... -0.3 V to +35 V
V_{SS} to GND ..... +0.3 V to -25 V
V_{LOGIC} to GND ..... -0.3 V to +7 V
V_{DD} to V_{SS} ..... 35 V
V_A, V_B, V_W to GND ..... V_{SS} -0.3 V, V_{DD} + 0.3 V
Digital input and output voltage to GND ..... -0.3 V to V_{LOGIC} + 0.3 V
EXT_CAP voltage to GND ..... -0.3 V to +7 V
IA, IB, IW
  Continuous ..... ±3 mA
  Pulsed 2/
    Frequency > 10 kHz ..... ±3/d 3/
    Frequency ≤ 10 kHz ..... ±3/√d 3/
Operating temperature range 4/ ..... -55°C to +125°C
Maximum Junction Temperature Range (T_J max) ..... 150°C
Storage temperature range ..... -65°C to 150°C
Reflow soldering
  Peak temperature ..... 260°C
  Time at peak temperature ..... 20 sec to 40 sec
Package power dissipation ..... (T_J max – T_A)/θ_{JA}
Thermal resistance

Case outline	θ_{JA}	θ_{JA}	Unit
Case X	93 5/	20	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JESD 51-2 – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Maximum terminal current is bounded by the maximum current handling of the switches, maximum poser dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
3/ Pulse duty factor.
4/ Includes programming of OTP memory.
5/ JEDEC 2S2P test board, still air (0 m/sec to 1 m/sec air flow).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Shift register content. The shift register content shall be as shown in figure 5.

3.5.6 Write timing diagram. The write timing diagram shall be as shown in figure 6.

3.5.7 Read timing diagram. The read timing diagram shall be as shown in figure 7.

3.5.8 Resistor position nonlinearity error. The resistor position nonlinearity error shall be as shown in figure 8.

3.5.9 Potentiometer divider nonlinearity error. The potentiometer divider nonlinearity error shall be as shown in figure 9.

3.5.10 Wiper resistance. The wiper resistance shall be as shown in figure 10.

3.5.11 Power supply sensitivity. The power supply sensitivity shall be as shown in figure 11.

3.5.12 Gain vs frequency. The gain vs frequency shall be as shown in figure 12.

3.5.13 Common mode leakage current. The common mode leakage current shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Device type	Limits		Unit
				Min	Max	
DC characteristics – Rheostat mode						
Resolution	N		All	10		Bits
Resistor differential nonlinearity 4/	R-DNL	R_{WB}, V_A = NC		-1	+1	LSB
Resistor integral nonlinearity 4/	R-INL	R_{AB} = 20 kΩ, $\|V_{DD} – V_{SS}\|$ = 26 V to 33 V		-2	+2	
		R_{AB} = 20 kΩ, $\|V_{DD} – V_{SS}\|$ = 26 V to 33 V		-3	+3	
Nominal resistor tolerance (R-Perf mode) 5/	$\Delta R_{AB}/R_{AB}$	7/		-1	+1	%
Nominal resistor tolerance (Normal mode) 6/	$\Delta R_{AB}/R_{AB}$			±7 TYP 3/		
Resistance temperature coefficient	$(\Delta R_{AB}/R_{AB})\Delta T \times 10^6$			35 TYP 3/		ppm/°C
Wiper resistance	R_W				100	Ω
DC characteristics – Potentiometer divider mode						
Resolution	N		All	10		Bits
Differential nonlinearity 8/	DNL			-1	+1	LSB
Integral nonlinearity 8/	INL			-2.5	+2.5	
Voltage divider temperature coefficient 6/	$(\Delta V_W/V_W)\Delta T \times 10^6$	Code = half scale		5 TYP 3/		ppm/°C
Full scale error	V_{WFSE}	Code = full scale		-8	+1	LSB
Zero scale error	V_{WZSE}	Code = zero scale		0	10	
Resistor terminals						
Terminal voltage range 9/	V_A, V_B, V_W		All	V_{SS}	V_{DD}	V
Capacitance A, Capacitance B 6/	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		85 TYP 3/		pF
Capacitance W 6/	C_W			65 TYP 3/		
Common mode leakage current 6/	I_{CM}	$V_A = V_B = V_W$		-120	+120	nA
Digital inputs						
Input logic high 6/	V_{IH}	V_{LOGIC} = 2.7 V to 5.5 V	All	2.0		V
Input logic low 6/	V_{IL}	V_{LOGIC} = 2.7 V to 5.5 V			0.8	
Input current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	µA
Input capacitance 6/	C_{IL}			5 TYP 3/		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Device type	Limits		Unit
				Min	Max	
Digital output (SDO and RDY)						
Output high voltage 6/	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}	All	V_{LOGIC} – 0.4		V
Output low voltage 6/	V_{OL}				GND + 0.4	
Three state leakage current				-1	+1	µA
Output capacitance 6/	C_{OL}			5 TYP 3/		pF
Power supplies						
Single supply power range	V_{DD}	V_{SS} = 0 V	All	9	33	V
Dual supply power range	V_{DD}/V_{SS}			±9	±16.5	V
Positive supply current	I_{DD}	V_{DD}/V_{SS} = ±16.5 V			2	µA
Negative supply current	I_{SS}	V_{DD}/V_{SS} = ±16.5 V		-2		µA
Logic supply range	V_{LOGIC}			2.7	5.5	V
Logic supply current	I_{LOGIC}	V_{LOGIC} =5 V, V_{IH} = 5 V or V_{IL} = GND			10	µA
OTP store current 6/ 10/	I_{LOGC_PROG}	V_{IH} = 5 V or V_{IL} = GND		25 TYP 3/		mA
OTP read current 6/ 11/	$I_{LOGIC\_FUSE\_READ}$	V_{IH} = 5 V or V_{IL} = GND		25 TYP 3/		mA
Power dissipation 12/	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND			110	µW
Power supply rejection ratio	PSSR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ±10%		0.103 TYP 3/		%/%
Dynamic characteristics 8/ 13/						
Bandwidth	BW	-3 dB	All	520 TYP 3/		
Total harmonic distortion	THD_W	V_A = 1Vrms, V_B = 0, f = 1 kHz		-93 TYP 3/		
V_W setting time	ts	VA = 30 V, VB = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF		750 TYP 3/		ns
		Code = full scale, normal mode		2.5 TYP 3/		µs
		Code = full scale, R-perf mode		2.5 TYP 3/		µs
		Code = half scale, normal mode		5 TYP 3/		µs
		Code = half scale, R-Perf mode				
Resistor noise density	e_{N_WB}	Code = half scale		10 TYP 3/		nV/√Hz

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 14/	Device type	Limits 15/		Unit
				Min	Max	
Interface timing specifications						
SCLK cycle time	t_1 16/		All	20		ns
SCLK high time	t2			10		
SCLK low time	t3			10		
$\overline{SYNC}$ to SCLK falling edge setup time	t4			10		
Data setup time	t5			5		
Data hold timw	t6			5		
SCLK falling edge to $\overline{SYNC}$ rising edge	t7			1		
Minimum $\overline{SYNC}$ high time	t8			400 17/		
$\overline{SYNC}$ rising edge to next SCLK fall ignore	t9			14		
RDY rising edge to $\overline{SYNC}$ falling edge	t_{10} 18/			1		
$\overline{SYNC}$ rising edge to RDY fall time	t_{11} 18/				40	
RDY low time, RDAC register write command execute time (R-Perf mode)	t_{12} 18/				2.4	µs
RDY low time, RDAC register write command execute time (normal mode)					419	ns
RDY low time, memory program execute time					8	ms
Software/hardware reset				1.5		ms
RDY low time, RDAC register readback execute time	t_{13} 18/				450	ns
RDY low time, memory readback execute time					1.3	ms
SCLK rising edge to SDO valid	t_{14} 18/				450	ns
Minimum $\overline{RESET}$ pulse width (asynchronous)	t_{RESET}			20		ns
Power on OTP restore time	$t_{POWER-UP}$ 19/				2	ms

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 21 V to 33 V, V_{SS} = 0V; V_{DD} = 10.5 V to 16.5 V, V_{SS} = -10.5 V to -16.5 V; V_{LOGIC} = 2.7 V to 5.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, -55°C < T_A < +125°C, unless otherwise noted.

3/ Typical values represent average readings at 25°C, V_{DD} = 15 V, V_{SS} = -15 V, and V_{LOGIC} = 5V.

4/ Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between R_{WB} at code 0x00B and code 0x3FF or between R_{WA} at code 0x3F3 and code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for VA < 12 V and 1.2 mA for VA ≥ 12 V.

5/ Resistor performance mode. The terms resistor performance mode and R-Perf mode are used interchangeably.

6/ Guaranteed by design and characterization, not subject to production test.

7/ Resistor performance mode code range

Resistor Tolerance per Code	-55°C < T_A < +125°C							
	$\|V_{DD} - V_{SS}\|$ = 30 V to 33V		$\|V_{DD} - V_{SS}\|$ = 26 V to 30V		$\|V_{DD} - V_{SS}\|$ = 22 V to 26V		$\|V_{DD} - V_{SS}\|$ = 21 V to 22V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x1EF to 0x3FF	From 0x000 to 0x210	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x0C3 to 0x3FF	From 0x000 to 0x33C	From 0x0E6 to 0x3FF	From 0x000 to 0x319	From 0x131 to 0x3FF	From 0x000 to 0x2CE	From 0x131 to 0x3FF	From 0x000 to 0x2CE
3% R-Tolerance	From 0x073 to 0x3FF	From 0x000 to 0x38C	From 0x087 to 0x3FF	From 0x000 to 0x378	From 0x0AF to 0x3FF	From 0x000 to 0x350	From 0x0AF to 0x3FF	From 0x000 to 0x350

8/ INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0V. DNL specification limits of ±1 LSB maximum guaranteed monotonic operating conditions.

9/ Resistor terminal A, Resistor terminal B, and Resistor terminal W, have no limitations on polarity with respect to each other. Dual supply operation enables ground referenced bipolar signal adjustment.

10/ Different from operating current; supply current for fuse program lasts approximately 550 µs.

11/ Different from operating current; supply current for fuse read lasts approximately 550 µs.

12/ P_{DISS} is calculated from (I_{DD} x V_{DD}) + (I_{LOGIC} x V_{LOGIC}).

13/ All dynamic characteristics use V_{DD} = 15 V, V_{SS} = -15 V, and V_{LOGIC} = 5 V.

14/ V_{DD}/V_{SS} = ±15 V, VLOGIC = 2.7 V to 5.5 V, -55°C < T_A < +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

15/ All input signal are specified with $t_R = t_F$ = 1ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} +V_{IH})/2.

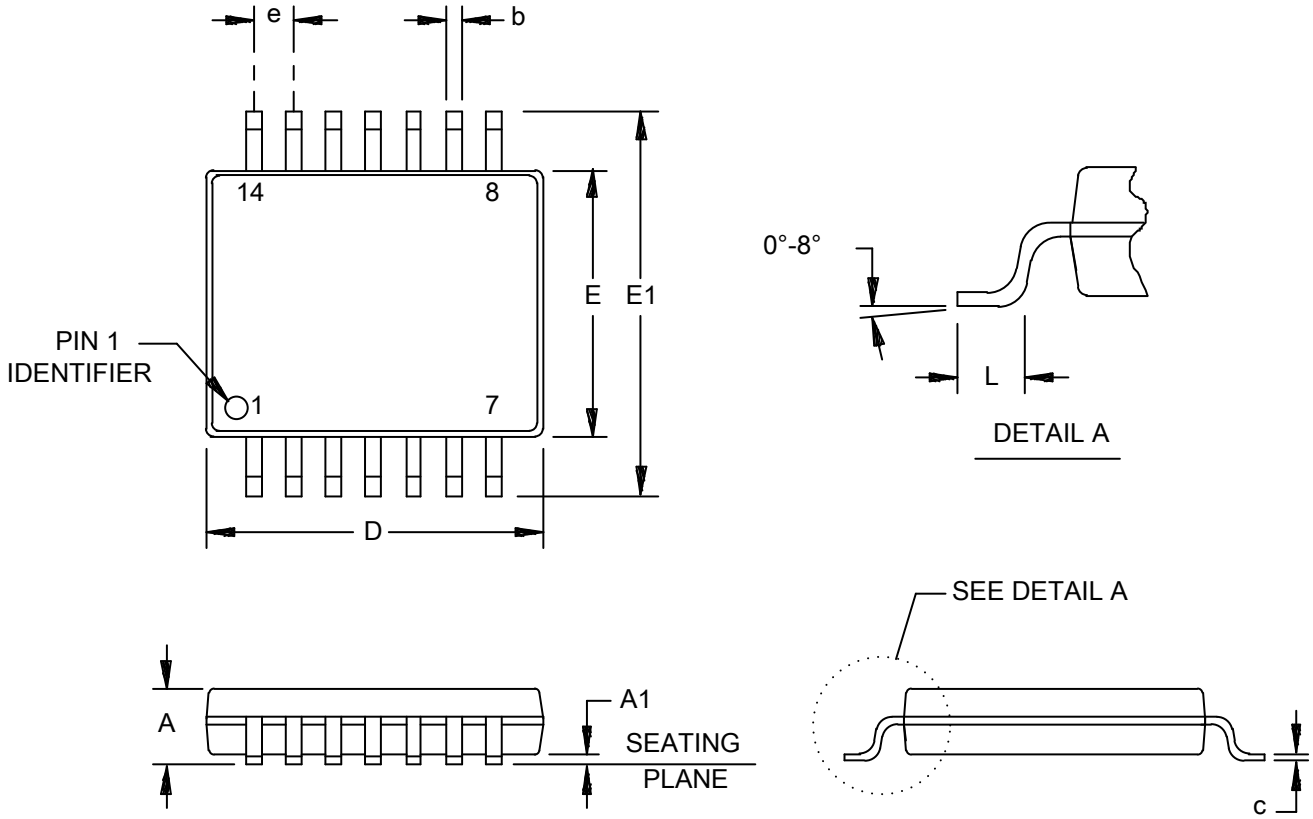
16/ Maximum SCLK frequency is 50 MHz.

17/ Refer to t12 and t13 for RDAC register and memory commands operations.

18/ $R_{PULL-UP}$ = 2.2 kΩ to V_{LOGIC}, with a capacitance load of 186 pF.

19/ Maximum time after V_{LOGIC} is equal to 2.5 V.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AB-1.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{\text{RESET}}$	8	V_{LOGIC}
2	V_{SS}	9	GND
3	A	10	DIN
4	W	11	SCLK
5	B	12	$\overline{\text{SYNC}}$
6	V_{DD}	13	SDO
7	EXT_CAP	14	RDY

FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
Number	Mnemonic	
1	$\overline{\text{RESET}}$	Hardware reset pin. Refreshes the RDAC register with the contents of the 20-TP memory register. Factory default loads midscale until the first 20-TP wiper memory location programmed. $\overline{\text{RESET}}$ is activated at the logic high transition. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if not used.
2	V_{SS}	Negative supply. Connect to 0 V for single supply applications. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
4	W	Wiper terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$.
5	B	Terminal B of RDAC. $V_{SS} \le V_B \le V_{DD}$.
6	V_{DD}	Positive power supply. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
7	EXT_CAP	External Capacitor. Connect a 1 µF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥ 7 V.
8	V_{LOGIC}	Logic power supply; 2.7 V to 5.5 V. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
9	GND	Ground pin, Logic ground reference.
10	DIN	Serial data input. The AD5292-EP has a 16 bit shift register. Data is clocked into register on the falling edge of the serial clock input.
11	SCLK	Serial clock input. data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	$\overline{\text{SYNC}}$	Falling edge synchronization signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of $\overline{\text{SYNC}}$ following the 16th clock cycle. If $\overline{\text{SYNC}}$ is taken high before 16th clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial data output. This open drain output requires an external pull up resistor. SDO can be used to clock data from the shift register in daisy chain mode or in readback mode.
14	RDY	Ready Pin. This active high open drain output identifies the completion of a write or read operation to or from the RDAC register or memory.

FIGURE 3. Terminal function.

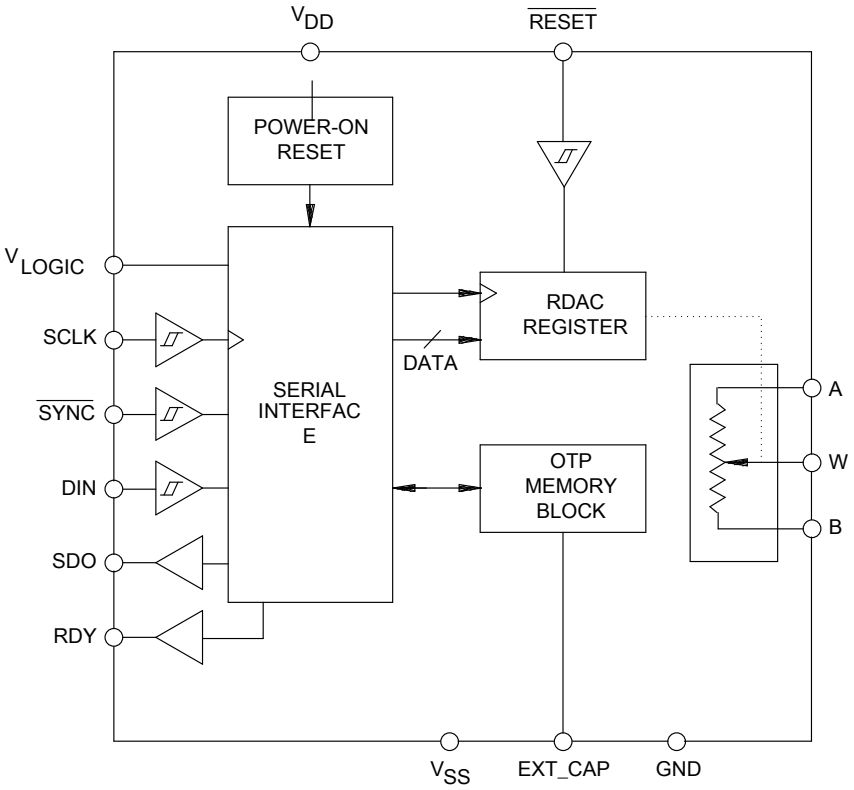


FIGURE 4. Functional block diagram.

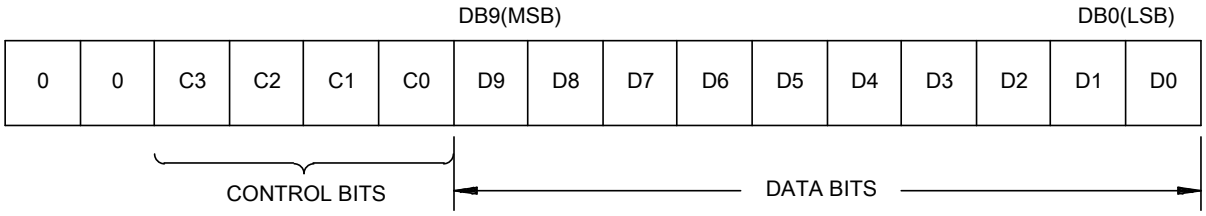


FIGURE 5. Shift register content.

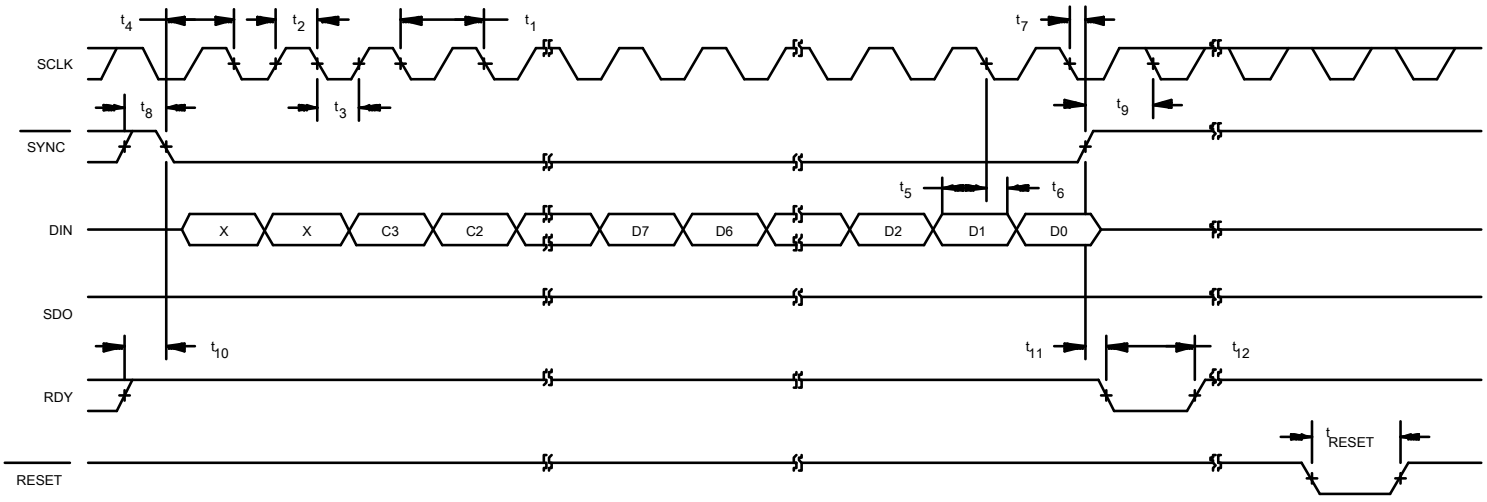


FIGURE 6. Write timing diagram, CPOL = 0, CPHA = 1.

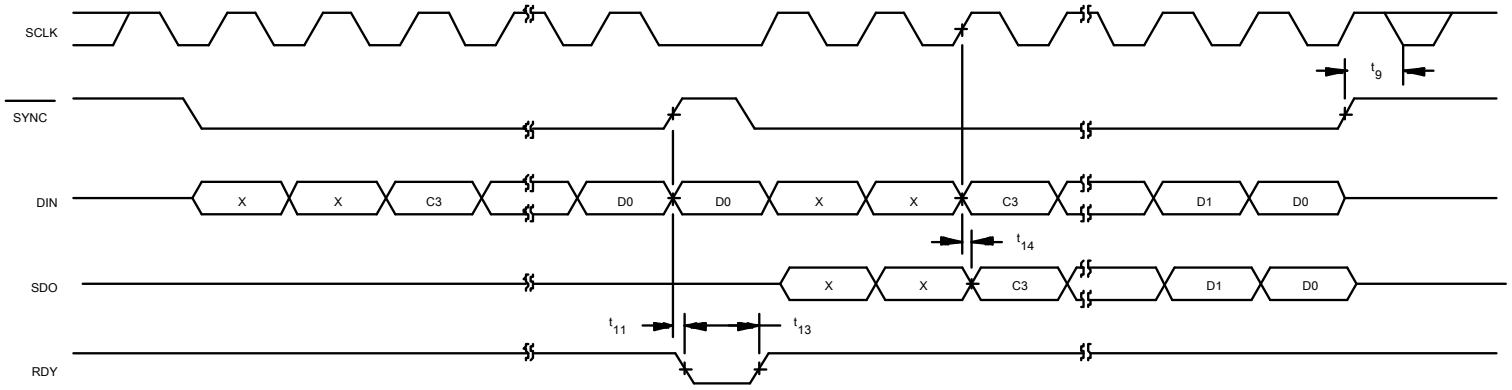


FIGURE 7. Read timing diagram, CPOL = 0, CPHA = 1.

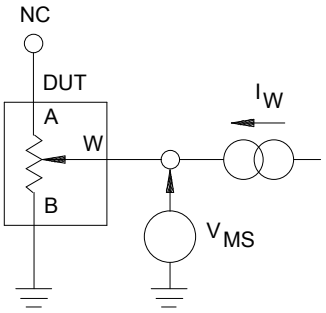


FIGURE 8. Resistor position nonlinearity error (Rheostat operation; R-INL, R-DNL).

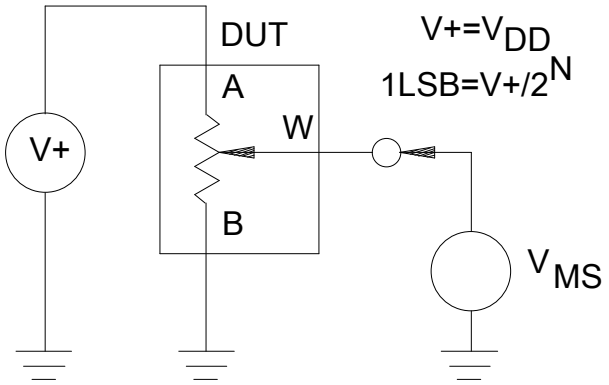
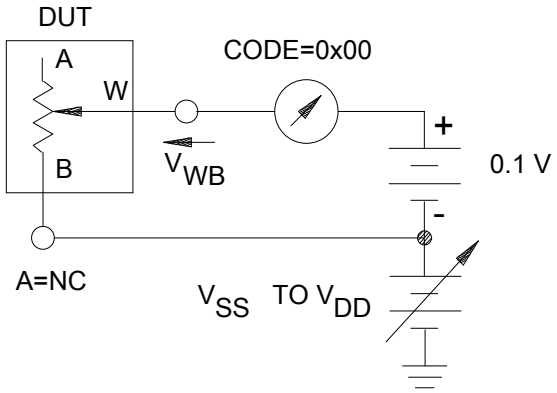


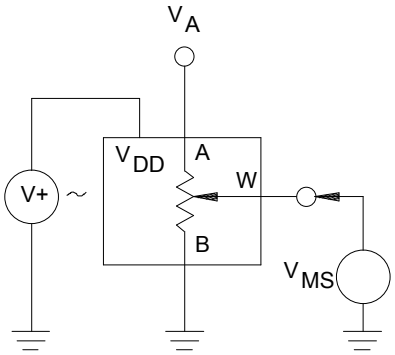
FIGURE 9. Potentiometer divider Nonlinearity error (INL, DNL).



$$RWB = \frac{0.1\ V}{I_{WB}}$$

$$RW = \frac{R_{WB}}{2}$$

FIGURE 10. Wiper resistance.



V+ = V_{DD} ±10%

PSRR (dB) = 20 log $\frac{\Delta V_{MS}}{\Delta V_{DD}}$

PSS(%%) = $\frac{\Delta V_{MS}{}^{\%}}{\Delta V_{DD}{}^{\%}}$

FIGURE 11. Power supply sensitive (PSS, PSRR).

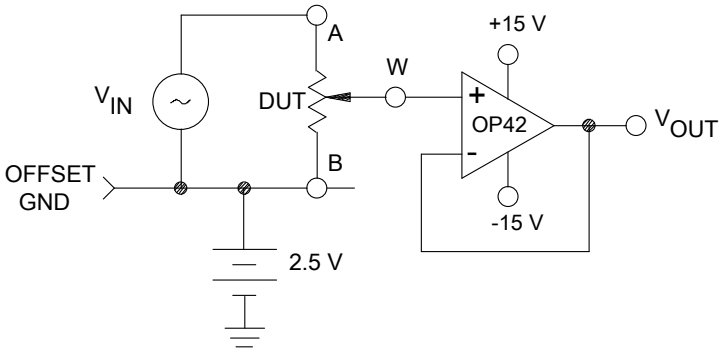


FIGURE 12. Gain vs Frequency.

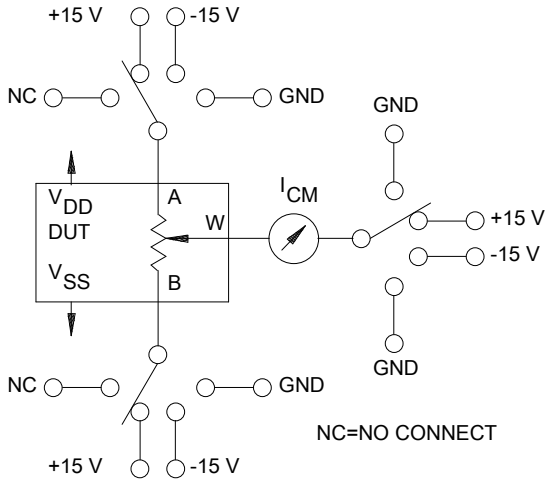


FIGURE 13. Common mode leakage current

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12616-01XB	24355	AD5292SRU-20-EP
V62/12616-01XE	24355	AD5292SRUZ-20-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106