REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct maximum operating junction temperature (T_J) to 150°C, in section 1.3.-phn.	12-12-14	Thomas M. Hess
B	Update ESD classification class level to paragraph 6.1. - MAA	15-04-10	Thomas M. Hess
C	Add case outline Y. - PHN	19-06-25	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	C	C	C	C	C	C	C	C	C	C	C	C	C								
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30								
REV STATUS OF PAGES		REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
		PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 12-11-06	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, EXTREME TEMPERATURE SINGLE PORT 10/100 MB/S ETHERNET PHYSICAL LAYER TRANSCEIVER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/12615**
	REV. C	**PAGE** 1 **OF** 30

AMSC N/A

5962-V110-19

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance extreme temperature single port 10/100 Mb/s Ethernet physical layer transceiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12615	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DP83848-EP	Extreme temperature single port 10/100 Mb/s Ethernet physical layer transceiver

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic Quad Flatpack
Y	48	MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, (V_{CC}) .... -0.5 V to 4.2 V
DC input voltage (V_{IN}) .... -0.5 V to V_{CC} + 0.5 V
DC output voltage (V_{OUT}) .... -0.5 V to V_{CC} + 0.5 V
Storage temperature (T_{STG}) .... -65°C to +150°C
Operating junction temperature (T_J) .... -55°C to +150°C
Lead temperature (T_L) (Soldering, 10 sec.) .... 260°C
ESD rating (R_{ZAP} = 1.5 kΩ, C_{ZAP} = 100 pF) .... 4.0 kV

1.4 Recommended operating conditions. 2/

Supply voltage, (V_{CC}) .... 3.0 V to 3.6 V
Operating free air temperature, (T_A) .... -55°C to +125°C 3/
Power dissipation (P_D) .... 267 mW

1.5 Thermal characteristics.

Thermal metric	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 4/	35.74	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 5/	21.8	
Junction to board thermal resistance, θ_{JB} 6/	19.5	
Junction to top characterization parameter, Ψ_{JT} 7/	1.2	
Junction to board characterization parameter, Ψ_{JB} 8/	19.4	
Junction to case (bottom) thermal resistance, θ_{JCbot} 9/	3.2	

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.
3/ Provided that thermal pad is soldered down.
4/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-k-board, as specified in JESD51-7, in an environment described in JESD51-2a.
5/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
6/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
7/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
8/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
9/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Junction-to-board thermal resistance Theta-JB or $R\theta_{JB}$

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88 - Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at http://www.ansi.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Device block diagram. The device block diagram shall be as shown in figure 3.

3.5.4 Power up timing. The power up timing shall be as shown in figure 4.

3.5.5 Reset timing. The reset timing shall be as shown in figure 5.

3.5.6 MII serial management timing. The MII serial management timing shall be as shown in figure 6.

3.5.7 100 Mb/s MII transmit timing. The 100 Mb/s MII transmit timing shall be as shown in figure 7.

3.5.8 100 Mb/s MII receive timing. The 100 Mb/s MII receive timing shall be as shown in figure 8.

3.5.9 100BASE-TX transmit packet latency timing. The 100BASE-TX transmit packet latency timing shall be as shown in figure 9.

3.5.10 100BASE-TX transmit packet deassertion timing. The 100BASE-TX transmit packet deassertion timing shall be as shown in figure 10.

3.5.11 100BASE-TX transmit packet timing ($t_{R/F}$ & Jitter). The 100BASE-TX transmit packet timing ($t_{R/F}$ & Jitter) shall be as shown in figure 11.

3.5.12 100BASE-TX receive packet latency timing. The 100BASE-TX receive packet latency timing shall be as shown in figure 12.

3.5.13 100BASE-TX receive packet deassertion timing. The 100BASE-TX receive packet deassertion timing shall be as shown in figure 13.

3.5.14 10 Mb/s MII transmit timing. The 10 Mb/s MII transmit timing shall be as shown in figure 14.

3.5.15 10 Mb/s MII receive timing. The 10 Mb/s MII receive timing shall be as shown in figure 15.

3.5.16 10 Mb/s serial mode transmit timing. The 10 Mb/s serial mode transmit timing shall be as shown in figure 16.

3.5.17 10 Mb/s serial mode receive timing. The 10 Mb/s serial mode receive timing shall be as shown in figure 17.

3.5.18 10BASE-T transmit timing (Start of packet). The 10BASE-T transmit timing (Start of packet) shall be as shown in figure 18.

3.5.19 10BASE-T transmit timing (End of packet). The 10BASE-T transmit timing (End of packet) shall be as shown in figure 19.

3.5.20 10BASE-T receive timing (Start of packet). The 10BASE-T receive timing (Start of packet) shall be as shown in figure 20.

3.5.21 10BASE-T receive timing (End of packet). The 10BASE-T receive timing (End of packet) shall be as shown in figure 21.

3.5.22 10 Mb/s heartbeat timing. The 10 Mb/s heartbeat timing shall be as shown in figure 22.

3.5.23 10 Mb/s Jabber timing. The 10 Mb/s Jabber timing shall be as shown in figure 23.

3.5.24 10BASE-T normal link pulse timing. The 10BASE-T normal link pulse timing shall be as shown in figure 24.

3.5.25 Auto-Negotiation Fast Link Pulse (FLP) timing. The auto-negotiation Fast Link Pulse (FLP) timing shall be as shown in figure 25.

3.5.26 100BASE-TX signal detect timing. The 100BASE-TX signal detect timing shall be as shown in figure 26.

3.5.27 100 Mb/s internal loopback timing. The 100 Mb/s internal loopback timing shall be as shown in figure 27.

3.5.28 10 Mb/s internal loopback timing. The 10 Mb/s internal loopback timing shall be as shown in figure 28.

3.5.29 RMII transmit timing. The RMII transmit timing shall be as shown in figure 29.

3.5.30 RMII receive timing. The RMII receive timing shall be as shown in figure 30.

3.5.31 Isolation timing. The Isolation timing shall be as shown in figure 31.

3.5.32 25 MHz_OUT timing. The 25 MHz_OUT timing shall be as shown in figure 32.

3.5.33 100 Mb/s X1 to TX_CLK timing. The 100 Mb/s X1 to TX_CLK timing shall be as shown in figure 33.

3.5.34 100BASE-TX transmit block diagram. The 100BASE-TX transmit block diagram shall be as shown in figure 34.

3.5.35 100BASE-TX receive block diagram. The 100BASE-TX receive block diagram shall be as shown in figure 35.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
DC SPECIFICATIONS					
Input high voltage	V_{IH}	Nominal V_{CC}	2.0		V
Input low voltage	V_{IL}			0.8	V
Input high current	I_{IH}	$V_{IN} = V_{CC}$		10	µA
Input low current	I_{IL}	V_{IN} = GND		10	µA
Output low voltage	V_{OL}	I_{OL} = 4 mA		0.4	V
Output high voltage	V_{OH}	I_{OH} = -4 mA	V_{CC} – 0.5		V
Tri state leakage	I_{OZ}	$V_{OUT} = V_{CC}$ or GND		±10	µA
100M transmit voltage	V_{TPTD_100}		0.89	1.15	V
100M transmit voltage symmetry	$V_{TPTDsym}$			±2	%
10M transmit voltage	V_{TPTD_10}		2.17	2.8	V
CMOS input capacitance	C_{IN1}		5 TYP		pF
CMOS output capacitance	C_{OUT1}		5 TYP		
100Base-TX signal detect turn-on threshold	SD_{THon}			1000	mv diff pk-pk
100Base-TX signal detect turn-off threshold	SD_{THoff}		200		mv diff pk-pk
10Base T receive threshold	V_{TH1}			585	mV
100Base – TX (Full duplex)	I_{dd100}		81 TYP		mA
10Base – TX (Full duplex)	I_{dd10}		92 TYP		
Power down mode	I_{dd}		14 TYP		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Conditions 2/	Limits Min	Limits Max	Unit
AC SPECIFICATIONS					
Power up timing See Figure 4.					
T2.1.1	Post power up stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32 bit serial management initialization X1 clock must be stable for a min. of 167 ms at power up	167		ms
T2.1.2	Hardware configuration latch in time from power up	Hardware configuration pins are described in the manufacturer data. X1 clock must be stable for a min. of 167 ms at power up	167		ms
T2.1.3	Hardware configuration pins transition to output drivers		50 TYP		ns
Reset timing 3/ See Figure 5.					
T2.2.1	Post reset stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32 bit serial management initialization	3 TYP		µs
T2.2.2	Hardware configuration latch in time from deassertion of RESET (either soft or hard)	Hardware configuration pins are described in the manufacturer data	3 TYP		µs
T2.2.3	Hardware configuration pins transition to output drivers		50 TYP		ns
T2.2.4	RESET pulse width	X1 clock must be stable for a min. of 1 µs during RESET pulse low time	1		µs
MII serial management timing See Figure 6.					
T2.3.1	MDC to MDIO (output) delay time		0	30	ns
T2.3.2	MDIO (input) to MDC setup time		10		ns
T2.3.3	MDIO (input) to MDC hold time		10		ns
T2.3.4	MDC frequency			25	MHz
100 Mb/s MII transmit timing See Figure 7.					
T2.4.1	TX_CLK high/low time	100 Mb/s Normal mode	16	24	ns
T2.4.2	TXD[3:0], TX_EN data setup to TX_CLK	100 Mb/s Normal mode	9.70		ns
T2.4.3	TXD[3:0], TX_EN data hold from TX_CLK	100 Mb/s Normal mode	0		ns
100 Mb/s MII receive timing 4/ See Figure 8.					
T2.5.1	RX_CLK high/low time	100 Mb/s Normal mode	16	24	ns
T2.5.2	RX_CLK to RXD[3:0], RX_DV, RX_ER delay	100 Mb/s Normal mode	10	30	ns
100 Base-TX transmit packet latency timing 5/ See Figure 9.					
T2.6.1	TX_CLK to PMD output pair latency	100 Mb/s Normal mode	6 TYP		bits
100 Base-TX transmit packet deassertion timing 6/ See Figure 10.					
T2.7.1	TX_CLK to PMD output pair deassertion	100 Mb/s Normal mode	6 TYP		bits

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Conditions 2/	Limits Min	Limits Max	Unit
AC SPECIFICATIONS – Cotinued.					
100Base TX transmit timing ($t_{R/F}$ & Jitter) 7/ 8/ See Figure 11.					
T2.8.1	100 Mb/s PMD output pair t_R and t_F		2.6	5.5	ns
	100 Mb/s t_R and t_F mismatch			500	ps
T2.8.2 25/	100 Mb/s PMD output pair transmit Jitter			1.4	ns
100 Base-TX receive packet latency timing 9/ 10/ 11/ See Figure 12.					
T2.9.1	Carrier sense ON delay	100 Mb/s Normal mode	20 TYP		bits
T2.9.2	Receive data latency	100 Mb/s Normal mode	24 TYP		bits
100 Base-TX receive packet deassertion timing 10/ 12/ See Figure 13.					
T2.10.1	Carrier sense OFF delay	100 Mb/s Normal mode	24 TYP		bits
10 Mb/s MII transmit timing 13/ See Figure 14.					
T2.11.1	TX_CLK high/low time	10 Mb/s MII mode	190	210	ns
T2.11.2	TXD[3:0], TX_EN data setup to TX_CLK fall	10 Mb/s MII mode	24.7		
T2.11.3	TXD[3:0], TX_EN data hold from TX_CLK rise	10 Mb/s MII mode	0		
10 Mb/s MII receive timing 14/ See Figure 15.					
T2.12.1	RX_CLK high/low time		160	240	ns
T2.12.2	RX_CLK to RXD[3:0], RX_DV delay	10 Mb/s MII mode	100		
T2.12.3	RX_CLK rising edge delay from RXD[3:0], RS_DV valid	10 Mb/s MII mode	100		
10 Mb/s serial mode transmit timing See Figure 16.					
T2.13.1	TX_CLK high time	10 Mb/s serial mode	20	30	ns
T2.13.2	TX_CLK low time	10 Mb/s serial mode	70	80	
T2.13.3	TXD_0, TX_EN data setup to TX_CLK rise	10 Mb/s serial mode	24.7		
T2.13.4	TXD_0, TX_EN data hold from TX_CLK rise	10 Mb/s serial mode	0		
10 Mb/s serial mode receive timing 14/ See Figure 17.					
T2.14.1	RX_CLK high/low time		35	65	ns
T2.14.2	RX_CLK fall to RXD_0, RX_DV delay	10 Mb/s serial mode	-10	10	
10Base T-transmit timing (Start of Packet) See Figure 18.					
T2.15.1	Transmit output delay from the falling edge of TX_CLK	10 Mb/s MII mode	3.5 TYP		bits
T2.15.2	Transmit output delay from the rising edge of TX_CLK	10 Mb/s serial mode	3.5 TYP		
10Base T-transmit timing (End of Packet) See Figure 19.					
T2.16.1	End of packet high time (with ‘0’ ending bit)		250		ns
T2.16.2	End of packet high time (with ‘1’ ending bit)		250		

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Conditions 2/	Limits Min	Limits Max	Unit
AC SPECIFICATIONS – Cotinued.					
10Base T-receive timing (Start of Packet) 15/ 16/ See Figure 20.					
T2.17.1	Carrier sense turn ON delay (PMD input pair to CRS)			1000	ns
T2.17.2	RX_DV latency		10 TYP		bits
T2.17.3	Receive data latency	Measure shown from SFD	8 TYP		
10Base T-receive timing (End of Packet) See Figure 21.					
T2.18.1	Carrier sense turn OFF delay			1.0	μs
10 Mb/s Heartbeat timing See Figure 22.					
T2.19.1	CD heartbeat delay	All 10 Mb/s modes	1200 TYP		ns
T2.19.2	CD heartbeat duration	All 10 Mb/s modes	1000 TYP		
10 Mb/s Jabber timing See Figure 23.					
T2.20.1	Jabber activation time		85 TYP		ms
T2.20.2	Jabber deactivation time		500 TYP		
10Base T normal link pulse timing 17/ See Figure 24.					
T2.21.1	Pulse width		100 TYP		ns
T2.21.2	Pulse period		16 TYP		ms
Auto negotiation Fast Link Pulse (FLP) timing 17/ See Figure 25.					
T2.22.1	Clock, data pulse width		100 TYP		ns
T2.22.2	Clock pulse to clock pulse period		125 TYP		μs
T2.22.3	Clock pulse to data pulse period	Data =1	62 TYP		μs
T2.22.4	Burst width		2 TYP		ms
T2.22.5	FLP burst to FLP burst period		16 TYP		ms
100Base TX signal detect timing 18/ See Figure 26.					
T2.23.1	SD internal Turn-ON time			1	ms
T2.23.2	SD internal Turn-OFF time			350	μs
100 Mb/s internal loopback timing 19/ 20/ See Figure 27.					
T2.24.1	TX_EN to RX_DV loopback	100 Mb/s internal loopback mode		240	ns
10 Mb/s internal loopback timing 20/ See Figure 28.					
T2.25.1	TX_EN to RX_DV loopback	10 Mb/s internal loopback mode		2	μs
RMII transmit timing See Figure 29.					
T2.26.1	X1 clock period	50 MHz reference clock	20 TYP		ns
T2.26.2	TXD[1:0], TX_EN, data setup to X1 rising		3.7		
T2.26.3	TXD[1:0], TX_EN, data hold from to X1 rising		1.7		
T2.26.4	X1 clock to PMD output pair latency	From X1 rising edge to first bit of symbol	17 TYP		bits

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

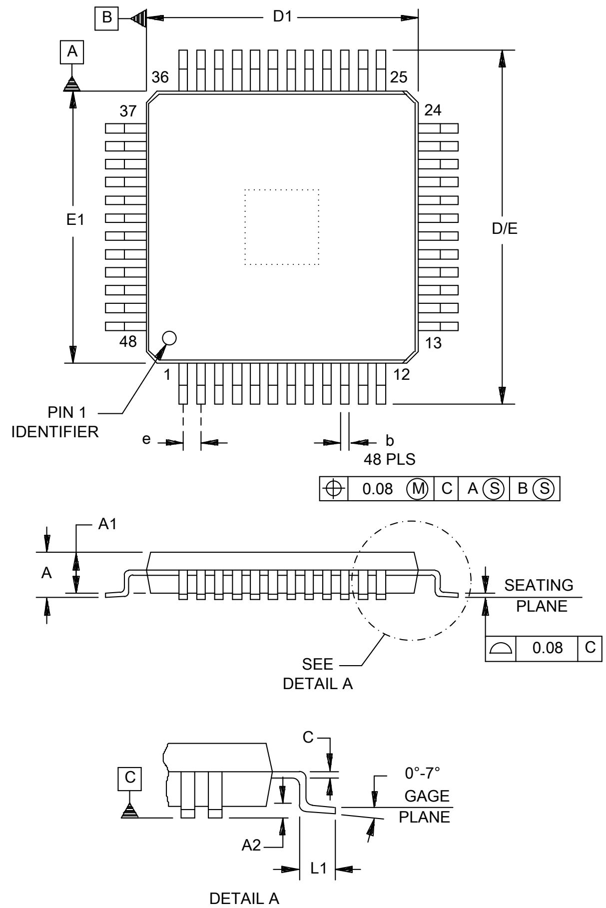
	Test	Conditions 2/	Limits Min	Limits Max	Unit
AC SPECIFICATIONS – Cotinued.					
RMII receive timing 21/ 22/ 23/ See Figure 30.					
T2.27.1	X1 clock period	50 MHz reference clock	20 TYP		ns
T2.27.2	RXD[1:0], CRS_DV, RX_DV and RX_ER output delay from X1 rising		2	14	ns
T2.27.3	CRS ON delay	From JK symbol on PMD receive pair to initial assertion of CRS_DV	18.5 TYP		bits
T2.27.4	CRS OFF delay	From TR symbol on PMD receive pair to initial deassertion of CRS_DV	27 TYP		
T2.27.5	RXD[1:0] and RX_ER latency	From symbol on Receive pair. Elasticity buffer set to default value (01)	38 TYP		
Isolation timing See Figure 31.					
T2.28.1	From software clear of bit 10 in the BMCR register to the transition from isolate to normal mode			100	µs
T2.28.2	From deassertion of S/W or H/W reset to transition from isolate to normal mode			500	
25 MHz_OUT timing 24/ See Figure 32.					
T2.29.1	25 MHz_OUT high/low time	MII mode	20 TYP		ns
		RMII mode	10 TYP		
T2.29.2	25 MHz_OUT propagation delay			8	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over operating free-air temperature range (unless otherwise noted).
3/ It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch in the proper value prior to the pin transitioning to an output driver.
4/ RX_CLK may be held low or high for a longer period of time during transition between reference and recovered clocks. Minimum high and low will not be violated.
5/ For normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the "J" code group as output from the PMD output pair. 1 bit time = 10 ns in 100 Mb/s mode.
6/ Deassertion is determined by measuring the time from the first rising edge of TX_CLK occurring after deassertion of TX_EN to the first bit of the "T" code group as output from the PMD output pair. 1bit time = 10 ns in 100 Mb/s mode.
7/ Normal mismatch is the difference between the maximum and minimum of all rise and fall times.
8/ Rise and fall times taken at 10% and 90% of the +1 or -1 amplitude.
9/ Carrier sense ON delay is determined by measuring the time from the first bit of the "J" code group to the assertion of Carrier sense.
10/ 1 bit time = 10 ns in 100 Mb/s mode.
11/ PMD input pair voltage amplitude is greater than the Signal detect Turn-ON threshold value.
12/ Carrier sense OFF delay is determined by measuring the time from the first bit of the "T" code group to the deassertion of Carrier sense.

TABLE I. Electrical performance characteristics - Continued. 1/

13/ An attached Mac should drive the transmit signals using the positive edge of TX_CLK. As shown in Fig. XX, the MII signals are sampled on the falling edge of TX_CLK.
14/ RX_CLK may be held low for a longer period of timing during transition between reference and recovered clocks. Minimum high and low times will not be violated.
15/ 1 bit time = 100 ns in 10 Mb/s mode.
16/ 10Base-T RX_DV latency is measured from first bit of preamble on the wire to the assertion of RX_DV.
17/ These specifications represent transmit timings.
18/ The signal amplitude on PMD input pair must be TP-PMD compliant.
19/ Due to the nature of the descrambler function, all 100Base-TX loopback modes will cause an initial “dead time” of up to 550 μs during which time no data will be present at the receive MII outputs. The 100Base-TX timing specified is based on device delays after the initial 550 μs “dead time”.
20/ Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.
21/ Per the RMII specification, output delays assume a 25 pF load.
22/ CRS_DV is asserted asynchronously in order to minimize latency of control signals through the why. CRS_DV may toggle synchronously at the end of the packet to indicate CRS deassertion.
23/ RX_DV is synchronous to X1. While not part of the RMII specification, this signal is provided to simplify recovery of receive data.
24/ 25 MHz_Out characteristics are dependent upon the X1 input characteristics.
25/ Specified from -40°C to +125°C

Case X

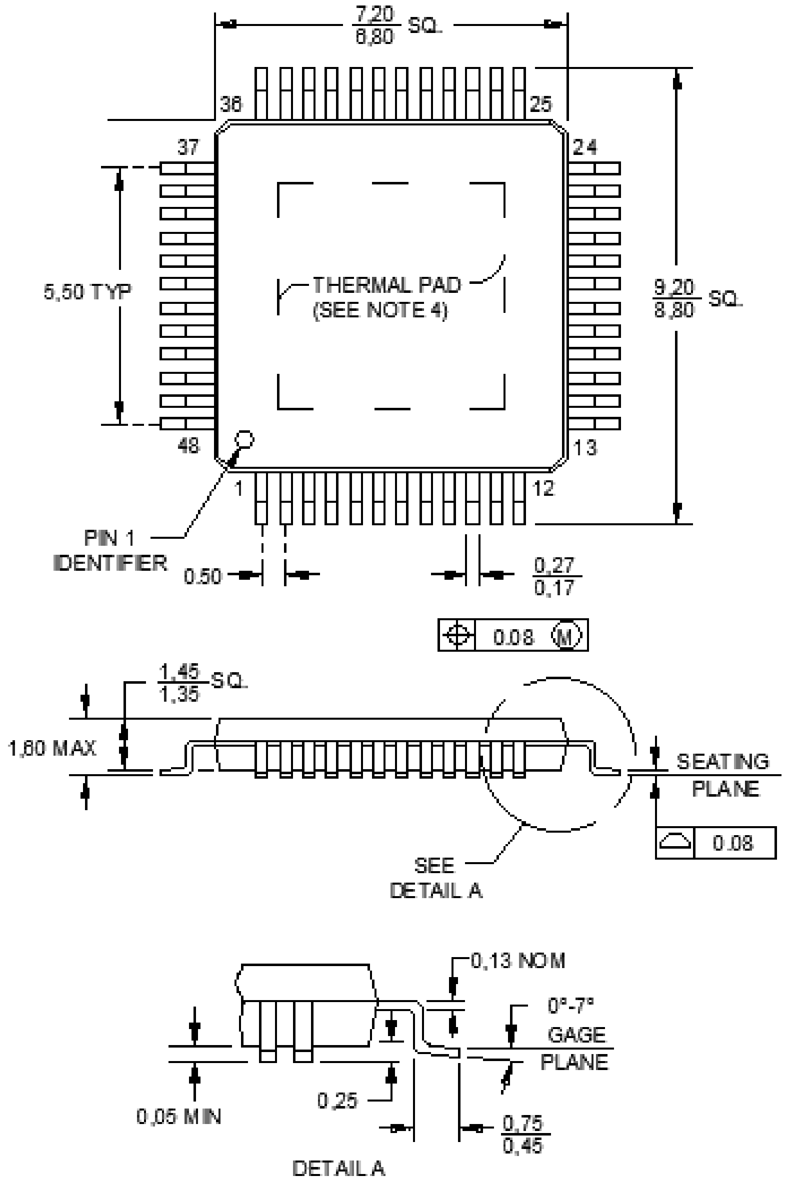


Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	8.80	9.20
A1	0.95	1.05	D1/E1	6.80	7.20
b	0.17	0.27	e	0.50 BSC	
c	0.13 NOM		L1	0.45	0.75

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion.
4. This package is designed to be soldered to a thermal pad on the board. Refer to the manufacturer data for more information.
5. Package Dimensions (W x L x H) = 7.0 mm x 7.0 mm x 1.00 mm.
6. Falls within JEDEC MS-026

FIGURE 1. Case outline.

Case Y



NOTES:

1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. This drawing is subject to change without notice.
3. Also may be thermally enhanced plastic package with leads connected to the die pads..
4. This package is designed to be soldered to a thermal pad on the board. Refer to the manufacturer data for more information regarding recommended board layout.
5. Package Dimensions (W x L x H) = 7.0 mm x 7.0 mm x 1.40 mm.
6. Falls within JEDEC MS-026

Case outline X and Y.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	TX_CLK	25	25MHz_OUT
2	TX_EN	26	LED_ACT/COL/AN_EN
3	TXD_0	27	LED_SPEED/AN1
4	TXD_1	28	LED_LINK/AN0
5	TXD_2	29	RESET_N
6	TXD_3/SNI_MODE	30	MDIO
7	PWR_DOWN/INT	31	MDC
8	TCK	32	IOVDD33
9	TDO	33	X2
10	TMS	34	X1
11	TRST#	35	IOGND
12	TDI	36	DGND
13	RD-	37	PFBIN2
14	RD+	38	RX_CLK
15	AGND	39	RX_DV/MII_MODE
16	TD-	40	CRS/CRS_DV/LED_CFG
17	TD+	41	RX_ER/MDIX_EN
18	PFBIN1	42	COL/PHYAD0
19	AGND	43	RXD_0/PHYAD1
20	RESERVED	44	RXD_1/PHYAD2
21	RESERVED	45	RXD_2/PHYAD3
22	AVD33	46	RXD_3/PHYAD4
23	PFBOUT	47	IOGND
24	RBIAS	48	IOVDD33
49		GNDPAD	

FIGURE 2. Terminal connections.

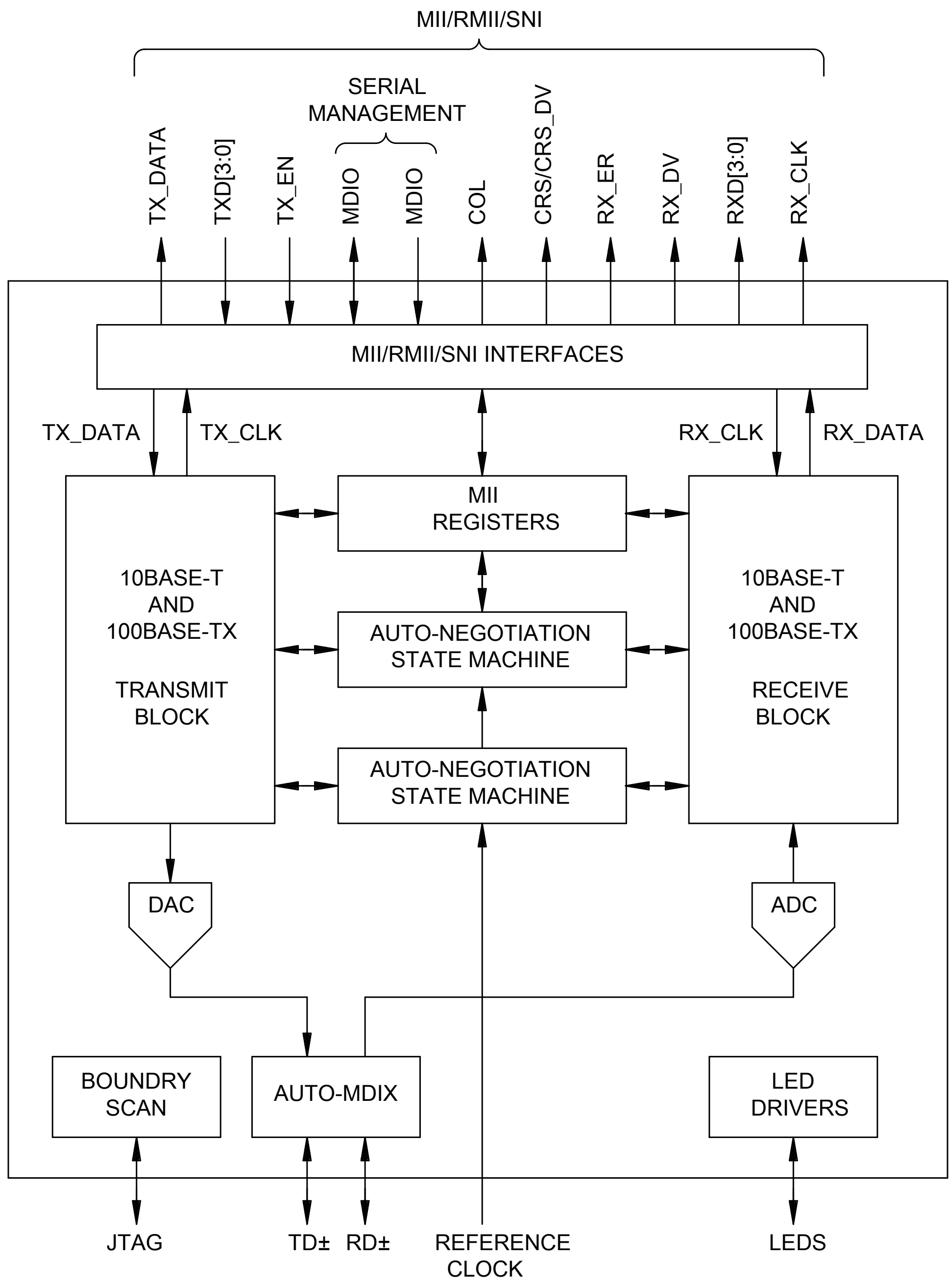


FIGURE 3. Device block diagram.

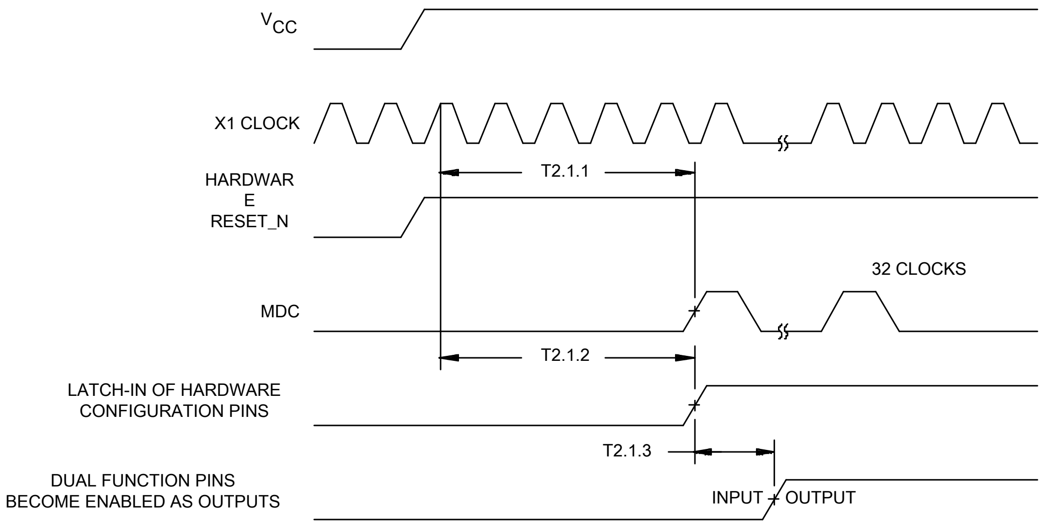


FIGURE 4. Power up timing.

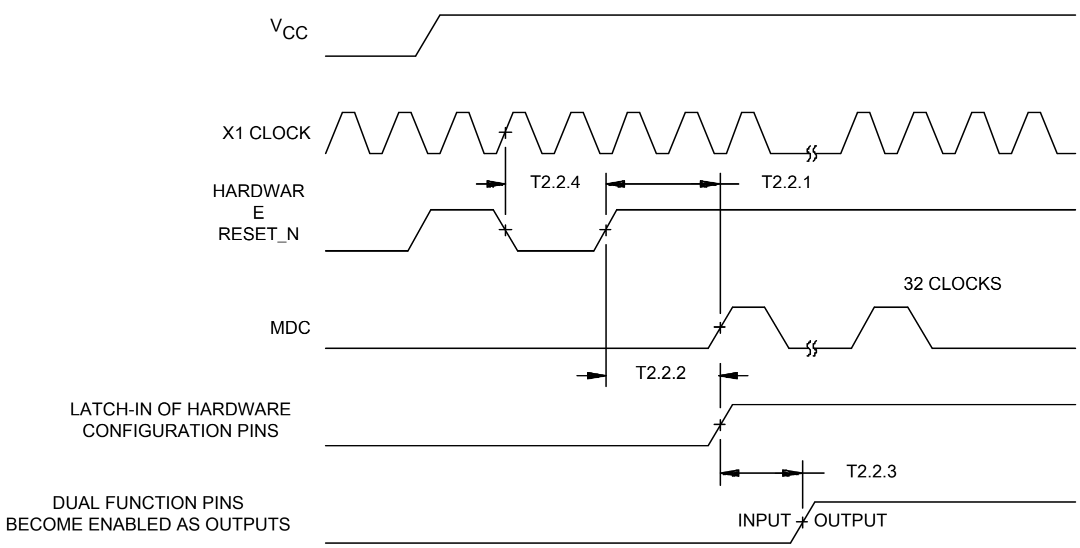


FIGURE 5. Reset timing.

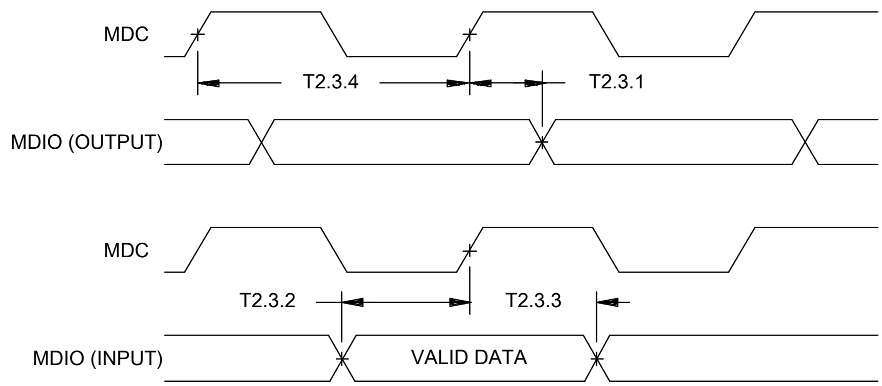


FIGURE 6. MII serial management timing.

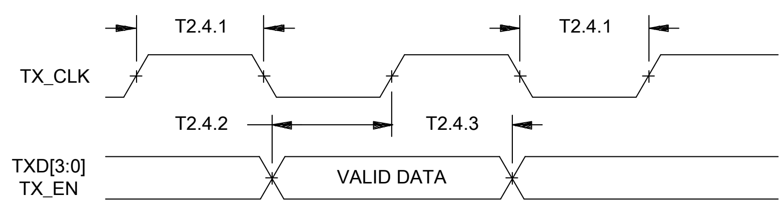


FIGURE 7. 100 Mb/s MII transmit timing.

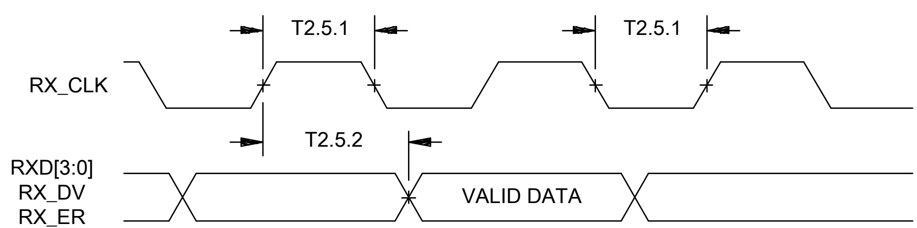


FIGURE 8. 100 Mb/s MII receive timing.

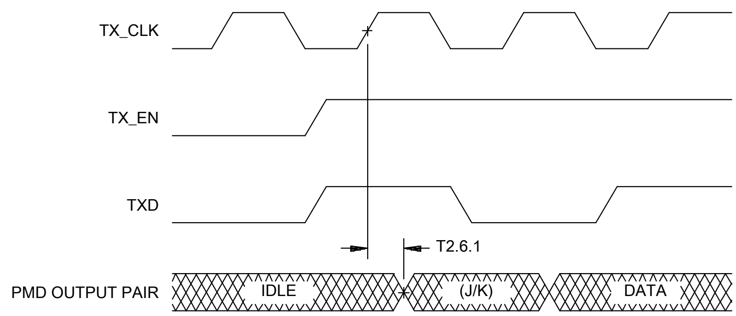


FIGURE 9. 100BASE-TX transmit packet latency timing.

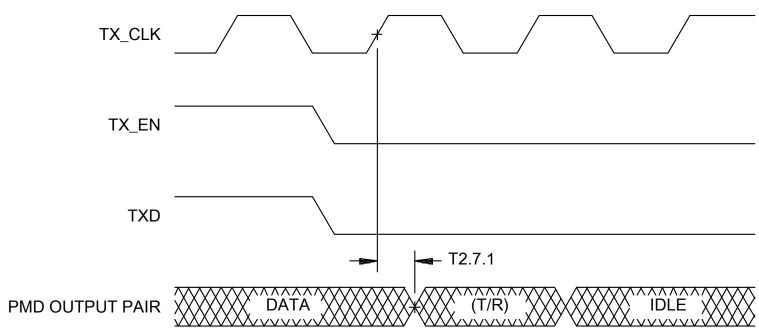


FIGURE 10. 100BASE-TX transmit packet deassertion timing.

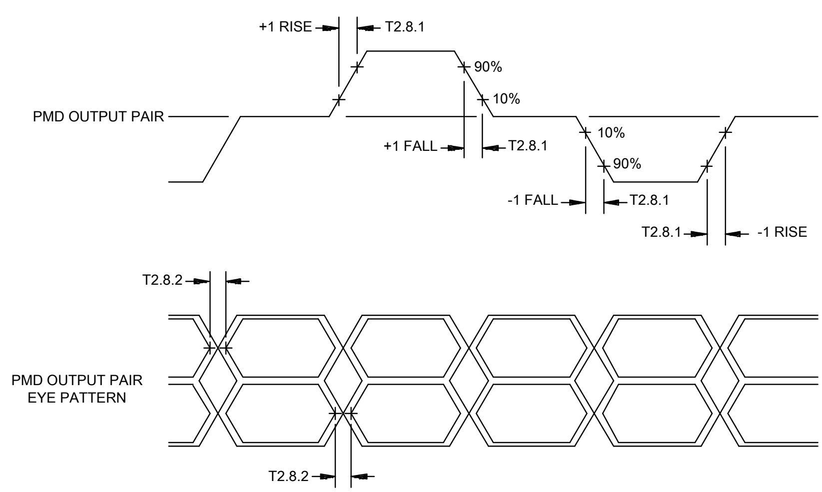


FIGURE 11. 100BASE-TX transmit timing ($t_{R/F}$ & Jitter).

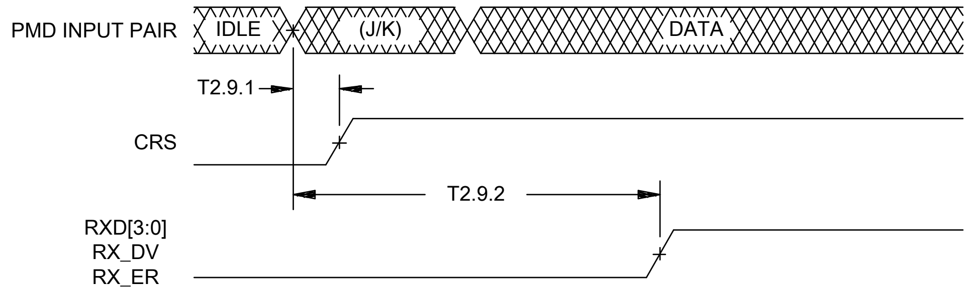


FIGURE 12. 100BASE-TX receive packet latency timing.

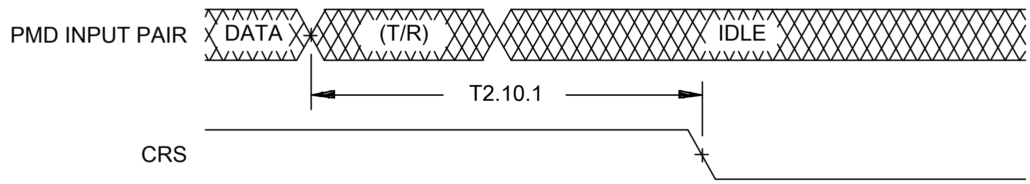


FIGURE 13. 100BASE-TX receive packet deassertion timing.

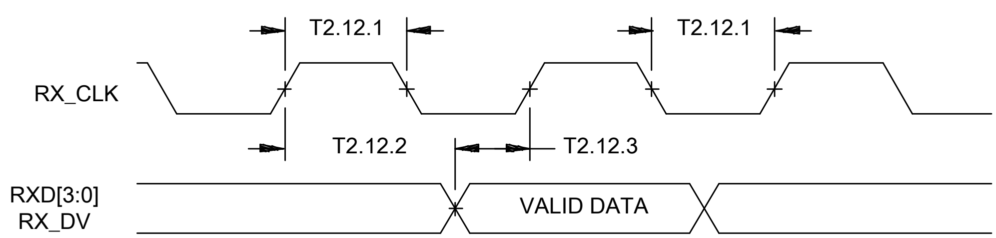


FIGURE 14. 10 Mb/s MII transmit timing.

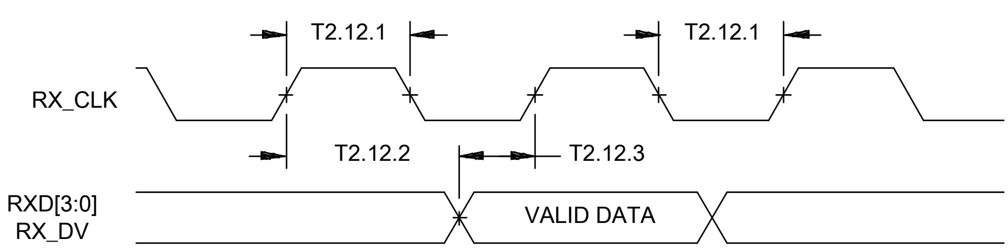


FIGURE 15. 10 Mb/s MII receive timing.

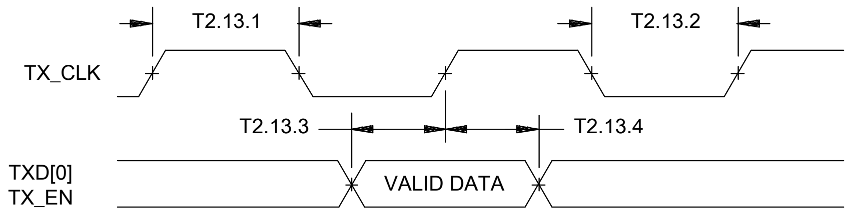


FIGURE 16. 10 Mb/s Serial mode transmit timing.

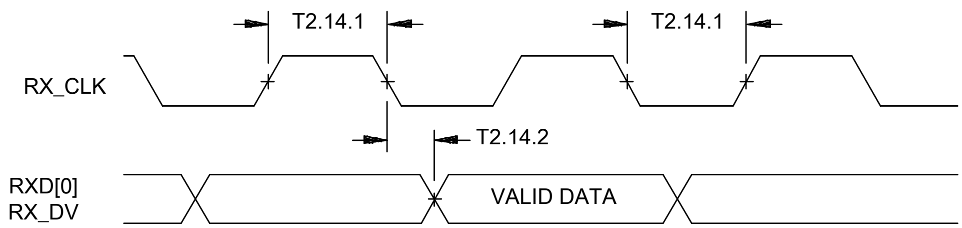


FIGURE 17. 10 Mb/s Serial mode receive timing.

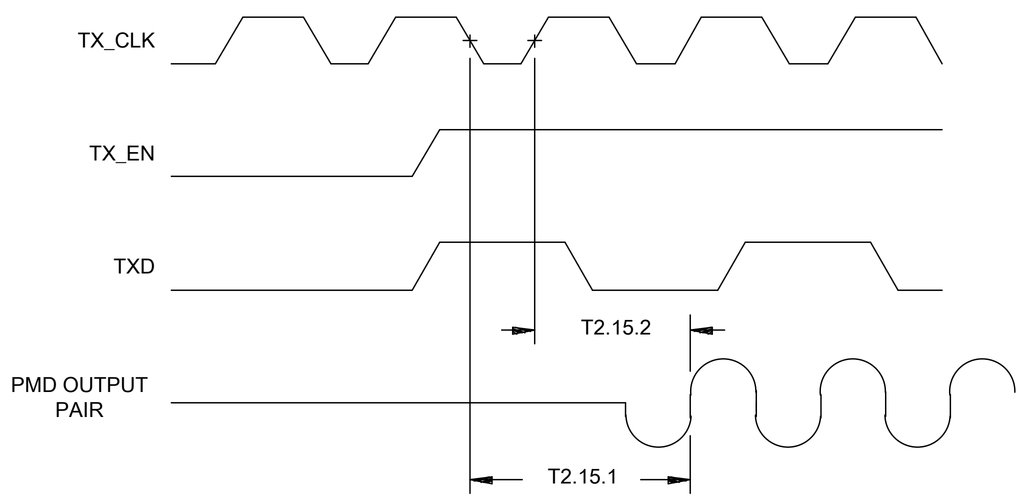


FIGURE 18. 10BASE-T transmit timing (Start of Packet).

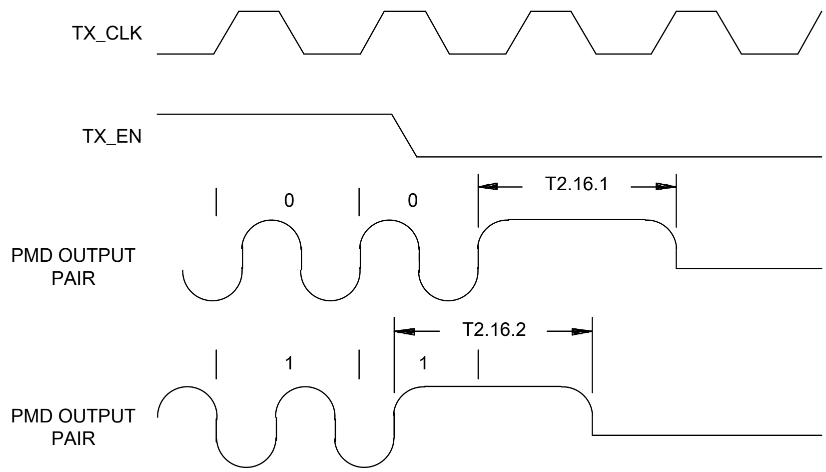


FIGURE 19. 10BASE-T transmit timing (End of Packet).

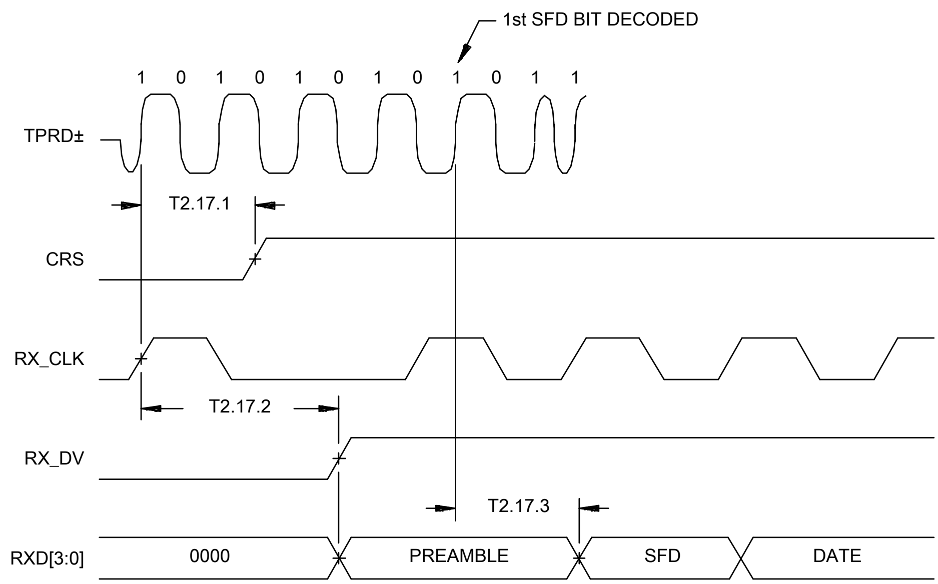


FIGURE 20. 10BASE-T receive timing (Start of Packet).

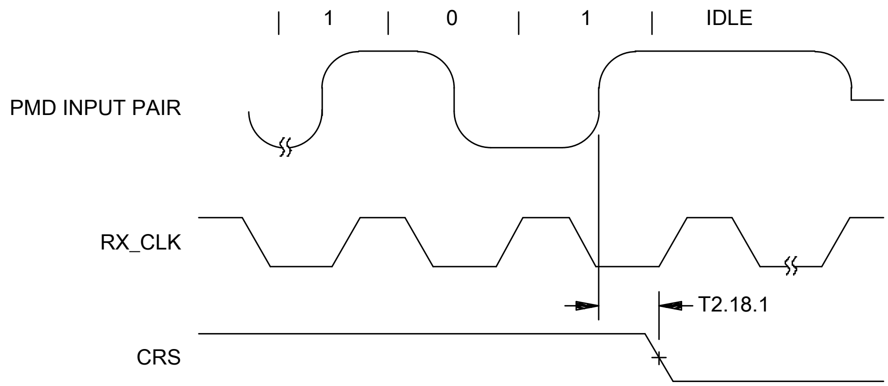


FIGURE 21. 10BASE-T receive timing (End of Packet).

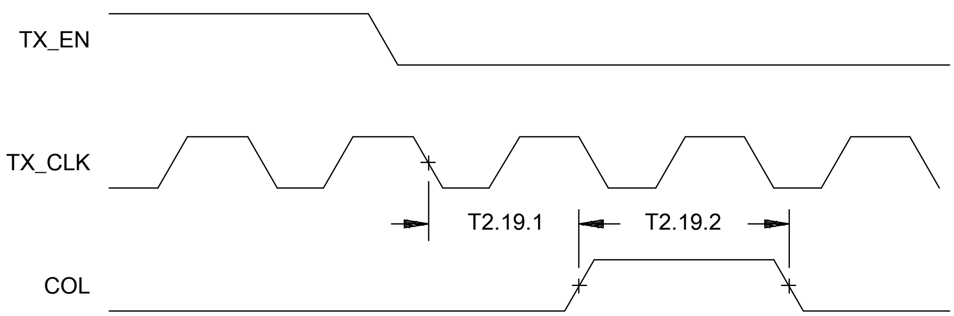


FIGURE 22. 10 Mb/s heartbeat timing.

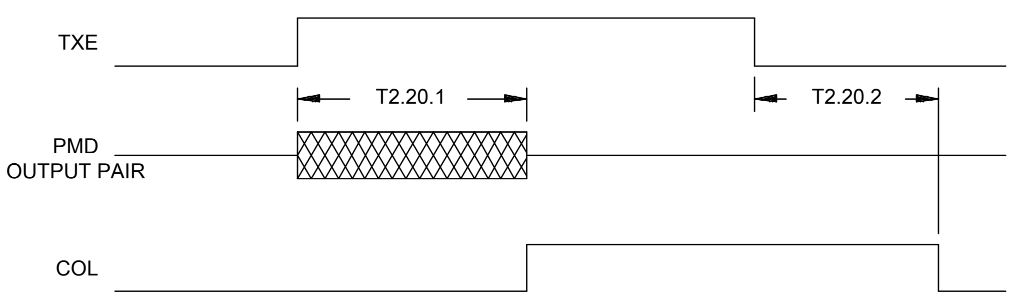


FIGURE 23. 10 Mb/s Jabber timing.

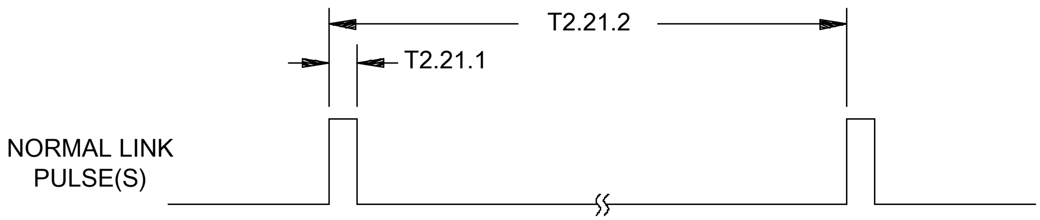


FIGURE 24. 10BASE-T normal link pulse timing.

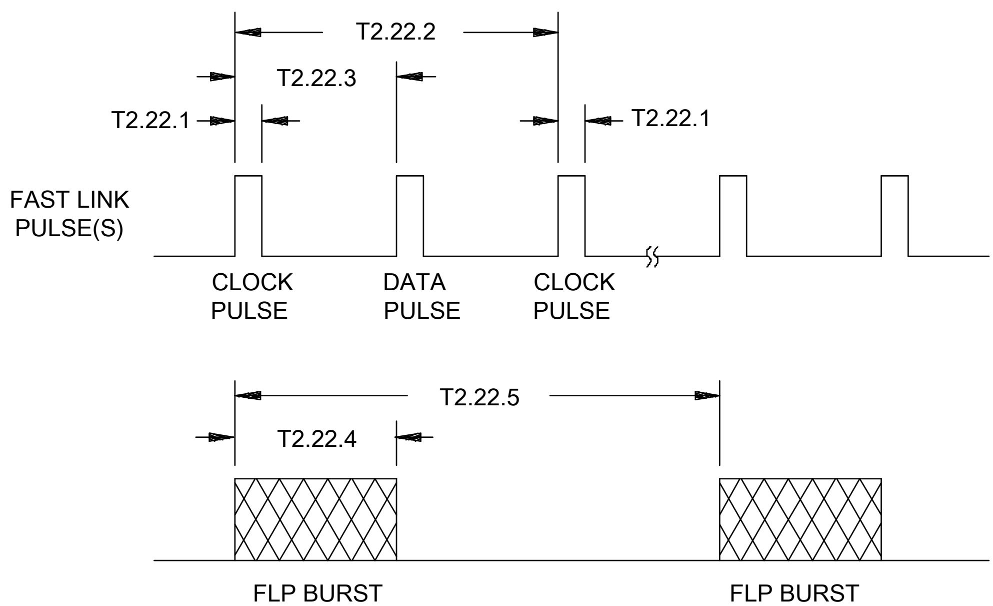


FIGURE 25. Auto-Negotiation Fast Link Pulse (FLP) timing.

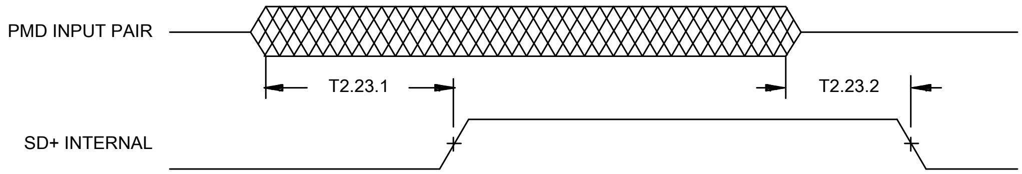


FIGURE 26. 100BASE-TX signal detect timing.

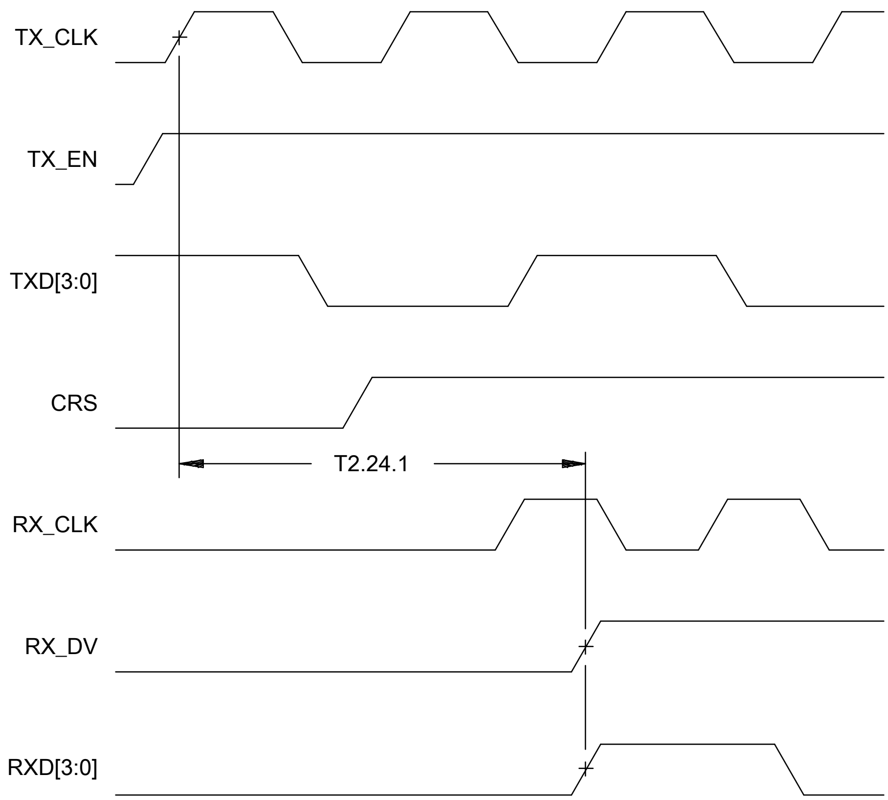


FIGURE 27. 100 Mb/s Internal Loopback timing.

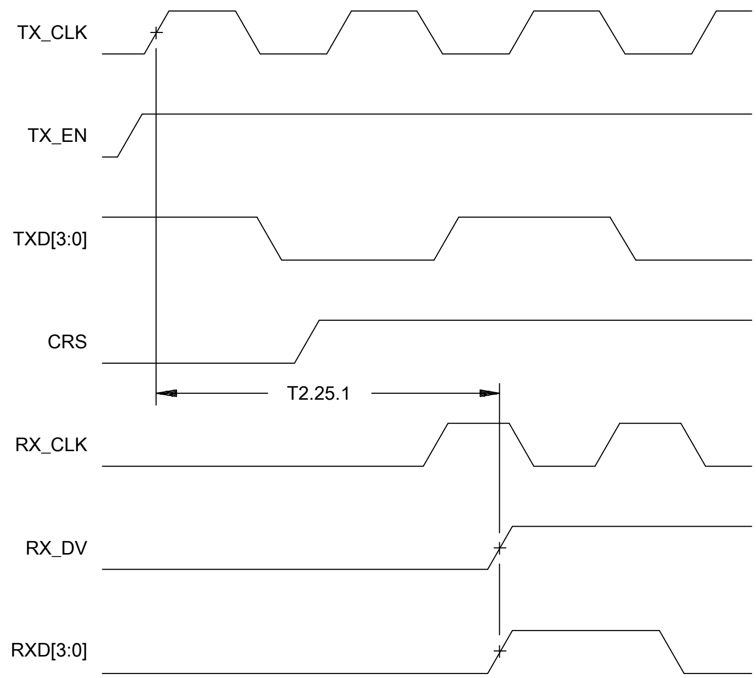


FIGURE 28. 10 Mb/s Internal Loopback timing.

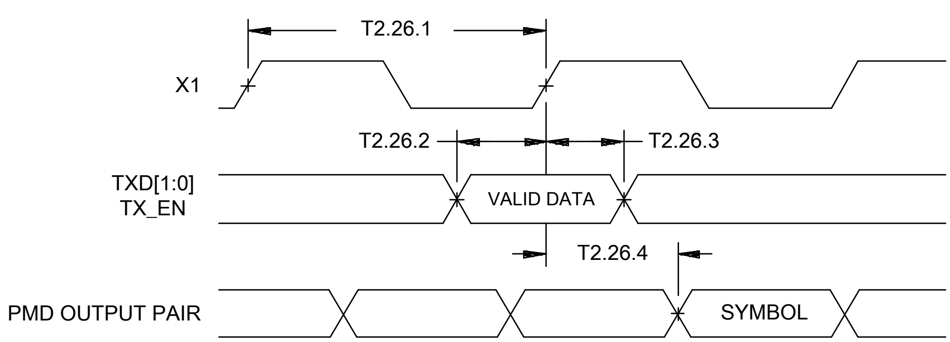


FIGURE 29. RMII transmit timing.

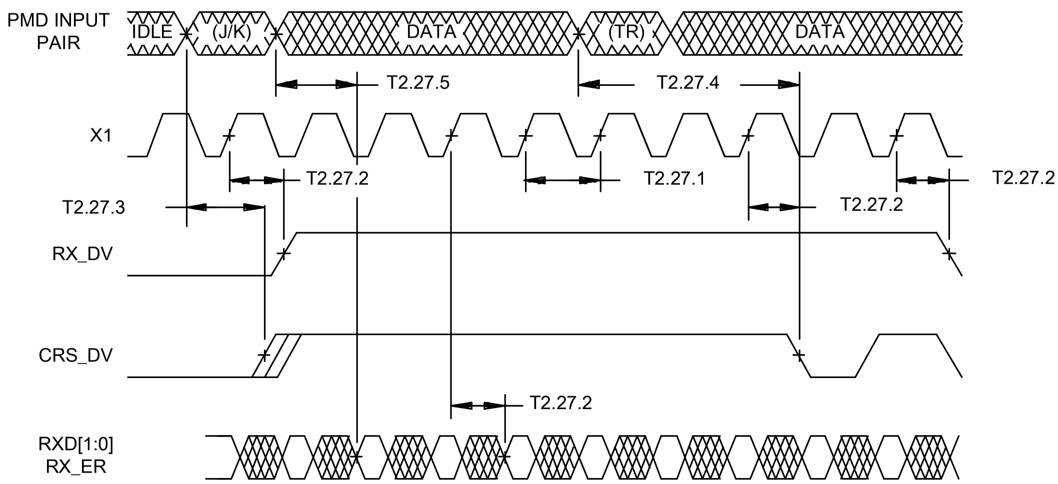


FIGURE 30. RMII transmit timing.

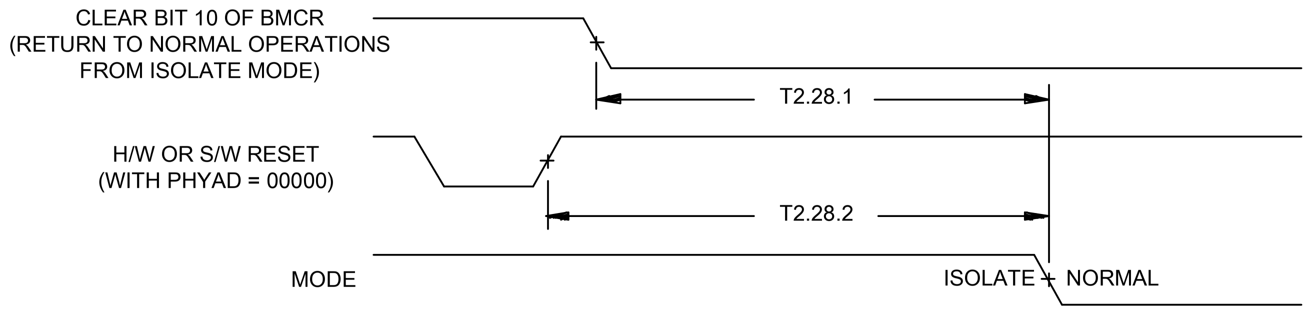


FIGURE 31. Isolation timing.

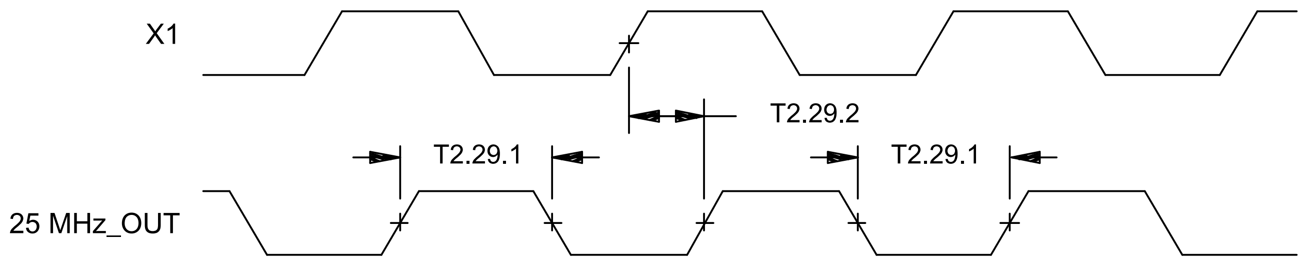


FIGURE 32. 25 MHz_Out timing.

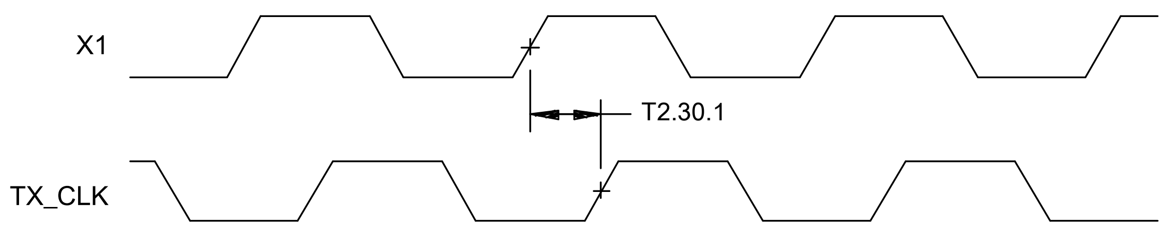


FIGURE 33. 100 Mb/s X1 to TX_CLK timing.

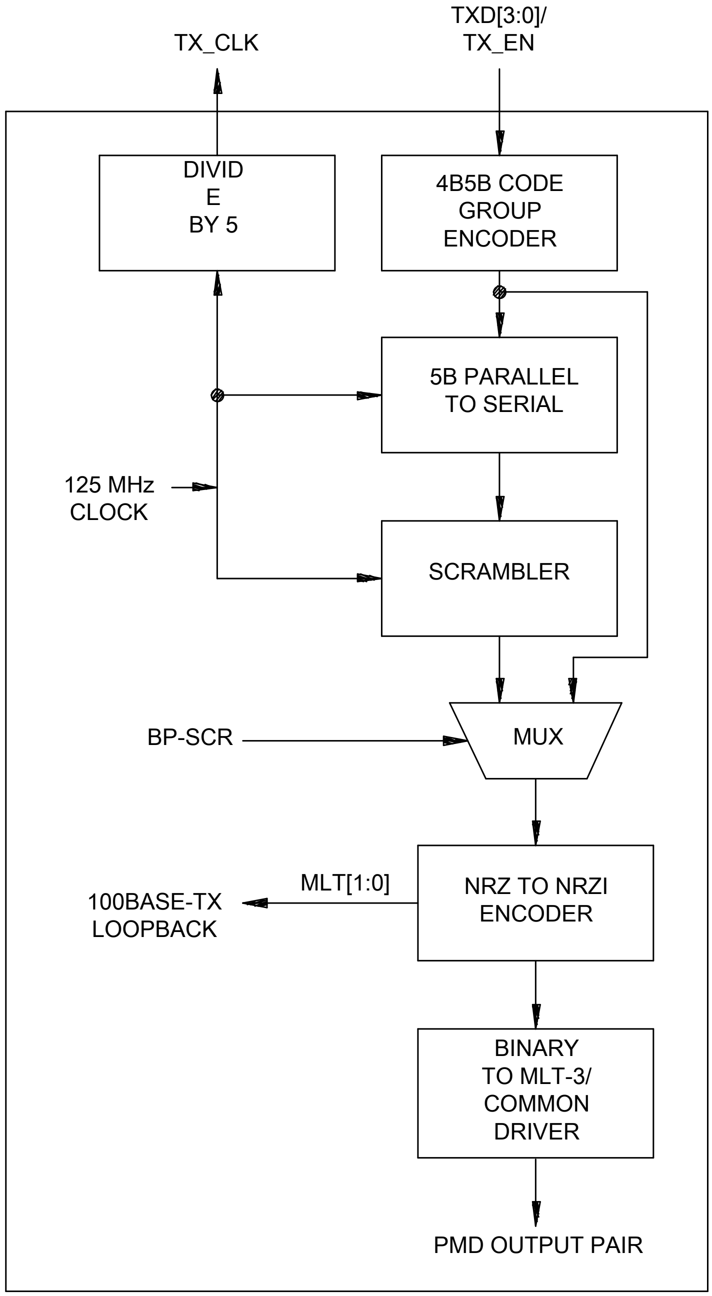


FIGURE 34. 100BASE-TX transmit block diagram.

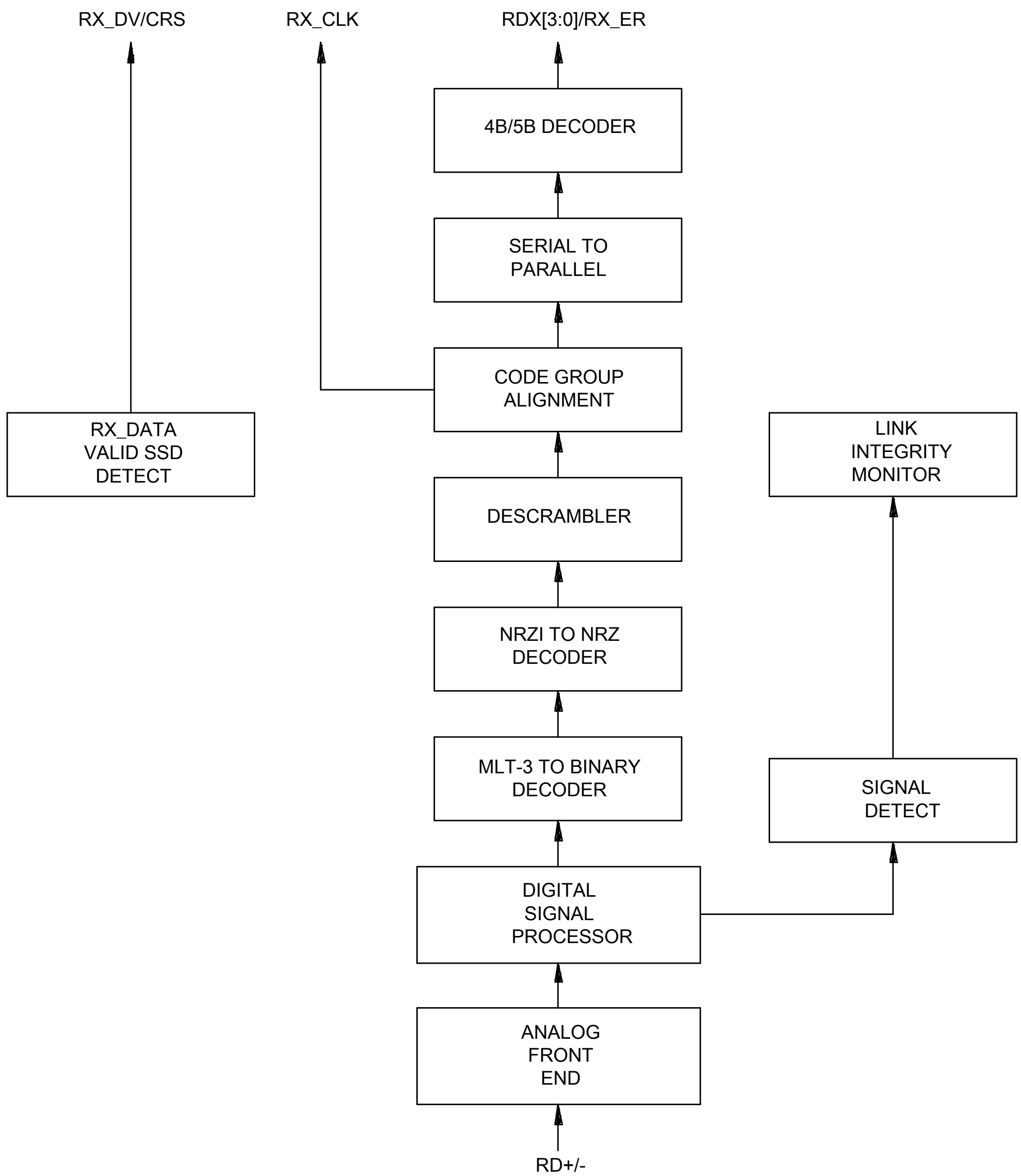


FIGURE 35. 100BASE-TX receive block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 3 (4000V) as tested.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top Side Marking	Orderable Part Number	Vendor part number
V62/12615-01XE	01295	DP83848EP	Tape and real, 1000	DP83848MPHPREP
			Tray, 250	DP83848MPHPEP
V62/12615-01YE	01295	DP83848EP	Tape and real, 1000	DP83848MPTBREP
			Tray, 250	DP83848MPTBEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243