

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add tube option under paragraph 6.3. - ro	12-08-06	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	18-08-07	C. SAFFLE
C	Add ANSI SEMI standard G30-88 reference to paragraph 2.0. Under Table I, add typical limits to test parameters. Update document to current requirements. - ro	24-01-04	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

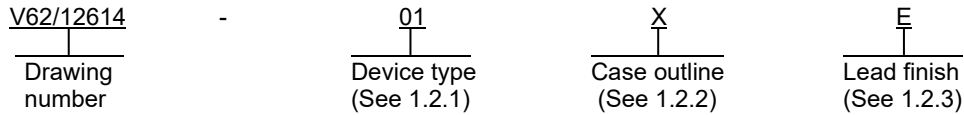
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12								

<b>PMIC N/A</b>  Original date of drawing YY-MM-DD 12-04-17	<b>PREPARED BY</b> RICK OFFICER		<b>DLA LAND AND MARITIME</b> COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/landandmaritime">https://www.dla.mil/landandmaritime</a>	
	<b>CHECKED BY</b> RAJESH PITHADIA		<b>TITLE</b> MICROCIRCUIT, LINEAR, DIFFERENCE AMPLIFIER, HIGH COMMON MODE VOLTAGE, MONOLITHIC SILICON	
	<b>APPROVED BY</b> CHARLES F. SAFFLE		<b>DWG NO.</b>  <b>V62/12614</b>	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high common mode voltage difference amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	INA149-EP	High common mode voltage difference amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Plastic small surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (+VS to -VS) .....	40 V
Input voltage range (continuous) .....	300 V
Common mode and differential, 10 seconds .....	500 V
Maximum voltage on REFA and REFB .....	-VS – 0.3 V to +VS + 0.3 V
Input current on any input pin .....	10 mA 2/
Output short circuit current duration .....	Indefinite
Junction temperature range (TJ) .....	+150°C
Storage temperature range (TSTG) .....	-65°C to +150°C
Electrostatic discharge (ESD) rating:	
Human body model (HBM) .....	1500 V
Charged device model (CDM) .....	1000 V
Machine model (MM) .....	100 V

1.4 Recommended operating conditions. 3/

Supply voltage range (+VS to -VS) .....	±15 V
Operating free-air temperature range (TA) .....	-55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient 4/	$\theta_{JA}$	110	°C/W
Thermal resistance, junction-to-case (top) 5/	$\theta_{JC(TOP)}$	57	°C/W
Thermal resistance, junction-to-board 6/	$\theta_{JB}$	54	°C/W
Characterization parameter, junction-to-top 7/	$\psi_{JT}$	11	°C/W
Characterization parameter, junction-to-board 8/	$\psi_{JB}$	53	°C/W

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ REFA and REFB are diode clamped to the power supply rails. Signal applied to these pins that can swing more than 0.3 V beyond the supply rails should be limited to 10 mA or less.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 4/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- 5/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- 6/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.
- 7/ Characterization parameter, junction-to-top ( $\psi_{JT}$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- 8/ Characterization parameter, junction-to-board ( $\psi_{JB}$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

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## 2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available from <https://www.ansi.org>.)

JEDEC Solid State Technology Association

EIA/JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)  
EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages  
EIA/JESD51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board  
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ +VS = +15 V, -VS = -15 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Gain section.							
Initial gain		V <sub>OUT</sub> = ±10.0 V	+25°C	01	1 typical		V/V
Gain error		V <sub>OUT</sub> = ±10.0 V	-55°C to +125°C	01		±0.047	%FSR
					±0.005 typical		
Gain versus temperature			-55°C to +125°C	01	±1.5 typical		ppm/ °C
Nonlinearity			+25°C	01		±0.001	%FSR
					±0.0005 typical		
Offset voltage section.							
Initial offset			-55°C to +125°C	01		3500	μV
					350 typical		
Initial offset versus temperature			-55°C to +125°C	01	2.5 typical		μV/°C
Initial offset versus supply (PSRR)		V <sub>S</sub> = ±2 V to ±18 V	-55°C to +125°C	01	90		dB
					120 typical		
Input section.							
Input differential impedance			+25°C	01	800 typical		kΩ
Input common mode impedance			+25°C	01	200 typical		kΩ
Input differential voltage range			+25°C	01	-13.5	13.5	V
Input common mode voltage range			+25°C	01	-275	275	V
Input common mode rejection ratio (CMRR)		At dc, V <sub>CM</sub> = ±275 V	-55°C to +125°C	01	84		dB
					98 typical		
		At ac, 500 Hz, V <sub>CM</sub> = 500 V <sub>PP</sub>	+25°C		90 typical		
		At ac, 1 kHz, V <sub>CM</sub> = 500 V <sub>PP</sub>	+25°C		90 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ +Vs = +15 V, -Vs = -15 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Output section.							
Output voltage range			-55°C to +125°C	01	-13.5	13.5	V
Output short circuit current			+25°C	01	±25 typical		mA
Output capacitive load drive		No sustained oscillations	+25°C	01	10 typical		nF
Output noise voltage section.							
Output noise voltage		0.01 Hz to 10 Hz	+25°C	01	20 typical		μV <sub>PP</sub>
		10 kHz			550 typical		nV / √Hz
Dynamic response section.							
Small signal bandwidth	SSBW		+25°C	01	500 typical		kHz
Slew rate	SR	V <sub>OUT</sub> = ±10 V step	-55°C to +125°C	01	1.7		V/μs
					5 typical		
Full power bandwidth	FPBW	V <sub>OUT</sub> = 20 V <sub>PP</sub>	+25°C	01	32 typical		kHz
Settling time	t <sub>s</sub>	0.01 %, V <sub>OUT</sub> = 10 V step	+25°C	01	7 typical		μs
Power supply section.							
Power supply voltage range	V <sub>S</sub>		+25°C	01	±2	±18	V
Quiescent current		V <sub>S</sub> = ±18 V, V <sub>OUT</sub> = 0 V	+25°C	01		950	μA
					810 typical		
Quiescent current versus temperature			-55°C to +125°C	01		1.1	mA
					0.95 typical		
Temperature range section.							
Specified temperature range				01	-55	+125	°C
Operating temperature range				01	-55	+125	°C
Storage temperature range				01	-65	+150	°C

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>3/</u> +VS = +5 V, -VS = 0 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Gain section.							
Initial gain		V <sub>OUT</sub> = 1.5 V to 3.5 V	+25°C	01	1 typical		V/V
Gain error		V <sub>OUT</sub> = 1.5 V to 3.5 V	+25°C	01	±0.005 typical		%FSR
Gain versus temperature			-55°C to +125°C	01	±1.5 typical		ppm/ °C
Nonlinearity			+25°C	01	±0.0005 typical		%FSR
Offset voltage section.							
Initial offset			+25°C	01	350 typical		μV
Initial offset versus temperature			-55°C to +125°C	01	3 typical		μV/°C
Initial offset versus supply (PSRR)		V <sub>S</sub> = 4 V to 5 V	+25°C	01	120 typical		dB
Input section.							
Input differential impedance			+25°C	01	800 typical		kΩ
Input common mode impedance			+25°C	01	200 typical		kΩ
Input common mode voltage range			+25°C	01	-20	25	V
Input common mode rejection ratio (CMRR)		At dc, V <sub>CM</sub> = -20 V to 25 V	+25°C	01	100 typical		dB
		At dc, versus temperature	-55°C to +125°C		100 typical		
		At ac, 500 Hz, V <sub>CM</sub> = 49 V <sub>PP</sub>	+25°C		100 typical		
		At ac, 1 kHz, V <sub>CM</sub> = 49 V <sub>PP</sub>	+25°C		90 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>3/</u> +Vs = +5 V, -Vs = 0 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Output section.							
Output voltage range			+25°C	01	1.7	3.4	V
Output short circuit current			+25°C	01	±15 typical		mA
Output capacitive load drive		No sustained oscillations	+25°C	01	10 typical		nF
Output noise voltage section.							
Output noise voltage		0.01 Hz to 10 Hz	+25°C	01	20 typical		μVPP
		10 kHz			550 typical		nV/ √Hz
Dynamic response section.							
Small signal bandwidth	SSBW		+25°C	01	500 typical		kHz
Slew rate	SR	VOUT = 2 V step	+25°C	01	5 typical		V/μs
Full power bandwidth	FPBW	VOUT = 2 VPP	+25°C	01	32 typical		kHz
Settling time	ts	0.01 %, VOUT = 2 V step	+25°C	01	7 typical		μs
Power supply section.							
Power supply voltage range	Vs		+25°C	01	5 typical		V
Quiescent current		Vs = 5 V	+25°C	01	810 typical		μA
Quiescent current versus temperature			-55°C to +125°C	01	1 typical		mA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, at TA = 25°C, RL = 2 kΩ connected to ground, and VCM = REFA = REF B = ground.

3/ Unless otherwise specified, at TA = 25°C, RL = 2 kΩ connected to 2.5 V, and VCM = REFA = REF B = 2.5 V.

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Case X

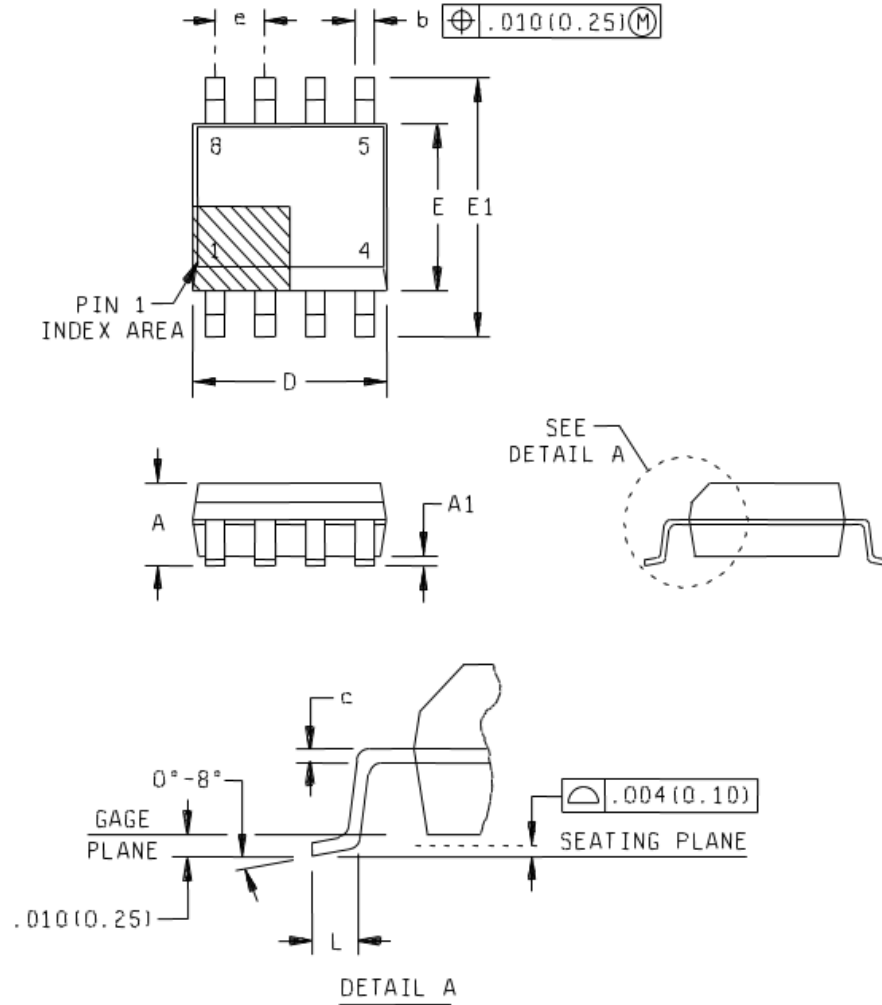


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash.
4. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	REFB	Reference input B.
2	-INPUT	Inverting input.
3	+INPUT	Noninverting input.
4	-VS	Negative supply voltage.
5	REFA	Reference input A.
6	VOUT	Output.
7	+VS	Positive supply voltage.
8	NC	No internal connection.

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/ 2/</u>	Device manufacturer CAGE code	Package marking	Mode of transportation	Vendor part number
V62/12614-01XE	01295	INA149AM	Tape and reel	INA149AMDREP
			Tube	INA149AMDEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer’s data sheet.

CAGE code

01295

Source of supply

Texas Instruments, Incorporated  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243

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