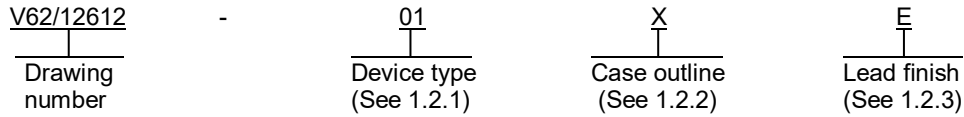




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power differential amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	THS4524-EP	Low power differential amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	38	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		<b>REV     B</b>	<b>PAGE    2</b>

1.3 Absolute maximum ratings. 1/

Supply voltage ( -Vs to +Vs ) .....	5.5 V
Input/output voltage ( ±VIN, ±VOUT, V <sub>OCM</sub> pins ) .....	-Vs – 0.7 V to +Vs + 0.7 V
Differential input voltage (VID) .....	1 V
Output current (IO) .....	100 mA
Input current (II) ( ±VIN, V <sub>OCM</sub> pins ) .....	10 mA
Continuous power dissipation (PD) .....	See table under 1.5
Maximum junction temperature range (T <sub>J</sub> ) .....	+150°C
Maximum junction temperature range (T <sub>J</sub> ) :	
Continuous operation, long term reliability .....	+125°C
Storage temperature range (T <sub>STG</sub> ) .....	-65°C to +150°C
Electrostatic discharge (ESD) ratings:	
Human body model (HBM) .....	1300 V
Charge device model (CDM) .....	1000 V
Machine model (MM) .....	50 V

1.4 Recommended operating conditions. 2/

Supply voltage range (Vs) .....	3.3 V and 5.0 V
Operating free-air temperature range (TA) .....	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV      B	PAGE    3

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient <u>3/</u>	$\theta_{JA}$	106.9	°C/W
Thermal resistance, junction-to-case (top) <u>4/</u>	$\theta_{JC(TOP)}$	59.8	°C/W
Thermal resistance, junction-to-board <u>5/</u>	$\theta_{JB}$	66.5	°C/W
Characterization parameter, junction-to-top <u>6/</u>	$\psi_{JT}$	17.1	°C/W
Characterization parameter, junction-to-board <u>7/</u>	$\psi_{JB}$	66.1	°C/W

3/ The thermal resistance, junction-to-ambient under natural convection is obtained in a simulation on a JEDEC standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

4/ The thermal resistance, junction-to-case (top) is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5/ The thermal resistance, junction-to-board is obtained by simulating in an environment with a ring cold plate fixture to control the printed circuit board (PCB) temperature, as described in JESD51-8.

6/ Characterization parameter, junction-to-top ( $\psi_{JT}$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

7/ Characterization parameter, junction-to-board ( $\psi_{JB}$ ) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV B	PAGE 4

2. APPLICABLE DOCUMENTS

AMERICAN NATIONAL STANDARDS INSTITUTE, SEMICONDUCTOR EQUIPMENT and MATERIALS INTERNATIONAL

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at <https://www.ansi.org>)

JEDEC Solid State Technology Association

- EIA/JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- EIA/JESD51-8 – Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV B	PAGE 5

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ +V <sub>S</sub> = 3.3 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
AC performance.							
Small signal bandwidth	SSBW	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 1	-55°C to +125°C	01	135 typical		MHz
		V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 2			49 typical		
		V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 5			18.6 typical		
		V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10			9.3 typical		
Gain bandwidth product	GBWP	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10	-55°C to +125°C	01	93 typical		MHz
Large signal bandwidth	LSBW	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	-55°C to +125°C	01	95 typical		MHz
Bandwidth for 0.1 dB flatness		V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	-55°C to +125°C	01	20 typical		MHz
Rising slew rate (differential)	SR	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	420 typical		V/μs
Falling slew rate (differential)	SR	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	460 typical		V/μs
Overshoot	OS	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	1.2 typical		%
Undershoot	US	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	2.1 typical		%
Rise time	t <sub>R</sub>	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	4 typical		ns
Fall time	t <sub>F</sub>	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	3.5 typical		ns
Settling time to 1 %	t <sub>S</sub>	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	13 typical		ns
Second harmonic distortion	2 nd HD	f = 1 kHz, V <sub>OUT</sub> = 1 V <sub>RMS</sub> , 3/ G = 1 , differential input	-55°C to +125°C	01	-122 typical		dBc
		f = 1 MHz, V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1			-85 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		<b>REV B</b>	<b>PAGE 6</b>

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12612
REV B	PAGE 7		

See footnotes at end of table.

Test	Symbol	Conditions <sup>2/</sup> +VS = 3.3 V, -VS = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits Min Max	Unit
AC performance – continued.						
Third harmonic distortion	3 rd HD	f = 1 kHz, VOUT = 1 VRMS, <sup>3/</sup> G = 1, differential input	-55°C to +125°C	01	-141 typical	dBc
					f = 1 MHz, VOUT = 2 VPP, G = 1	-90 typical
Second order intermodulation distortion		Two tone, f <sub>1</sub> = 2 MHz, f <sub>2</sub> = 2.2 MHz, VOUT = 2 VPP envelope	-55°C to +125°C	01	-83 typical	dBc
Third order intermodulation distortion		Two tone, f <sub>1</sub> = 2 MHz, f <sub>2</sub> = 2.2 MHz, VOUT = 2 VPP envelope	-55°C to +125°C	01	-90 typical	dBc
Input voltage noise		f > 10 kHz	-55°C to +125°C	01	4.6 typical	nV / √Hz
Input current noise		f > 100 kHz	-55°C to +125°C	01	0.6 typical	pA / √Hz
Overdrive recovery time		Overdrive = ±0.5 V	-55°C to +125°C	01	80 typical	ns
Output balance error		VOUT = 100 mV, f ≤ 2 MHz, differential input	-55°C to +125°C	01	-57 typical	dB
Closed loop output impedance		f = 1 MHz (differential)	-55°C to +125°C	01	0.3 typical	Ω
Channel to channel crosstalk		f = 10 kHz, measured differentially	-55°C to +125°C	01	-125 typical	dB

TABLE 1. Electrical performance characteristics – Continued. <sup>1/</sup>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> +V <sub>S</sub> = 3.3 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
DC performance.							
Open loop voltage gain	AOL		-55°C to +125°C	01	80		dB
Input referred offset voltage			-55°C to +125°C	01		±7	mV
Input offset voltage <u>4/</u> drift			-55°C to +125°C	01	±2 typical		μV/°C
Input bias current	I <sub>IB</sub>		-55°C to +125°C	01		3.8	μA
Input bias current <u>4/</u> drift			-55°C to +125°C	01	±1.75 typical		nA/°C
Input offset current	I <sub>IO</sub>		-55°C to +125°C	01		±2.0	μA
Input offset current <u>4/</u> drift			-55°C to +125°C	01	±0.1 typical		nA/°C
Input section.							
Common mode input voltage low			-55°C to +125°C	01		0	V
Common mode input voltage high			-55°C to +125°C	01	1.8		V
Common mode rejection ratio	CMRR		-55°C to +125°C	01	73.8		dB
Input resistance	R <sub>IN</sub>	<u>5/</u>	-55°C to +125°C	01	110  1.5 typical		kΩ  pF
Output section.							
Output voltage low	V <sub>OL</sub>		-55°C to +125°C	01		0.2	V
Output voltage high	V <sub>OH</sub>		-55°C to +125°C	01	2.95		V
Output current drive (for linear operation)		R <sub>L</sub> = 50 Ω	-55°C to +125°C	01	±35 typical		mA

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV B	PAGE 8

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ +V <sub>S</sub> = 3.3 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Power supply section.							
Specified operating voltage			-55°C to +125°C	01	2.5	5.5	V
Quiescent operating current, per channel			-55°C to +125°C	01	0.85	1.25	mA
Power supply rejection ratio	±PSRR		-55°C to +125°C	01	65		dB
Power down section.							
Enable voltage threshold		Assured "on" above 2.1 V	-55°C to +125°C	01		2.1	V
Disable voltage threshold		Assured "off" below 0.7 V	-55°C to +125°C	01	0.7		V
Disable pin bias current			-55°C to +125°C	01	1 typical		μA
Power down quiescent current			-55°C to +125°C	01	10 typical		μA
Turn on time delay		Time to V <sub>OUT</sub> = 90% of final value, V <sub>IN</sub> = 2 V, R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	108 typical		ns
Turn off time delay		Time to V <sub>OUT</sub> = 10% of original value, V <sub>IN</sub> = 2 V, R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	88 typical		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		<b>REV B</b>	<b>PAGE 9</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ +Vs = 3.3 V, -Vs = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
VOCM voltage control section.							
Small signal bandwidth	SSBW		-55°C to +125°C	01	23 typical		MHz
Slew rate	SR		-55°C to +125°C	01	55 typical		V/μs
Gain			-55°C to +125°C	01	0.98	1.021	V/V
Common mode offset voltage from VOCM input		Measured at VOUT with VOCM input driven, VOCM = 1.65 V ±0.5 V	-55°C to +125°C	01		±7	mV
Input bias current		VOCM = 1.65 V ±0.5 V	-55°C to +125°C	01		±8	μA
VOCM voltage range			-55°C to +125°C	01	0.8 to 2.5 typical		V
Input impedance		6/	-55°C to +125°C	01	72  1.5 typical		kΩ  pF
Default output common mode voltage offset from (+Vs - -Vs) / 2		Measured at VOUT with VOCM input open	-55°C to +125°C	01		±5	mV

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV      B	PAGE    10

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u> +V <sub>S</sub> = 5.0 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
AC performance.							
Small signal bandwidth	SSBW	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 1	-55°C to +125°C	01	145 typical		MHz
		V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 2			50 typical		
		V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 5			20 typical		
		V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10			9.5 typical		
Gain bandwidth product	GBWP	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10	-55°C to +125°C	01	95 typical		MHz
Large signal bandwidth	LSBW	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	-55°C to +125°C	01	145 typical		MHz
Bandwidth for 0.1 dB flatness	BW	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	-55°C to +125°C	01	30 typical		MHz
Rising slew rate (differential)	SR	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	490 typical		V/μs
Falling slew rate (differential)	SR	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	600 typical		V/μs
Overshoot	OS	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	1 typical		%
Undershoot	US	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	2.6 typical		%
Rise time	t <sub>R</sub>	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	3.4 typical		ns
Fall time	t <sub>F</sub>	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	3 typical		ns
Settling time to 1 %	t <sub>S</sub>	V <sub>OUT</sub> = 2 V step, G = 1 , R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	10 typical		ns
Second harmonic distortion	2 nd HD	f = 1 kHz, V <sub>OUT</sub> = 1 V <sub>RMS</sub> , <u>3/</u> G = 1 , differential input	-55°C to +125°C	01	-122 typical		dBc
		f = 1 MHz, V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1			-85 typical		

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		<b>REV B</b>	<b>PAGE 11</b>

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12612
REV B	PAGE 12		

See footnotes at end of table.

Test	Symbol	Conditions $\bar{Z}$ +VS = 5.0 V, -VS = 0 V, unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Third harmonic distortion	3 rd HD	f = 1 kHz, VOUT = 1 VRMS, $\bar{Z}$ G = 1, differential input	-55°C to +125°C	01	-141 typical		dBc
Second order intermodulation distortion		Two tone, f <sub>1</sub> = 2 MHz, f <sub>2</sub> = 2.2 MHz, VOUT = 2 VPP envelope	-55°C to +125°C	01	-86 typical		dBc
Third order intermodulation distortion		Two tone, f <sub>1</sub> = 2 MHz, f <sub>2</sub> = 2.2 MHz, VOUT = 2 VPP envelope	-55°C to +125°C	01	-93 typical		dBc
Input voltage noise		f > 10 kHz	-55°C to +125°C	01	4.6 typical		nV / $\sqrt{\text{Hz}}$
Input current noise		f > 100 kHz	-55°C to +125°C	01	0.6 typical		pA / $\sqrt{\text{Hz}}$
Signal to noise ratio	SNR	VOUT = 5 VPP, 20 Hz to 22 kHz BW, differential input	-55°C to +125°C	01	114 typical		dBc
Total harmonic distortion plus noise	THD+N	VOUT = 5 VPP, f = 1 kHz, 20 Hz to 22 kHz BW, differential input	-55°C to +125°C	01	112 typical		dBc
Overdrive recovery time		Overdrive = $\pm 0.5$ V	-55°C to +125°C	01	75 typical		ns
Output balance error		VOUT = 100 mV, f $\leq$ 2 MHz, differential input	-55°C to +125°C	01	-57 typical		dB
Closed loop output impedance		f = 1 MHz (differential)	-55°C to +125°C	01	0.3 typical		$\Omega$
Channel to channel crosstalk		f = 10 kHz, measured differentially	-55°C to +125°C	01	-125 typical		dB

AC performance – continued.

TABLE 1. Electrical performance characteristics – Continued. <sup>1/</sup>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> +V <sub>S</sub> = 5.0 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
DC performance.							
Open loop voltage gain	AOL		-55°C to +125°C	01	83		dB
Input referred offset voltage			-55°C to +125°C	01		±8	mV
Input offset voltage <u>4/</u> drift			-55°C to +125°C	01	±2 typical		μV/°C
Input bias current	I <sub>IB</sub>		-55°C to +125°C	01		5.5	μA
Input bias current <u>4/</u> drift			-55°C to +125°C	01	±1.8 typical		nA/°C
Input offset current	I <sub>IO</sub>		-55°C to +125°C	01		±1.7	μA
Input offset current <u>4/</u> drift			-55°C to +125°C	01	±0.1 typical		nA/°C
Input section.							
Common mode input voltage low			-55°C to +125°C	01		0	V
Common mode input voltage high			-55°C to +125°C	01	3.5		V
Common mode rejection ratio	CMRR		-55°C to +125°C	01	80		dB
Input impedance		<u>6/</u>	-55°C to +125°C	01	100  0.7 typical		kΩ  pF
Output section.							
Output voltage low	V <sub>OL</sub>		-55°C to +125°C	01		0.2	V
Output voltage high	V <sub>OH</sub>		-55°C to +125°C	01	4.65		V
Output current drive (for linear operation)		R <sub>L</sub> = 50 Ω	-55°C to +125°C	01	±55 typical		mA

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV    B	PAGE    13

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ +V <sub>S</sub> = 5.0 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Power supply section.							
Specified operating voltage			-55°C to +125°C	01	2.5	5.5	V
Quiescent operating current, per channel			-55°C to +125°C	01	0.9	1.4	mA
Power supply rejection ratio	±PSRR		-55°C to +125°C	01	62		dB
Power down section.							
Enable voltage threshold		Assured "on" above 2.1 V	-55°C to +125°C	01		2.1	V
Disable voltage threshold		Assured "off" below 0.7 V	-55°C to +125°C	01	0.7		V
Disable pin bias current			-55°C to +125°C	01	1 typical		μA
Power down quiescent current			-55°C to +125°C	01	20 typical		μA
Turn on time delay		Time to V <sub>OUT</sub> = 90% of final value, V <sub>IN</sub> = 2 V, R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	70 typical		ns
Turn off time delay		Time to V <sub>OUT</sub> = 10% of original value, V <sub>IN</sub> = 2 V, R <sub>L</sub> = 200 Ω	-55°C to +125°C	01	60 typical		ns

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		<b>REV B</b>	<b>PAGE 14</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ +V <sub>S</sub> = 5.0 V, -V <sub>S</sub> = 0 V, unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
V <sub>OCM</sub> voltage control section.							
Small signal bandwidth	SSBW		-55°C to +125°C	01	23 typical		MHz
Slew rate	SR		-55°C to +125°C	01	55 typical		V/μs
Gain			-55°C to +125°C	01	0.98	1.021	V/V
Common mode offset voltage from V <sub>OCM</sub> input		Measured at V <sub>OUT</sub> with V <sub>OCM</sub> input driven, V <sub>OCM</sub> = 2.5 V ±1 V	-55°C to +125°C	01		±12.5	mV
Input bias current		V <sub>OCM</sub> = 2.5 V ±1 V	-55°C to +125°C	01		±25	μA
V <sub>OCM</sub> voltage range			-55°C to +125°C	01	0.8 to 4.2 typical		V
Input impedance		6/	-55°C to +125°C	01	46  1.5 typical		kΩ  pF
Default output common mode voltage offset from (+V <sub>S</sub> - -V <sub>S</sub> ) / 2		Measured at V <sub>OUT</sub> with V <sub>OCM</sub> input open	-55°C to +125°C	01		±8	mV

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, V<sub>OCM</sub> = open, V<sub>OUT</sub> = 2 V<sub>PP</sub> (differential), R<sub>L</sub> = 1 kΩ differential, G = 1 V/V, single ended input, differential output, and input and output referenced to midsupply.
- 3/ Not directly measureable, calculated using noise gain of 101 as described in manufacturer's datasheet.
- 4/ Input offset voltage drift, input bias current drift, and input offset current are average values calculated by taking data at -55°C and +125°C, computing the difference, and dividing by 180.
- 5/ The || symbolizes that the input resistance is being represented as the resistance value is in parallel with the capacitance.
- 6/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		<b>REV B</b>	<b>PAGE 15</b>

Case X

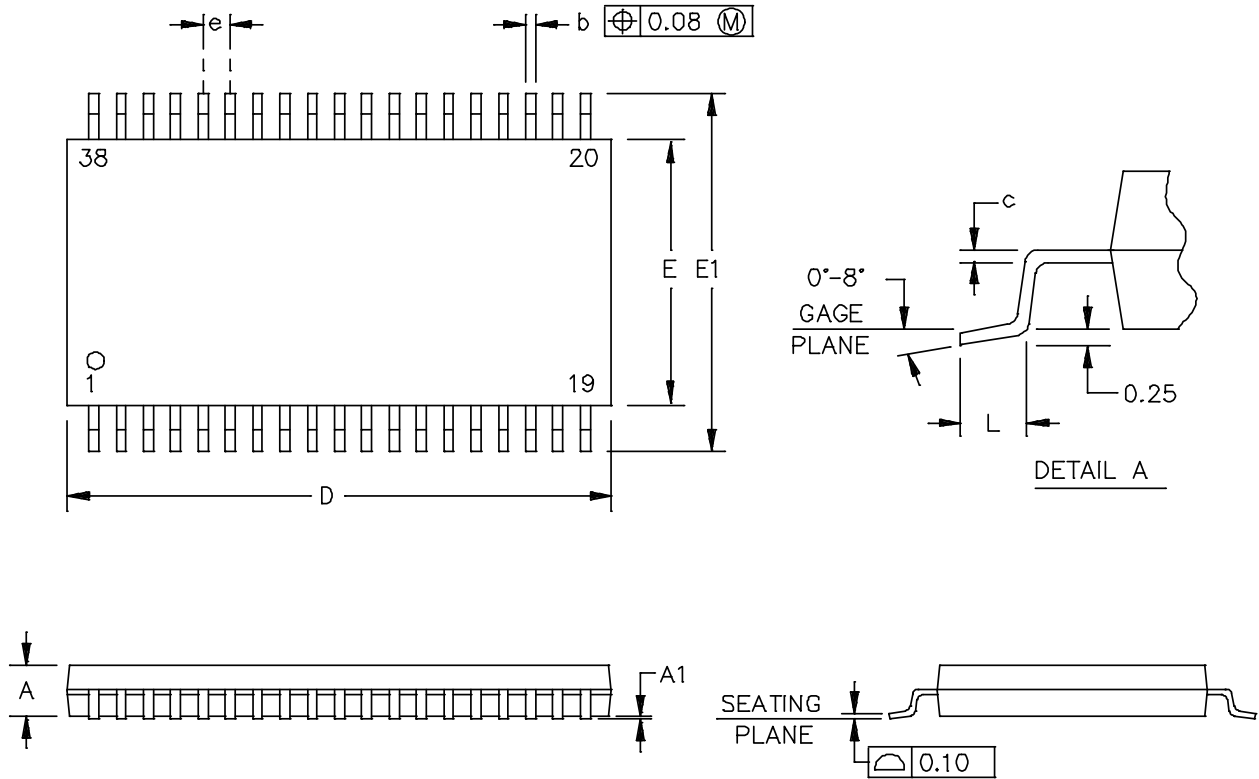


FIGURE 1. Case outline

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE <b>A</b></p>	<p>CODE IDENT NO. <b>16236</b></p>	<p>DWG NO. <b>V62/12612</b></p>
		<p>REV    <b>B</b></p>	<p>PAGE    <b>16</b></p>

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.001	0.005	0.05	0.15
b	0.006	0.016	0.17	0.27
c	0.005 nominal		0.15 nominal	
D	0.377	0.385	9.60	9.80
E	0.169	0.177	4.30	4.50
E1	0.244	0.259	6.20	6.60
e	0.019 BSC		0.50 BSC	
L	0.019	0.029	0.50	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion.
3. Falls within reference to JEDEC MO-153.

FIGURE 1. Case outline - continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV    B	PAGE    17

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	$\overline{\text{PD}} 1$	Power down 1. $\overline{\text{PD}}$ = logic low puts channel into low power mode. $\overline{\text{PD}}$ = logic high or open for normal operation.
2	+VIN1	Noninverting amplifier 1 input.
3	-VIN1	Inverting amplifier 1 input.
4	VOCM1	Common mode voltage input 1
5	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
6	$\overline{\text{PD}} 2$	Power down 2. $\overline{\text{PD}}$ = logic low puts channel into low power mode. $\overline{\text{PD}}$ = logic high or open for normal operation.
7	+VIN2	Noninverting amplifier 2 input.
8	-VIN2	Inverting amplifier 2 input.
9	VOCM2	Common mode voltage input 2.
10	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
11	$\overline{\text{PD}} 3$	Power down 3. $\overline{\text{PD}}$ = logic low puts channel into low power mode. $\overline{\text{PD}}$ = logic high or open for normal operation.
12	+VIN3	Noninverting amplifier 3 input.
13	-VIN3	Inverting amplifier 3 input.
14	VOCM3	Common mode voltage input 3.
15	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
16	$\overline{\text{PD}} 4$	Power down 4. $\overline{\text{PD}}$ = logic low puts channel into low power mode. $\overline{\text{PD}}$ = logic high or open for normal operation.
17	+VIN4	Noninverting amplifier 4 input.
18	-VIN4	Inverting amplifier 4 input.
19	VOCM4	Common mode voltage input 4.

FIGURE 2. Terminal connections.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV B	PAGE 18

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
20	+VS4	Amplifier 4 positive power supply input.
21	+VOUT4	Noninverting amplifier 4 output.
22	-VOUT4	Inverting amplifier 4 output.
23	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
24	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
25	+VS3	Amplifier 3 positive power supply input.
26	+VOUT3	Noninverting amplifier 3 output.
27	-VOUT3	Inverting amplifier 3 output.
28	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
29	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
30	+VS2	Amplifier 2 positive power supply input.
31	+VOUT2	Noninverting amplifier 2 output.
32	-VOUT2	Inverting amplifier 2 output.
33	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
34	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.
35	+VS1	Amplifier 1 positive power supply input.
36	+VOUT1	Noninverting amplifier 1 output.
37	-VOUT1	Inverting amplifier 1 output.
38	-VS	Negative power supply input. Note that -VS is tied together on multi-channel devices.

FIGURE 2. Terminal connections - continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV B	PAGE 19

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/ 2/</u>	Device manufacturer CAGE code	Transportation mode and quantity	Top side marking	Vendor part number
V62/12612-01XE	01295	Reel of 2000	THS4524EP	THS4524MDBTREP
		Tube of 50		THS4524MDBTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/12612</b>
		REV B	PAGE 20