REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct vendor part in section 6.3. - PHN	12-06-04	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-04-16	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	23-08-24	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
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REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing

YY MM DD

12-05-01

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil/

TITLE
MICROCIRCUIT, DIGITAL, 9 CHANNEL RS-422/ RS-485 TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/12607
REV C		PAGE 1 OF 14

AMSC N/A

5962-V142-23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 9 channel RS-422/ RS-485 transceiver microcircuit, with an operating temperature range of -40ºC to +85ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12607	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65HVD09-EP	9 channel RS-422/ RS-485 transceiver

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	56	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC}) ..... -0.3 V to 6.0 V 2/
Bus voltage range ..... -10 V to 15 V
Data I/O and control (A side) voltage range ..... -0.3 V to V_{CC} + 0.5 V
Receiver output current (IO) ..... ±40 mA
Electrostatic discharge:
B side and GND, ESD HBM ..... 12 kV
B side and GND, ESD MM ..... 400 V
All terminals, ESD HBM ..... 4 kV
All terminals, ESD MM ..... 400 V
Continuous total power dissipation ..... Internally limited 3/
Dissipation ratings

Package	$T_A \leq 25°C$	Operating factor 4/ above $T_A = 25°C$	$T_A = 70°C$ Power rating	$T_A = 70°C$ Power rating
Case X	2500 mW	20 mW/°C	1600 mW	1300 mW

Thermal characteristics

	Typical	Unit
Junction to ambient thermal resistance (θ_{JA})	50	°C/W
Junction to case (top) thermal resistance (θ_{JA})	27	°C/W
Thermal shutdown temperature (T_{SD})	165	°C

1.4 Recommended operating conditions.

Supply voltage, (V_{CC}) ..... 4.75 V to 5.25 V
Minimum high level input voltage, (V_{IH}) (except nB+, nB-) 5/ ..... 2.0 V
Maximum low level input voltage, (V_{IL}) (except nB+, nB-) 5/ ..... 0.8 V
Voltage at any bus terminal, (V_O, V_I, V_{IC}) (separately or common mode) (nB+ or nB-) ..... - 7.0 V to 12.0 V
Output current:
Driver ..... -60 mA to 60 mA
Receiver ..... -8 mA to 8 mA
Operating free air temperature, (T_A) ..... -40°C to 85°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to the GND terminals.
3/ The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.
4/ This is inverse of the junction to ambient temperature when board mounted and with no air flow.
5/ n = 1 – 9.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Driver test circuit, RS-422 and RS-485 loading. The driver test circuit, RS-422 and RS-485 loading shall be as shown in figure 5.

3.5.6 Driver test circuit, pull-up and pull down loading. The driver test circuit, pull-up and pull-down loading shall be as shown in figure 6.

3.5.7 Driver delay and transition time test waveforms. The Driver delay and transition time test waveforms shall be as shown in figure 7.

3.5.8 Receiver propagation delay and transition time test circuit. The receiver propagation delay and transition time test circuit shall be as shown in figure 8.

3.5.9 Receiver delay and transition time waveforms. The receiver delay and transition time waveforms shall be as shown in figure 9.

3.5.10 Driver enable and disable time test circuit. The driver enable and disable time test circuit shall be as shown in figure 10.

3.5.11 Driver enable time waveforms. The driver enable time waveforms shall be as shown in figure 11.

3.5.12 Receiver enable and disable time test circuit. The receiver enable and disable time test circuit shall be as shown in figure 12.

3.5.13 Receiver enable and disable time waveforms. The receiver enable and disable time waveforms shall be as shown in figure 13.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/		Limits Min	Limits Max	Unit
Driver differential output voltage magnitude	$\|V_{DD}\|$	RS-422 load RL = 100 Ω See figure 5		0.56		V
		RS-485 load RL = 54 Ω See figure 5		1.4	TYP	V
		Pull up Pull-down load See figure 6		1		V
High level output voltage	V_{OH}	A side, I_{OH} = -8 mA, V_{ID} = 200 mV See figure 8		4		V
		B side, See figure 6		3	TYP	V
Low level output voltage	V_{OL}	A side, I_{OH} = 8 mA, V_{ID} = -200 mV See figure 8			0.8	V
		B side, See figure 6		1	TYP	V
Receiver positive going differential input threshold voltages	V_{IT+}	I_{OH} = -8 mA See figure 8			0.2	V
Receiver negative going differential input threshold voltages	V_{IT-}	I_{OH} = 8 mA See figure 8		-0.2		V
Receiver input hysteresis (V_{IT+} - V_{IT-})	V_{hys}	V_{CC} = 5 V, TA = 25°C		24		mV
Bus input current	I_I	V_{IH} = 12 V, V_{CC} = 5 V	Other input at 0 V		1	mA
		V_{IH} = 12 V, V_{CC} = 0 V			1	mA
		V_{IH} = -7 V, V_{CC} = 5 V		-0.8		mA
		V_{IH} = -7 V, V_{CC} = 0 V		-0.8		mA
High level input current	I_{IH}	nA, BSR, DE/$\overline{RE}$, and $\overline{CRE}$, V_{IH} = 2 V		-100		µA
		CDE0, CDE1, and CDE2 V_{IH} = 2 V			100	µA
Low level input current	I_{IL}	nA, BSR, DE/$\overline{RE}$, and $\overline{CRE}$, V_{IH} = 0.8 V		-100		µA
		CDE0, CDE1, and CDE2 V_{IH} = 0.8 V			100	µA
Short circuit output current	I_{OS}	nB+ on nB-			±260	mA
High impedance state output current	I_{OZ}	nA		See I_{IH} and I_{IL}		mA
		nB+ or nB-		See I_{II}		mA
Supply current	I_{CC}	Disabled			10	mA
		All drivers enabled, no load			60	mA
		All receivers enabled, no load			45	mA
Output capacitance	C_O	nB+ or nB- to GND		18	TYP	pF
Power dissipation capacitance 3/	C_{pd}	Receiver		40	TYP	pF
		Driver		100	TYP	pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Driver switching characteristics					
Propagation delay time, t_{PHL} or t_{PLH} (see figure 6 and 7)	t_{pd}		2.5	13.5	ns
Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$			5	ns
Fall time	t_f	S1 to B, See figure 7		4 TYP	ns
Rise time	t_r	See figure 7		8 TYP	ns
Enable time, control inputs to active output	t_{en}			50	ns
Disable time, control inputs to high impedance output	t_{dis}			225	ns
Propagation delay time, high level to high impedance output	t_{PHZ}	See figure 10 and 11		225	ns
Propagation delay time, low level to high impedance output	t_{PLZ}			225	ns
Propagation delay time, high impedance to high level output	t_{PZH}			50	ns
Propagation delay time, high impedance to low level output	t_{PZL}			50	ns
Receiver switching characteristics					
Propagation delay time, t_{PHL} or t_{PLH} (see figure 6 and 7)	t_{pd}		8	14.5	ns
Skew limit, maximum t_{pd} – minimum t_{pd} 4/	$t_{sk(lim)}$			5	ns
Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$			5	ns
Transition time (t_r or t_f)	t_t	See figure 9		2 TYP	ns
Enable time, control inputs to active output	t_{en}			31 TYP	ns
Disable time, control inputs to high impedance output	t_{dis}			41 TYP	ns
Propagation delay time, high level to high impedance output	t_{PHZ}	See figure 12 and 13		34 TYP	ns
Propagation delay time, low level to high impedance output	t_{PLZ}			14 TYP	ns
Propagation delay time, high impedance to high level output	t_{PZH}			30 TYP	ns
Propagation delay time, high impedance to low level output	t_{PZL}			30 TYP	ns

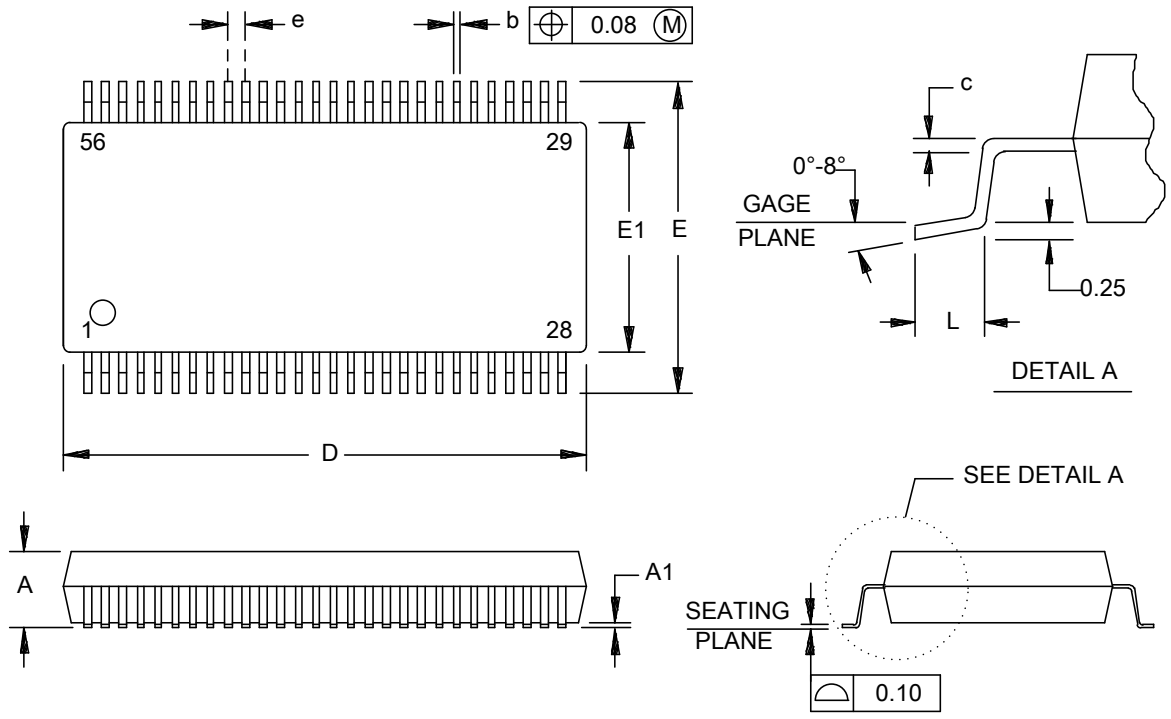
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating free air temperature range (unless otherwise noted). All typical values are with respect to V_{CC} = 5 V, and T_A = 25°C.

3/ C_{pd} determines the no-load dynamic supply current consumption, $I_S = C_{PD} \times V_{CC} \times f + I_{CC}$.

4/ This parameter is applicable at one VCC and operating temperature with the recommended operating conditions and to any two devices.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millim eters	
	Min	Max		Min	Max
A		1.20	E	7.90	8.30
A1	0.05	0.15	E1	6.00	6.20
b	0.17	0.27	e	0.50 TYP	
c	0.15 NOM		L	0.50	0.75
D	13.90	14.10			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold protrusions not exceed 0.15.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outlines.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	15	GND	29	1B-	43	GND
2	BSR	16	GND	30	1B+	44	GND
3	$\overline{CRE}$	17	GND	31	2B-	45	V_{CC}
4	1A	18	V_{CC}	32	2B+	46	6B-
5	1DE/$\overline{RE}$	19	5A	33	3B-	47	6B+
6	3A	20	5DE/$\overline{RE}$	34	3B+	48	7B-
7	2DE/$\overline{RE}$	21	6A	35	4B-	49	7B+
8	V_{CC}	22	6DE/$\overline{RE}$	36	4B+	50	8B-
9	3DE/$\overline{RE}$	23	7A	37	5B-	51	8B+
10	4A	24	7DE/$\overline{RE}$	38	5B+	52	9B-
11	4DE/$\overline{RE}$	25	8A	39	V_{CC}	53	9B+
12	V_{CC}	26	8DE/$\overline{RE}$	40	GND	54	CDE0
13	GND	27	9A	41	GND	55	CDE1
14	GND	28	9DE/$\overline{RE}$	42	GND	56	CDE2

FIGURE 2. Terminal connections.

Terminal		I/O	Description
Name	No.		
1A to 9A	4, 6, 8, 10, 19,21, 23, 25, 27	I/O	1A to 9A carry data to and from the communication controller
1b- to 9B-	29, 31, 33, 35, 37, 46, 48, 50, 52	I/O	1B- to 9B- are the inverted data signals of the balanced pair to/from the bus
1B+ to 9B+	30, 32, 34, 36, 38, 47, 49, 51, 53	I/O	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus
BSR	2	I	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired OR drivers when BSR and DE/$\overline{RE}$ and CDE1 and CDE2 are high. Channel 9 is placed in a high impedance state with BSR high
CDE0	54	I	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/$\overline{RE}$ - 9DE/$\overline{RE}$ are high.
CDE1	55	I	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	56	I	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
$\overline{CRE}$	3	I	$\overline{CRE}$ is the common receiver enabled. When high, CRE diables receiver channel 5 to 9.
1DE/$\overline{RE}$ to 9DE/$\overline{RE}$	5, 7, 9, 11, 20, 22, 24, 26, 28	I	1DE/$\overline{RE}$ - 9DE/$\overline{RE}$ are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/$\overline{RE}$ to 9DE/$\overline{RE}$ and CRE and BSR are low and CDE1 and CDE2 are low
GND	1, 13, 14, 15, 16, 17, 40, 41, 42, 43, 44	Power	GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity. 1/
V_{CC}	12, 18, 39, 45	Power	Supply voltage.

1. Terminal 1 must be connected to signal ground for proper operation.

FIGURE 3. Terminal function.

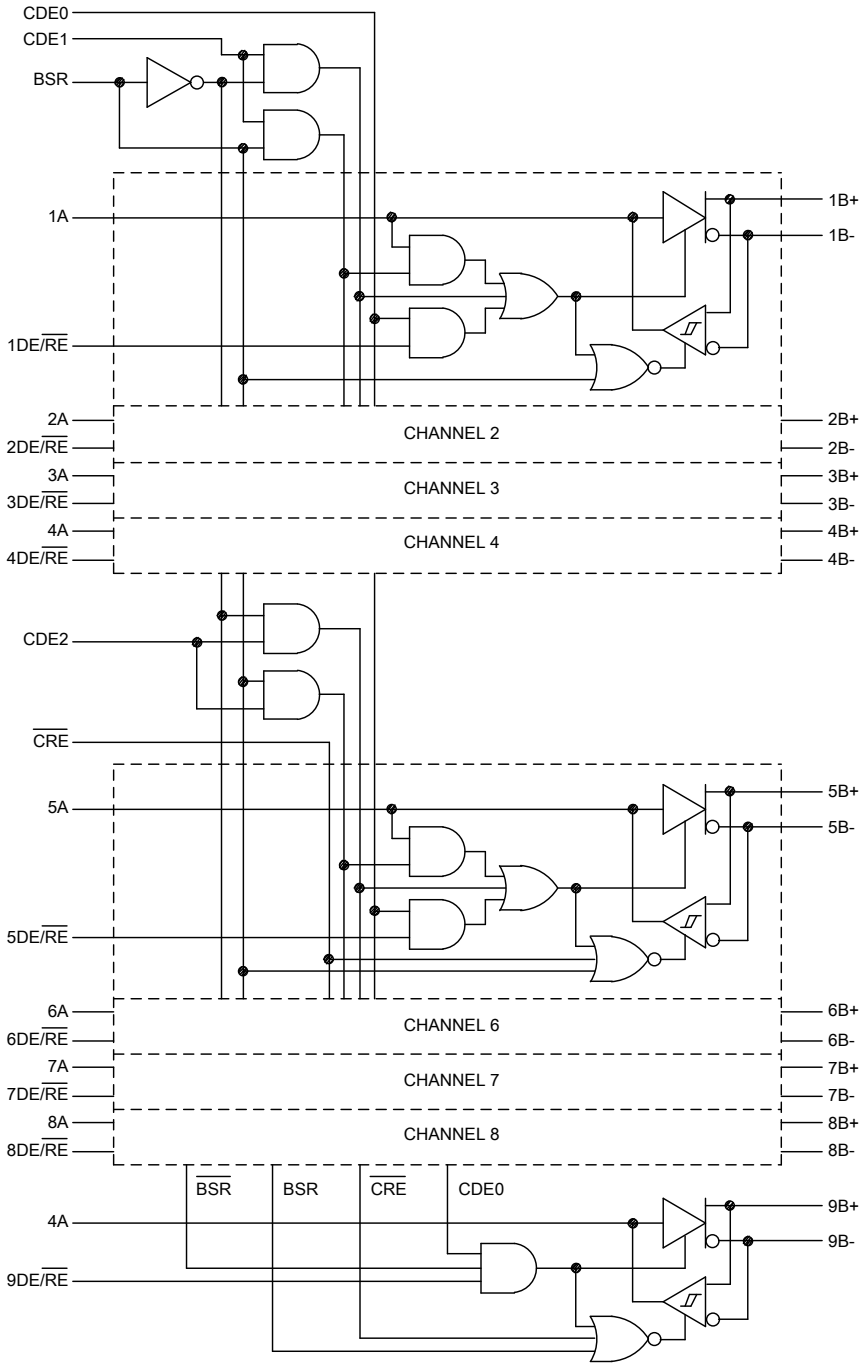
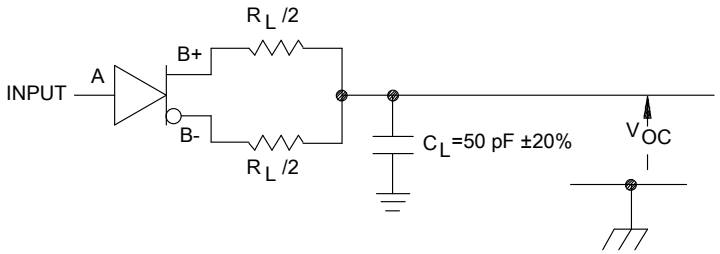
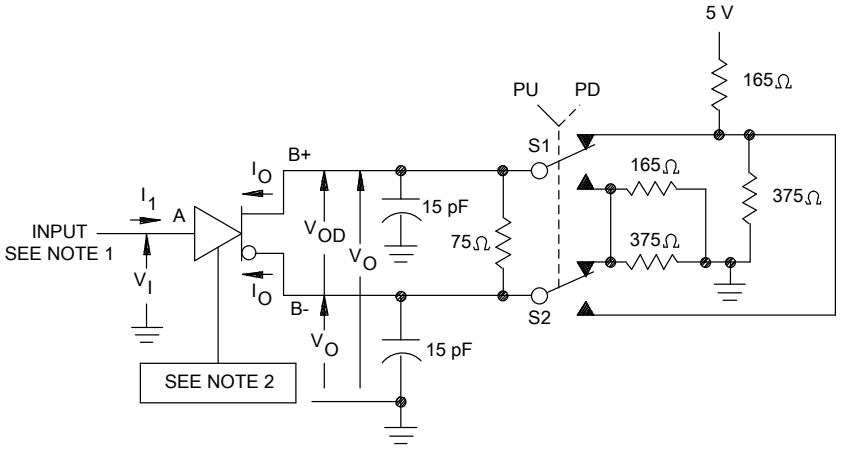


FIGURE 4. Logic diagram.



C_L INCLUDES FIXTURE AND
INSTRUMENTATION CAPACITANCE

FIGURE 5. Driver test circuit, RS-422 and RS 485 loading.



NOTES:
1. CDEO and DE/$\overline{RE}$ are at 2 V, BSR is at 0.8 V, and all others are open.
2. All nine drivers are enabled, simply loaded, and switching.

FIGURE 6. Driver test circuit, Pull up and pull down loading.

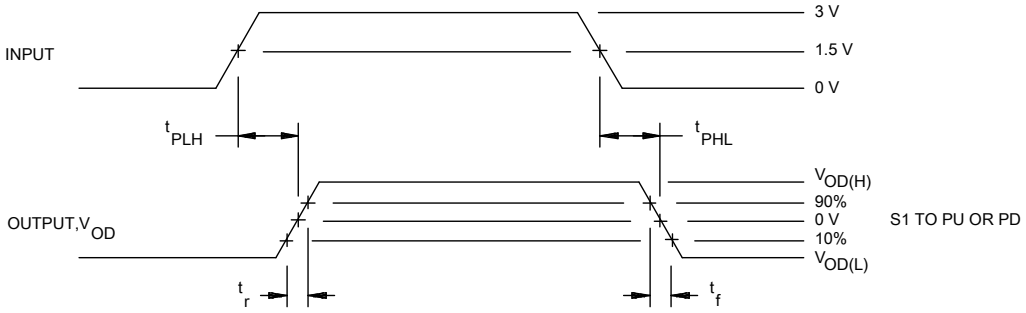
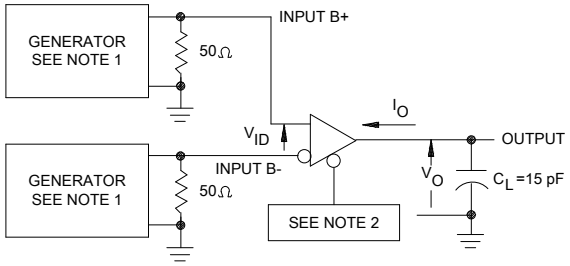
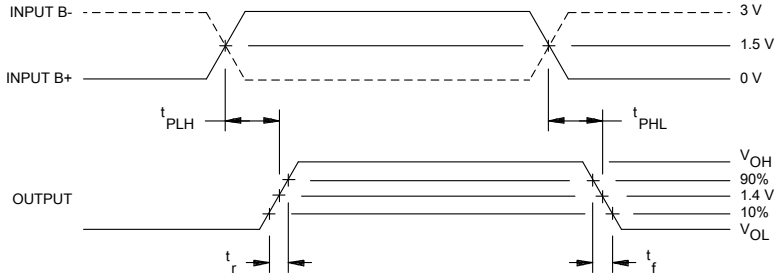


FIGURE 7. Driver delay and transition time test waveforms.



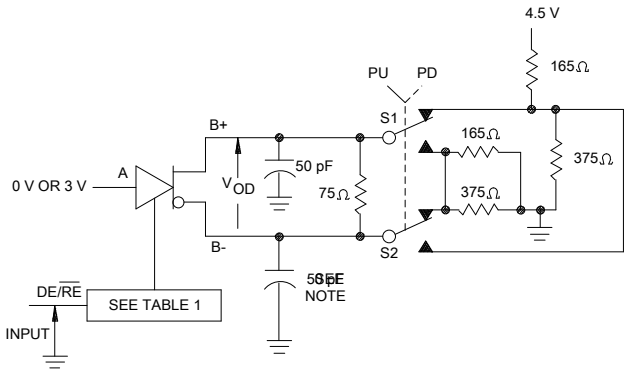
NOTES:
1. CDE0, CDE1, CDE2, BSR, CRE, and DE/$\overline{\text{RE}}$ are at 0.8 V.
2. All nine receivers are enabled and switching.

FIGURE 8. Receiver propagation delay and transition time test circuit.



NOTES:
1. All input pulses are supplied by a generator having the following characteristics: t_r ≤ 6 ns, t_f ≤ 6 ns, PRR ≤ 1 MHz, duty cycle = 50%, ZO = 50 Ω.
2. All resistances are in Ω and ±5%, unless otherwise indicated.
3. All capacitances are in pF and ±10%, unless otherwise indicated.
4. All indicated voltages are ±10 mV.

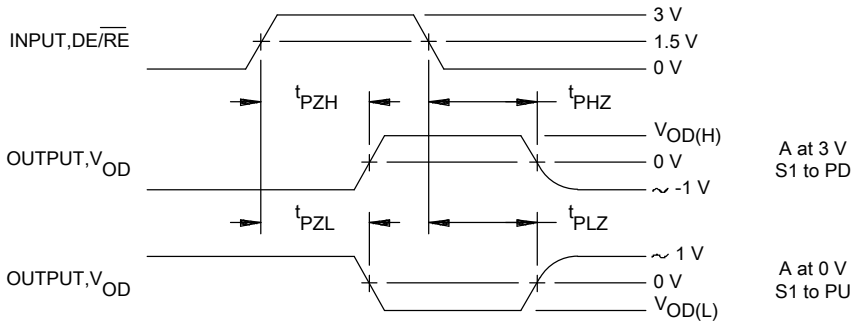
FIGURE 9. Receiver delay and transition time waveforms.



NOTE:
1. Includes probe and jig capacitance in two places.

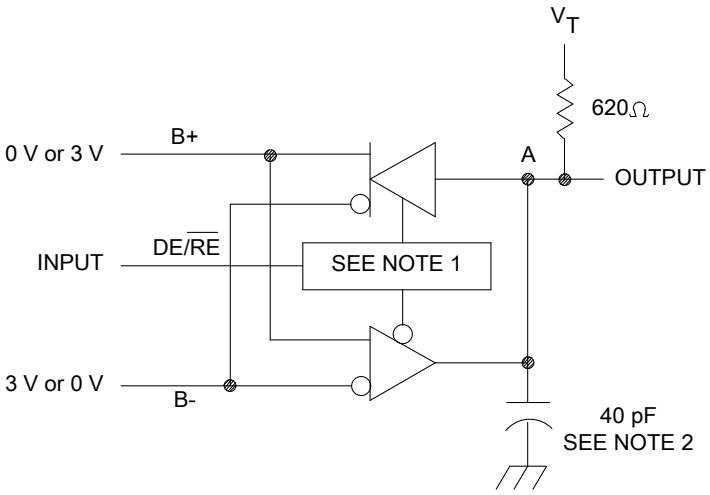
FIGURE 10. Driver enable and disable time test circuit.

Driver	BSR	CDE0	CDE1	CDE2	$\overline{CRE}$
1-8	H	H	L	L	X
9	L	H	H	H	H



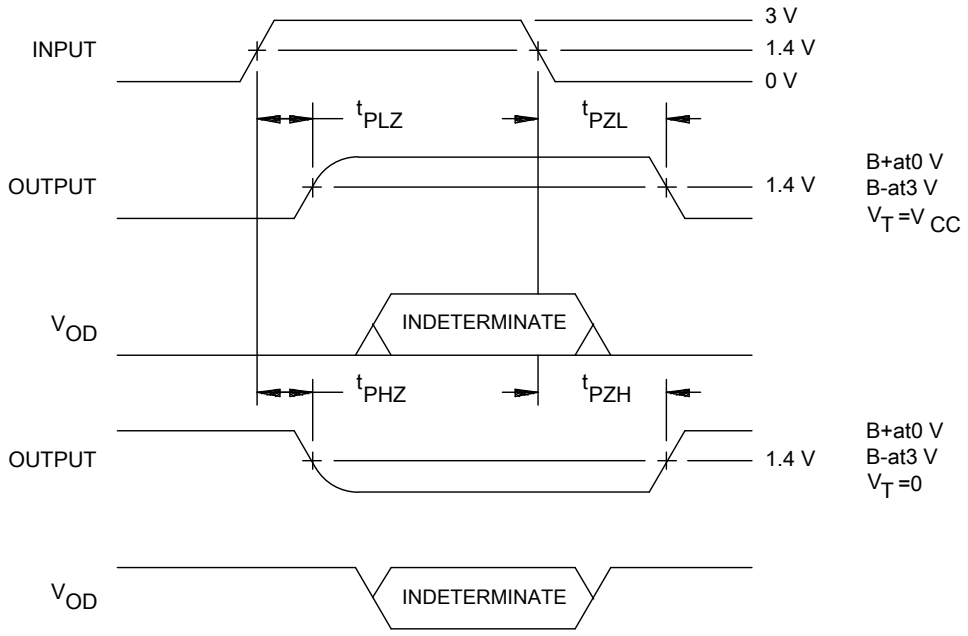
NOTES:
1. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, ZO = 50 Ω.
2. All resistances are in Ω and ±5%, unless otherwise indicated.
3. All capacitances are in pF and ±10%, unless otherwise indicated.
4. All indicated voltages are ±10 mV.

FIGURE 11. Driver enable time waveforms.



NOTES:
1. CDE0 is high, CDE1, CDE2, BSR, and $\overline{CRE}$ are low, all others are open.
2. Includes probe and jig capacitance.

FIGURE 12. Receiver enable and disable time test circuit.



NOTES:
1. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, ZO = 50 Ω.
2. All resistances are in Ω and ±5%, unless otherwise indicated.
3. All capacitances are in pF and ±10%, unless otherwise indicated.
4. All indicated voltages are ±10 mV.

FIGURE 13. Receiver enable and disable time waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/12607-01XE	01295	SN65HVD09IDGGREP	SN65HVD09EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243