| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPROVED |
| A | Correct Internal RAM supply voltage condition in Recommended operating conditions table. Correct data value on test No 12, sheet 19 and test No 8, sheet 22, in Table I. - phn | 14-11-25 | Thomas M. Hess |
| | | | |
| | | | |

Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **REV** | A | A | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | 84 | 85 | | | | | | | | | | | | | | | | | | | | |
| **REV** | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **PAGE** | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 |
| **REV** | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **PAGE** | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 |
| **REV** | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| **PAGE** | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 |
| **REV STATUS OF PAGES** | | | **REV** | | | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| | | | **PAGE** | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |

| | | |
|---|---|---|
| **PMIC N/A** | **PREPARED BY**<br>Phu H. Nguyen | **DLA LAND AND MARITIME**<br>**COLUMBUS, OHIO 43218-3990**<br>**http://www.landandmaritime.dla.mil/** |
| Original date of drawing<br>YY-MM-DD<br>13-08-13 | **CHECKED BY**<br>Phu H. Nguyen<br>**APPROVED BY**<br>Thomas M. Hess | **TITLE**<br>MICROCIRCUIT, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON |
| | **SIZE** **A** / **CODE IDENT. NO.** **16236** | **DWG NO.** **V62/12605** |
| | **REV** **A** | **PAGE** 1 **OF** 85 |

1.1 Scope. This drawing documents the general requirements of a high performance digital processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| V62/12605 | - | 01 | X | E |
|---|---|---|---|---|
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| Device type | Generic | Circuit function |
|---|---|---|
| 01 | OMAPL138B-EP | Digital signal processor |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| Outline letter | Number of pins | JEDEC PUB 95 | Package style |
|---|---|---|---|
| X | 361 | JEDEC MO-275 | Plastic ball grid array |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| Finish designator | Material |
|---|---|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

1.3 Absolute maximum ratings. 1/

Supply voltage range:
- Core logic, variable and fixed (CVDD, RVDD, RTC_CVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD) ..... -0.5 V to 1.4 V 2/
- I/O, 1.8 V (USB0_VDDA18, USB1_VDDA18, SATA_VDDR, DDR_DVDD18) ..... -0.5 V to 2.0 V 2/
- I/O, 3.3 V (DVDD3318_A, DVDD3318_B, DVDD3318_C, USB0_VDDA33, USB1_VDDA33) ..... -0.5 V to 3.8 V 2/

Input voltage ranges ($V_I$):
- Oscillator inputs (OSCIN, RTC_XI), 1.2 V ..... -0.3 V to $CV_{DD}$ + 0.3 V
- Dual voltage LVCMOS inputs 3.3 V or 1.8 V (steady state) ..... -0.3 V to $DV_{DD}$ + 0.3 V
- Dual voltage LVCMOS inputs, operated at 3.3 V (Transient) ..... $DV_{DD}$ + 20% up to 20% of signal period
- Dual voltage LVCMOS inputs, operated at 1.8 V (transient) ..... $DV_{DD}$ + 30% up to 30% of signal period
- USB 5V tolerant IOs: (USB0_DM, USB0_DP, USB0_ID, USB1_DM, USB1_DP) ..... 5.25 v 3/
- USB0 VBUS Pin ..... 5.50 V 3/

Output voltage ranges, ($V_O$):
- Dual voltage LVCMOS outputs, 3.3 V or 1.8 V (steady state) ..... -0.5 V to $DV_{DD}$ + 0.3 V
- Dual voltage LVCMOS outputs, operated at 3.3 V (Transient) ..... $DV_{DD}$ + 20% up to 20% of signal period
- Dual voltage LVCMOS outputs, operated at 1.8 V (Transient) ..... $DV_{DD}$ + 30% up to 30% of signal period

Clamp current,
- Input or output voltages 0.3 V above or below their respective power rails.
- Limits clamp current that flows through the I/O's internal diode protection cells..... ±20 mA

Operating Junction temperature ranges, ($T_J$) ..... -55°C to 125°C

Storage temperature range ($T_{STG}$) ..... -55°C to 150°C

ESD stress voltage, (VESD) 4/ :
- Human Body Level (HBL) 5/ ..... >1000 V
- Charged Device Model (CDM) 6/ ..... >500 V

---

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Alll voltage value with respect to VSS, USB0_VSSA33, USB_VSSA, PLL0_VSSA, OSCVSS, RTC_VSS.

3/ Up to maximum of 24 hours.

4/ Electronic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic dischargers into the device.

5/ Level listed above is the passing level per ANSI/JEDEC JS-001-2010. JEDEC document JEP 155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500 V HBM is possible if necessary precaution are taken. Pin listed as 1000 V may actually have higher performance.

6/ Level listed above is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP 155 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Pin listed as 250 V may actually have higher performance.

1.4 Recommended operating conditions. 7/

| | Name | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | CVDD | Core logic supply voltage (variable) | 1.3 V operating point | 1.25 | 1.35 | V |
| | | | 1.2 V operating point | 1.14 | 1.32 | |
| | | | 1.1 V operating point | 1.05 | 1.16 | |
| | | | 1.0 V operating point | 0.95 | 1.05 | |
| | RVDD | Internal RAM supply voltage | 345 MHz version | 1.14 | 1.32 | |
| | RTC_CVDD 8/ | RTC core logic supply voltage | | 0.9 | 1.32 | V |
| | PLL0_VDDA | PLL0 supply voltage | | 1.14 | 1.32 | |
| | PLL1_VDDA | PLL1 supply voltage | | 1.14 | 1.32 | |
| | SATA_VDD | SATA core logic supply voltage | | 1.14 | 1.32 | |
| | USB_CVDD | USB0, USB1 core logic supply voltage | | 1.14 | 1.32 | |
| | USB0_VDDA18 | USB0 PHY supply voltage | | 1.71 | 1.89 | |
| | USB0_VDDA33 | USB0 PHY supply voltage | | 3.15 | 3.45 | |
| | USB1_VDDA18 | USB1 PHY supply voltage | | 1.71 | 1.89 | |
| | USB1_VDDA33 | USB1 PHY supply voltage | | 3.15 | 3.45 | |
| | DVDD18 9/ | 1.8 V logic supply | | 1.71 | 1.89 | |
| | SATA_VDDR | SATA PHY internal regular supply voltage | | 1.71 | 1.89 | |
| | DDR_DVDD18 9/ | DDR2 PHY supply voltage | | 1.71 | 1.89 | |
| | DDR_VREF | DDR2/mDDR reference voltage | | 0.49* DDR_DVDD18 | 0.51* DDR_DVDD18 | |
| | DDR_ZP | DDR2/mDDR impedance control, connect via 50Ω resistor to $V_{SS}$ | | $V_{SS}$ TYP | | |
| | DVDD3318_A | Power group A dual voltage IO supply voltage | 1.8 V operating point | 1.71 | 1.89 | |
| | | | 3.3 V operating point | 3.15 | 3.45 | |
| | DVDD3318_B | Power group B dual voltage IO supply voltage | 1.8 V operating point | 1.71 | 1.89 | |
| | | | 3.3 V operating point | 3.15 | 3.45 | |
| | DVDD3318_C | Power group C dual voltage IO supply voltage | 1.8 V operating point | 1.71 | 1.89 | |
| | | | 3.3 V operating point | 3.15 | 3.45 | |
| Supply Ground | VSS | Core logic digital ground | | 0 | 0 | V |
| | PLL0_VSSA | PLL0 ground | | | | |
| | PLL1_VSSA | PLL1 ground | | | | |
| | SATA_VSS | SATA PHY ground | | | | |
| | OSCVSS 11/ | Oscillator ground | | | | |
| | RTC_VSS 11/ | RTC Oscillator ground | | | | |
| | USB0_VSSA | USB0 PHY ground | | | | |
| | USB0_VSSA33 | USB0 PHY ground | | | | |
| Voltage input high | VIH | High level input voltage, Dual voltage I/O 3.3 V 12/ | | 2 | | V |
| | | High level input voltage, Dual voltage I/O 1.8 V 12/ | | 0.65*DVDD | | |
| | | High level input voltage, RTC_XI | | 0.8*RTC_CVDD | | |
| | | High level input voltage, OSCIN | | 0.8*CVDD | | |

See foot note at end of table.

1.4 Recommended operating conditions - Continued. 7/

| | Name | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Voltage input low | VIL | Low level input voltage, Dual voltage I/O 3.3 V 12/ | | | 0.8 | V |
| | | Low level input voltage, Dual voltage I/O 1.8 V 12 | | | 0.35*DVDD | |
| | | Low level input voltage, RTC_XI | | | 0.2*RTC_CVDD | |
| | | Low level input voltage, OSCIN | | | 0.2*CVDD | |
| USB | USB0_VBUS | USB external charge pump input | | 0 | 5.25 | V |
| Differential Clock input Voltage | | Differential input voltage, SATA_REFCLKP and $\overline{\text{SATA_REFCLKN}}$ | | 250 | 2000 | mV |
| Transition time | $t_t$ | Transition time, 10%-90%, All inputs (unless otherwise specified in the electrical data section) | | | 0.25P or 10 13/ | ns |
| Operating frequency | $F_{PLL0_SYSCLK1,6}$ | Military temperature grade (M suffix) | CVDD = 1.2 V operating point | 0 | 345 14/ | MHz |

7/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
8/ The RTC provides an option for isolating the RTC_CVDD from the CVDD to reduce current leakage when the RTC is powered independently. If these power supply are not isolated (CTRL.SPLITPOWER =0), RTC_CVDD must be equal to or greater than CVDD.
9/ DVDD18 must be powered even if all of the DVDD3318_x supplies are operated at 3.3 V.
10/ DDR_DVDD18
11/ When an external crystal is used oscillator (OSC_VSS, RTC_VSS) ground must be kept separate from other grouns and connected directly to the crystal load capacitor ground. These pins are shorted to VSS on the device itself and should not be connected to VSS on the circuit board. If a crystal is not used and the clock input is driven directly, then the oscillator VSS may be connected to board ground.
12/ These IO specifications apply to the dual voltage IOs only and do not apply to DDR2/mDDR or SATA interfaces. DDR2/mDDR IOs are 1.8 V IOs and adhere to the JESD79-2A standard.
13/ Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.
14/ The operating point is 300 MHz on revision 1.x silicon.

1.4 Recommended operating conditions - Continued. 7/

Thermal resistance characteristics for case outline X:

| No. | | °C/W 15/ | Air Flow (m/s) 16/ |
|---|---|---|---|
| 1 | Junction to case, ($R\theta_{JC}$) | 7.3 | N/A |
| 2 | Junction to board, ($R\theta_{JB}$) | 12.4 | N/A |
| 3 | Junction to free air, ($R\theta_{JA}$) | 23.7 | 0.0 |
| 4 | Junction to moving air, ($R\theta_{JMA}$) | 21.0 | 0.5 |
| 5 | | 20.1 | 1.0 |
| 6 | | 19.3 | 2.0 |
| 7 | | 18.4 | 4.0 |
| 8 | Junction to package top, ($Psi_{JT}$) | 0.2 | 0.0 |
| 9 | | 0.3 | 0.5 |
| 10 | | 0.3 | 1.0 |
| 11 | | 0.4 | 2.0 |
| 12 | | 0.5 | 4.0 |
| 13 | Junction to board, ($Psi_{JB}$) | 12.3 | 0.0 |
| 14 | | 12.2 | 0.5 |
| 15 | | 12.1 | 1.0 |
| 16 | | 12.0 | 2.0 |
| 17 | | 11.9 | 4.0 |

1.5 Recommended Power On Hours (POH).

| **Silicon Revision** | **Speed Grade** | **Operating Junction Temperature ($T_J$)** | **Nominal CVDD voltage (V)** | **Power On Hour [POH] (hours)** |
|---|---|---|---|---|
| B | 345 MHz | 0 to 105°C | 1.2 V | 100,000 |
| B | 345 MHz | -55 to 125°C | 1.2 V | 29,145 |

15/ These measurements were conducted in s JEDEC defined as 2S2P system and will change based on environment as well as application. For more information see these EIA/JEDEC standards –JESD51-2 and JESD51-7. Power dissipation of 1 W and ambient temp of 70°C assumed. PCB with 2 oz (70 µm) top and bottom copper thickness and 1.5 oz (50 µm) inner copper thickness.

16/ m/s = meters per second.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

| | | |
|---|---|---|
| JEP95 | – | Registered and Standard Outlines for Semiconductor Devices |
| JEP 155 | – | Recommended ESD target levels for HBM/MM qualification |
| JESD51-2 | – | Integrated Circuits thermal test method environmental conditions – Natural convection (Still Air) |
| JESD51-7 | – | High Effective Thermal Conductivity Test Board for Leaded Surface Mount Package. |
| JESD22 | – | Electro Static Discharge (ESD) protection |
| JESD79-2A | – | DDR2 SDRAM standard |

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Test load circuit for AC timing measurements. The test load circuit for AC timing measurements shall be as shown in figure 4.

3.5.5 Input and Output voltage reference levels for AC timing measurements. The Input and Output voltage reference levels for AC timing measurements shall be as shown in figure 5.

3.5.6 Rise and Fall transaction time voltage reference levels. The Rise and Fall transaction time voltage reference levels shall be as shown in figure 6.

3.5.7 Power ON reset timing. The Power ON rest timing shall be as shown in figure 7.

3.5.8 Warm Reset timing. The Warm Reset timing shall be as shown in figure 8.

3.5.9 On chip oscillator. The on chip oscillator shall be as shown in figure 9

3.5.10 External 1.2 V clock source. The external 1.2 V clock source shall be as shown in figure 10.

3.5.11 EMIFA basic SDRAM Write operation. The EMIFA basic SDRAM Write operation shall be as shown in figure 11.

3.5.12 EMIFA basic SDRAM Read operation. The EMIFA basic SDRAM Read operation shall be as shown in figure 12.

3.5.13 Asynchronous Memory Read timing for EMIFA. The asynchronous Memory Read timing for EMIFA shall be as shown in figure 13.

3.5.14 Asynchronous Memory Write timing for EMIFA. The asynchronous Memory Write timing for EMIFA shall be as shown in figure 14.

3.5.15 EMA_WAIT Read timing requirements. The EMA_WAIT Read timing requirements shall be as shown in figure 15.

3.5.16 EMA_WAIT Write timing requirements. The EMA_WAIT Write timing requirements shall be as shown in figure 16.

3.5.17 MMC/SD Host command timing. The MMC/SD Host command timing shall be as shown in figure 17.

3.5.18 MMC/SD Card response timing. The MMC/SD Card response timing shall be as shown in figure 18.

3.5.19 MMC/SD Host Write timing. The MMC/SD Host Write timing shall be as shown in figure 19.

3.5.20 MMC/SD Host Read and Card Status timing. The MMC/SD Host Read and Card Status timing shall be as shown in figure 20.

3.5.21 McASP Block Diagram. The McASP Block Diagram shall be as shown in figure 21.

3.5.22 McASP Input timings. The McASP Input timings shall be as shown in figure 22.

3.5.23 McASP Output timings. The McASP Output timings shall be as shown in figure 23.

3.5.24 McBSP timings. The McBSP timings shall be as shown in figure 24.

3.5.25 FSR timing when GSYNC = 1. The FSR timing when GSYNC = 1 shall be as shown in figure 25

3.5.26 Block Diagram of SPI module. The Block Diagram of SPI module shall be as shown in figure 26.

3.5.27 SPI Timings – Master mode. The SPI Timings – Master mode shall be as shown in figure 27

3.5.28 SPI Timings – Slave mode. The SPI Timings – Slave mode shall be as shown in figure 28

3.5.29 SPI Timings – Master mode (4-Pin and 5-Pin). The SPI Timings – Master mode (4-Pin and 5-Pin) shall be as shown in figure 29

3.5.30 SPI Timings – Slave mode(4-Pin and 5-Pin). The SPI Timings – Slave mode (4-Pin and 5-Pin) shall be as shown in figure 30

3.5.31 I2C Receive timings. The I2C Receive timings shall be as shown in figure 31.

3.5.32 I2C Transmit timings. The I2C transmit timings shall be as shown in figure 32.

3.5.33 UART Transmit/Receive timing. The UART Transmit/Receive timing shall be as shown in figure 33.

3.5.34 USB2.0 Integrated Transceiver Interface timing. The USB2.0 Integrated Transceiver Interface timing shall be as shown in figure 34.

3.5.35 MII_RXCLK timing (EMAC – Receive). The MII_RXCLK timing (EMAC – Receive) shall be as shown in figure 35.

3.5.36 MII_TXCLK timing (EMAC – Transmit). The MII_TXCLK timing (EMAC – Transmit) shall be as shown in figure 35.

3.5.37 EMAC Receive Interface timing. The EMAC Receive Interface timing shall be as shown in figure 37.

3.5.38 EMAC Transmit Interface timing. The EMAC Transmit Interface timing shall be as shown in figure 38.

5.3.39 RMII Timing diagram. The RMII timing diagram shall be as shown in figure 39.

5.3.40 MDIO Input timing. The MDIO Input timing shall be as shown in figure 40

5.3.41 MDIO Output timing. The MDIO Output timing shall be as shown in figure 41

5.3.42 LCD Raster Mode display format. The LCD Raster Mode display format shall be as shown in figure 42

5.3.43 LCD Raster Mode active. The LCD Raster Mode active shall be as shown in figure 43

5.3.44 LCD Raster Mode Passive. The LCD Raster Mode passive shall be as shown in figure 44

5.3.45 LCD Raster Mode Control signal activation. The LCD Raster Mode Control signal activation shall be as shown in figure 45.

5.3.46 LCD Raster Mode Control signal deactivation. The LCD Raster Mode Control signal deactivation shall be as shown in figure 46.

5.3.47 UHPI Read timing ($\overline{\mathrm{HAS}}$ not used, Tied high). The UHPI Read timing ($\overline{\mathrm{HAS}}$ not used, Tied high) shall be as shown in figure 47.

5.3.48 UHPI Read timing ($\overline{\mathrm{HAS}}$ used). The UHPI Read timing ($\overline{\mathrm{HAS}}$ used) shall be as shown in figure 48.

5.3.49 UHPI Writed timing ($\overline{\mathrm{HAS}}$ not used, Tied high). The UHPI Write timing ($\overline{\mathrm{HAS}}$ not used, Tied high) shall be as shown in figure 49.

5.3.50 UHPI Write timing ($\overline{\mathrm{HAS}}$ used). The UHPI Write timing ($\overline{\mathrm{HAS}}$ used) shall be as shown in figure 50.

5.3.51 µPP Single Data Rate (SDR) receive timing. The µPP Single Data Rate (SDR) receive timing shall be as shown in figure 51.

5.3.52 µPP Double Data Rate (SDR) receive timing. The µPP Double Data Rate (DDR) receive timing shall be as shown in figure 52.

5.3.53 µPP Single Data Rate (SDR) transmit timing. The µPP Single Data Rate (SDR) transmit timing shall be as shown in figure 53.

5.3.54 µPP Double Data Rate (SDR) transmit timing. The µPP Double Data Rate (DDR) transmit timing shall be as shown in figure 54.

5.3.55 Video Port Capture VP_CLKINx timing. The Video Port Capture VP_CLKINx timing shall be as shown in figure 55.

5.3.56 VPIF channels 0/1 Video capture data and control input timing. The VPIF channels 0/1 Video capture data and control input timing shall be as shown in figure 56.

5.3.57 VPIF channels 2/3 Video Display Data Output timing with respect to VP_CLKOUT2/3. The VPIF channels 2/3 Video Display Data Output timing with respect to VP_CLKOUT2/3 shall be as shown in figure 57.

5.3.58 eCAP functional block diagram. The eCAP functional block diagram shall be as shown in figure 58

5.3.59 PWM Hi-Z characteristics. The PWM Hi-Z characteristics shall be as shown in figure 59.

5.3.60 Timer timing. The Timer timing shall be as shown in figure 60.

5.3.61 Timer timing. The Timer timing shall be as shown in figure 61.

5.3.62 GPIO port timing. The GPIO port timing shall be as shown in figure 62.

5.3.63 GPIO external interrupt timing. The GPIO external interrupt timing shall be as shown in figure 63.

5.3.64 JTAG test port timing. The JTAG test port timing shall be as shown in figure 64.

TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Test conditions 2/ | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| High level output voltage (Dual voltage LVCMOS IOs at 3.3 V) 3/ | $V_{OH}$ | DVDD = 3.15 V, $I_{OH}$ = -4 mA | 2.4 | | V |
| | | DVDD = 3.15 V, $I_{OH}$ = -100 µA | 2.95 | | |
| High level output voltage (Dual voltage LVCMOS IOs at 1.8 V) 3/ | | DVDD = 1.71 V, $I_{OH}$ = -2 mA | DVDD – 0.45 | | |
| Low level output voltage (Dual voltage LVCMOS IOs at 3.3 V) 3/ | $V_{OL}$ | DVDD = 3.15 V, $I_{OL}$ = 4 mA | | 0.4 | |
| | | DVDD = 3.15 V, $I_{OL}$ = 100 µA | | 0.2 | |
| Low level output voltage (Dual voltage LVCMOS IOs at 1.8 V) 3/ | | DVDD = 1.71 V, $I_{OL}$ = 2 mA | | 0.45 | |
| Input current 3/ (dual voltage LVCMOS I/Os) | $I_I$ 4/ | $V_I$ = VSS to DVDD without opposing internal resistor | | ±9 | µA |
| | | $V_I$ = VSS to DVDD with opposing internal pullup resistor 5/ | 70 | 310 | |
| | | $V_I$ = VSS to DVDD with opposing internal pulldown resistor 5/ | -75 | -270 | |
| Input current (DDR2/mDDR I/Os) | | $V_I$ = VSS to DVDD with opposing internal pulldown resistor 5/ | -77 | -286 | |
| High level output current 3/ (dual voltage LVCMOS I/Os) | $I_{OH}$ | | | -6 | mA |
| Low level output current 3/ (dual voltage LVCMOS I/Os) | $I_{OL}$ | | | 6 | |
| Input capacitance (dual voltage LVCMOS) | Capacitance | | 3 TYP | | pF |
| Output capacitance (dual voltage LVCMOS) | | | 3 TYP | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | Test conditions 2/ | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **Reset timings requirements** 6/ 7/ 8/ (See FIGURE 7 and 8) | | | | | | | | | | |
| 1 | Pulse width, $\overline{RESET}/\overline{TRST}$ low | $t_{w(RSTL)}$ | | 100 | | 100 | | 100 | | ns |
| 2 | Setup time, boot pins valid before , $\overline{RESET}/\overline{TRST}$ high | $t_{su(BPV-RSTH)}$ | | 20 | | 20 | | 20 | | |
| 3 | Hold time, boot pins valid after , $\overline{RESET}/\overline{TRST}$ high | $t_{h(RSTH-BPV)}$ | | 20 | | 20 | | 20 | | |
| 4 | $\overline{RESET}$ high to $\overline{RESETOUT}$ high; Warm reset | $t_{d(RSTH-RESETOUTH)}$ | | 4096 | | 4096 | | 4096 | | cycles 9/ |
| | $\overline{RESET}$ high to $\overline{RESETOUT}$ high; Power on reset | | | 6169 | | 6169 | | 6169 | | |
| 5 | Delay time, $\overline{RESET}/\overline{TRST}$ low to $\overline{RESETOUT}$ low | $t_{d(RSTL-RESETOUTL)}$ | | | 14 | | 16 | | 20 | ns |

| No. | Test | Symbol | Test conditions 2/ | Limits | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| **Oscillator timing requirements** 10/ (See FIGURE 9) | | | | | | |
| | Oscilltor frequency range (OSCIN/OSCOUT) | $f_{OSC}$ | | 12 | 30 | MHz |
| **OSCIN timing requirements for an externally driven clock** 11/ (see FIGURE 10) | | | | | | |
| | OSCIN frequency range | $f_{OSCIN}$ | | 12 | 50 | MHz |
| | Cycle time, external clock driven on OSCIN | $t_{c(OSCIN)}$ | | 20 | | ns |
| | Pulse width high, external clock on OSCIN | $t_{w(OSCINH)}$ | | 0.4 $t_{c(OSCIN)}$ | | |
| | Pulse width low, external clock on OSCIN | $t_{w(OSCINL)}$ | | 0.4 $t_{c(OSCIN)}$ | | |
| | Transition time, OSCIN | $t_{t(OSCIN)}$ | | | 0.25P or 10 11/ | |
| | Period jitter, OSCIN | $t_{j(OSCIN)}$ | | | 0.02P | |
| **Allowed PLL operating conditions (PLL0 and PLL1)** | | | | | | |
| 1 | PLLRST: Assertion time during initilization | | | 1000 | N/A | ns |
| 2 | Lock time 12/ | | | N/A | 13/ | OSCIN cycles |
| 3 | PREDIV: Pre-divider value | | | /1 | /32 | |
| 4 | PLLREF: PLL input frequency | | | 12 | 14/ | MHz |
| 5 | PLLM: PLL multiplier values | | | x4 | x32 | |
| 6 | PLLOUT: PLL output frequency | | | 300 | 600 | MHz |
| 7 | POSTDIV: Post divider value | | | /1 | /32 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | **EMIFA Electrical Data/Timing** | | | | | | | | |
| **Timing requirements for EMIFA SDRAM interface** (see FIGURE 11 and 12) | | | | | | | | | |
| 19 | Input setup time, read data valid on EMA_D[15:0] before EMA_CLK rising | $t_{su(EMA_DV-EM_CLKH)}$ | 2 | | 3 | | 3 | | ns |
| 20 | Input hold time, read data valid on EMA_D[15:0] after EMA_CLK rising | $t_{h(CLKH-DIV)}$ | 1.6 | | 1.6 | | 1.6 | | |
| **Switching characteristics for EMIFA SDRAM interface** (see FIGURE 11 and 12) | | | | | | | | | |
| 1 | Cycle time, EMIF clock EMA_CLK 15/ | $t_{c(CLK)}$ | 10 | | 15 | | 20 | | ns |
| 2 | Pulse width, EMIF clock EMA_CLK high or low 15/ | $t_{w(CLK)}$ | 3 | | 5 | | 8 | | |
| 3 | Delay time, EMA_CLK rising to $\overline{EMA_CS[0]}$ valid | $t_{d(CLKH-CSV)}$ | | 7 | | 9.5 | | 13 | |
| 4 | Output hold time, EMA_CLK rising to $\overline{EMA_CS[0]}$ invalid | $t_{oh(CLKH-CSIV)}$ | 1 | | 1 | | 1 | | |
| 5 | Delay time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] invalid | $t_{d(CLKH-DQMV)}$ | | 7 | | 9.5 | | 13 | |
| 6 | Output hold time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] invalid | $t_{oh(CLKH-DQMIV)}$ | 1 | | 1 | | 1 | | |
| 7 | Delay time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] invalid | $t_{d(CLKH-AV)}$ | | 7 | | 9.5 | | 13 | |
| 8 | Output hold time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] invalid | $t_{oh(CLKH-AIV)}$ | 1 | | 1 | | 1 | | |
| 9 | Delay time, EMA_CLK rising to EMA_D[15:0] valid | $t_{d(CLKH-DV)}$ | | 7 | | 9.5 | | 13 | |
| 10 | Output hold time, EMA_CLK rising to EMA_D[15:0] invalid | $t_{oh(CLKH-DIV)}$ | 1 | | 1 | | 1 | | |
| 11 | Delay time, EMA_CLK rising to $\overline{EMA_RAS}$ valid | $t_{d(CLKH-RASV)}$ | | 7 | | 9.5 | | 13 | |
| 12 | Output hold time, EMA_CLK rising to $\overline{EMA_RAS}$ invalid | $t_{oh(CLKH-RASIV)}$ | 1 | | 1 | | 1 | | |
| 13 | Delay time, EMA_CLK rising to $\overline{EMA_CAS}$ valid | $t_{d(CLKH-CASV)}$ | | 7 | | 9.5 | | 13 | |
| 14 | Output hold time, EMA_CLK rising to $\overline{EMA_CAS}$ invalid | $t_{oh(CLKH-CASIV)}$ | 1 | | 1 | | 1 | | |
| 15 | Delay time, EMA_CLK rising to $\overline{EMA_WE}$ valid | $t_{d(CLKH-WEV)}$ | | 7 | | 9.5 | | 13 | |
| 16 | Output hold time, EMA_CLK rising to $\overline{EMA_WE}$ valid | $t_{oh(CLKH-WEIV)}$ | 1 | | 1 | | 1 | | |
| 17 | Delay time, EMA_CLK rising to EMA_D[15:0] tri-stated 15/ | $t_{d(CLKH-DHZ)}$ | | 7 | | 9.5 | | 13 | |
| 18 | Output hold time, EMA_CLK rising to EMA_D[15:0] driving 15/ | $t_{oh(CLKH-DHIZ)}$ | 1 | | 1 | | 1 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | **Timing requirements for EMIFA asynchronous memory interface** 16/ | | | | | | | | |
| **READS and WRITERS** | | | | | | | | | |
| E | Cycle time, EMIFA module clock | $t_{c(CLK)}$ | 6.75 | | 15 | | 20 | | ns |
| 2 | Pulse duration, EM_WAIT assertion and deassertion | $t_{w(EM_WAIT)}$ | 2E | | 2E | | 2E | | |
| **READS** (see FIGURE 13) | | | | | | | | | |
| 12 | Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high | $t_{su(MDV_EMOEH)}$ | 3 | | 5 | | 7 | | ns |
| 13 | Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high | $t_{h(EMOEH_EMDIV)}$ | 0 | | 0 | | 0 | | |
| 14 | Setup time, EM_WAIT asserted before end of Strobe Phase 17/ | $t_{su(EMOEL_EMWAIT)}$ | 4E+3 | | 4E+3 | | 4E+3 | | |
| **WRITES** (see FIGURE 14-16) | | | | | | | | | |
| 28 | Setup time, EM_WAIT asserted before end of Strobe Phase 17 | $t_{su(EMWEL_EMWAIT)}$ | 4E+3 | | 4E+3 | | 4E+3 | | ns |

| No. | Test 2/ | Symbol | 1.3V, 1.2V, 1.1V, 1.0V | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| | **Switching characteristics for EMIFA asynchronous memory interface** 16/ 18/ 19/ | | | | |
| **READS and WRITES** | | | | | |
| 1 | Turn around time | $t_{d(TURNAROUND)}$ | (TA)*E-3 | (TA)*E+3 | ns |
| **READS** (see FIGURE 13) | | | | | |
| 3 | EMIF read cycle time (EW = 0) | $t_{c(EMRCYCLE)}$ | (RS+RST+RH)*E-3 | (RS+RST+RH)*E+3 | ns |
| | EMIF read cycle time (EW = 1) | | (RS+RST+RH+ (EWC*16))*E-3 | (RS+RST+RH+ (EWC*16))*E+3 | |
| 4 | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS=0) | $t_{su(EMCEL-EMOEL)}$ | (RS)*E-3 | (RS)*E+3 | |
| | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS=1) | | -3 | +3 | |
| 5 | Output hold time $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS=0) | $t_{h(EMOEH-EMCEH)}$ | (RH)*E-3 | (RH)*E+3 | |
| | Output hold time $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS=1) | | -3 | +3 | |
| 6 | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_OE}$ low | $t_{su(EMBAV-EMEOL)}$ | (RS)*E-3 | (RS)*E+3 | |
| 7 | Output hold time $\overline{EMA_OE}$ high to $\overline{EMA_BA[1:0]}$ invalid | $t_{h(EMEOH-EMBAIV)}$ | (RH)*E-3 | (RH)*E+3 | |
| 8 | Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_OE}$ low | $t_{su(EMBAV-EMOEL)}$ | (RS)*E-3 | (RS)*E+3 | |
| 9 | Output hold time $\overline{EMA_OE}$ high to $\overline{EMA_A[13:0]}$ invalid | $t_{h(EMEOH-EMAIV)}$ | (RH)*E-3 | (RH)*E+3 | |
| 10 | $\overline{EMA_OE}$ active low width (EW=0) | $t_{w(EMOEL)}$ | (RST)*E-3 | (RST)*E+3 | |
| | $\overline{EMA_OE}$ active low width (EW=1) | | (RST+(EWC*16)) *E-3 | (RST+(EWC*16)) *E+3 | |
| 11 | Delay time from EMA_WAIT deasserted to $\overline{EMA_OE}$ high | $t_{d(EMWAITH-EMOEH)}$ | 3E - 3 | 4E+3 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V, 1.1V, 1.0V | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| | **Switching characteristics for EMIFA asynchronous memory interface - Continued** 16/ 18/ 19/ | | | | |
| **WRITES** (see FIGURE 14-16) | | | | | |
| 15 | EMIF write cycle time (EW = 0) | $t_{c(EMWCYCLE)}$ | (WS+WST+WH)*E-3 | (WS+WST+WH)*E+3 | ns |
| | EMIF write cycle time (EW = 1) | | (WS+WST+WH+ (EWC*16))*E-3 | (WS+WST+WH+ (EWC*16))*E+3 | |
| 16 | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS=0) | $t_{su(EMCEL-EMWEL)}$ | (WS)*E-3 | (WS)*E+3 | |
| | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS=1) | | -3 | +3 | |
| 17 | Output hold time $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS=0) | $t_{h(EMWEH-EMCEH)}$ | (WH)*E-3 | (WH)*E+3 | |
| | Output hold time $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS=1) | | -3 | +3 | |
| 18 | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low | $t_{su(EMDQMV-EMWEL)}$ | (WS)*E-3 | (WS)*E+3 | |
| 19 | Output hold time $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid | $t_{h(EMWEH-EMDQMIV)}$ | (WH)*E-3 | (WH)*E+3 | |
| 20 | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low | $t_{su(EMBAV-EMWEL)}$ | (WS)*E-3 | (WS)*E+3 | |
| 21 | Output hold time $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid | $t_{h(EMEWEH-EMBAIV)}$ | (WH)*E-3 | (WH)*E+3 | |
| 22 | Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_WE}$ low | $t_{su(EMAV-EMWEL)}$ | (WS)*E-3 | (WS)*E+3 | |
| 23 | Output hold time $\overline{EMA_WE}$ high to $\overline{EMA_A[13:0]}$ invalid | $t_{H(EMWEH-EMAIV)}$ | (WH)*E-3 | (WH)*E+3 | |
| 24 | $\overline{EMA_WE}$ active low width (EW=0) | $t_{w(EMWEL)}$ | (WST)*E-3 | (WST)*E+3 | |
| | $\overline{EMA_WE}$ active low width (EW=1) | | (WST+(EWC*16)) *E-3 | (WST+(EWC*16)) *E+3 | |
| 25 | Delay time from EMA_WAIT deasserted to $\overline{EMA_WE}$ high | $t_{d(EMWAITH-EMOEH)}$ | 3E-3 | 4E+3 | |
| 26 | Output setup time, $\overline{EMA_D[15:0]}$ valid to $\overline{EMA_WE}$ low | $t_{su(EMDV-EMWEL)}$ | (WS)*E-3 | (WS)*E+3 | |
| 27 | Output hold time $\overline{EMA_WE}$ high to $\overline{EMA_D[15:0]}$ invalid | $t_{h(EMEWEH-EMDIV)}$ | (WH)*E-3 | (WH)*E+3 | |

| No. | Test | Symbol | Test conditions 2/ | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **Switching characteristics for DDR2/mDDR memory controller** | | | | | | | | | | |
| 1 | Cycle time, DDR_CLKP, DDR_CLKN | $t_{c(DDR_CLK)}$ | DDR2 | 125 | 156 | 125 | 150 | 20/ | 20/ | MHz |
| | | | mDDR | 105 | 150 | 100 | 133 | 95 | 133 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | **MMC/SD Electrical Data/Timing** | | | | | | | | |
| **Timing requirements for MMC/SD** | (see FIGURE 18 to 20) | | | | | | | | |
| 1 | Setup time, MMCSD_CMD valid before MMCSD_CLK high | $t_{su(CMDV-CLKH)}$ | 4 | | 4 | | 6 | | ns |
| 2 | Hold time, MMCSD_CMD valid after MMCSD_CLK high | $t_{h(CLKH-CMDV)}$ | 2.5 | | 2.5 | | 2.5 | | |
| 3 | Setup time, MMCSD_DATx valid before MMCSD_CLK high | $t_{su(DATV-CLKH)}$ | 4.5 | | 5 | | 6 | | |
| 4 | Hold time, MMCSD_DATx valid after MMCSD_CLK high | $t_{h(CLKH-DATV)}$ | 2.5 | | 2.5 | | 2.5 | | |
| **Switching characteristics for MMC/SD** | (see FIGURE 17 to 20)) | | | | | | | | |
| 7 | Operating frequency, MMCSD_CLK | $f_{(CLK)}$ | 0 | 52 | 0 | 50 | 0 | 25 | MHz |
| 8 | Identification mode frequency, MMCSD_CLK | $f_{(CLK_ID)}$ | 0 | 400 | 0 | 400 | 0 | 400 | KHz |
| 9 | Pulse width, MMCSD_CLK low | $t_{w(CLKL)}$ | 6.5 | | 6.5 | | 10 | | ns |
| 10 | Pulse width, MMCSD_CLK high | $t_{w(CLKH)}$ | 6.5 | | 6.5 | | 10 | | |
| 11 | Rise time, MMCSD_CLK | $t_{r(CLK)}$ | | 3 | | 3 | | 10 | |
| 12 | Fall time, MMCSD_CLK | $t_{f(CLK)}$ | | 3 | | 3 | | 10 | |
| 13 | Delay time, MMCSD low to MMCSD_CMD transaction | $t_{d(CLKL-CMD)}$ | -4 | 2.5 | -4 | 3 | -4 | 4 | |
| 14 | Delay time, MMCSD low to MMCSD_DATx transaction | $t_{d(CLKL-DAT)}$ | -4 | 3.3 | -4 | 3.5 | -4 | 4 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| | **McASP Electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for McASP0** 21/ 22/ (see FIGURE 22 to 23) | | | | | | | | | | |
| 1 | Cycle time, AHCLKR/X | | $t_{c(AHCLKRX)}$ 23/ | 25 | | 28 | | 35 | | ns |
| 2 | Pulse duration, AHCLK/X high or low | | $t_{w(AHCLKRX)}$ 23/ | 12.5 | | 14 | | 17.5 | | |
| 3 | Cycle time, AHCLKR/X | AHCLKR/X ext | $t_{c(ACLKRX)}$ 23/ | 25 24/ | | 28 24/ | | 35 24/ | | |
| 4 | Pulse duration, AHCLK/X high or low | AHCLKR/X ext | $t_{w(ACLKRX)}$ 23/ | 12.5 | | 14 | | 17.5 | | |
| 5 | Setup time, AFSR/X input to ACLKR/X 25/ | AHCLKR/X int | $t_{su(AFSRX-ACLKRX)}$ 23/ | 11.5 | | 12 | | 16 | | |
| | | AHCLKR/X ext input | | 4 | | 5 | | 5.5 | | |
| | | AHCLKR/X ext output | | 4 | | 5 | | 5.5 | | |
| 6 | Hold time, AFSR/X input after ACLKR/X 25/ | AHCLKR/X int | $t_{h(ACLKRX-AFSRX)}$ | -1 | | -2 | | -2 | | |
| | | AHCLKR/X ext input | | 1 | | 1 | | 1 | | |
| | | AHCLKR/X ext output | | 1 | | 1 | | 1 | | |
| 7 | Setup time, AXR0[n] input to ACLKR/X 25/ *26/* | AHCLKR/X int | $t_{su(AXR-ACLKRX)}$ 23/ | 11.5 | | 12 | | 16 | | |
| | | AHCLKR/X ext input | | 4 | | 5 | | 5.5 | | |
| 8 | Hold time, AXR0[n] input after ACLKR/X 25/ *26/* | AHCLKR/X ext | $t_{h(ACLKRX-AXR)}$ | -1 | | -2 | | -2 | | |
| | | AHCLKR/X ext input | | 3 | | 4 | | 5 | | |
| | | AHCLKR/X ext output | | 3 | | 4 | | 5 | | |
| **Switching characteristics for McASP0** 27/ (see FIGURE 22 to 23) | | | | | | | | | | |
| 9 | Cycle time, AHCLKR/X | | $t_{c(AHCLKRX)}$ 23/ | 25 | | 28 | | 35 | | ns |
| 10 | Pulse duration, AHCLK/X high or low | | $t_{w(AHCLKRX)}$ 23/ | AH-2.5 28/ | | AH-2.5 28/ | | AH-2.5 28/ | | |
| 11 | Cycle time, AHCLKR/X | AHCLKR/X int | $t_{c(ACLKRX)}$ 23/ | 25 22/ 24/ | | 28 22/ 24/ | | 35 22/ 24/ | | |
| 12 | Pulse duration, AHCLK/X high or low | AHCLKR/X int | $t_{w(ACLKRX)}$ 23/ | A-2.5 29/ | | A-2.5 29/ | | A-2.5 29/ | | |
| 13 | Delay time, ACLKR/X transmit edge to AFSX/R output valid 25/ | AHCLKR/X int | $t_{d(ACLKRX-AFSRX)}$ | -1 | 6 | -1 | 8 | -0.5 | 10 | |
| | | AHCLKR/X ext input | | 2 | 13.5 | 2 | 14.5 | 2 | 19 | |
| | | AHCLKR/X ext output | | 2 | 13.5 | 2 | 14.5 | 2 | 19 | |
| 14 | Delay time, ACLKX transmit edge to AXR output valid | AHCLKR/X int | $t_{d(ACLKX-AXRV)}$ | -1 | 6 | -1 | 8 | -0.5 | 10 | |
| | | AHCLKR/X ext input | | 2 | 13.5 | 2 | 15 | 2 | 19 | |
| | | AHCLKR/X ext output | | 2 | 13.5 | 2 | 15 | 2 | 19 | |
| 15 | Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit | AHCLKR/X int | $t_{dis(ACLKX-AXrhz)}$ 23/ | 0 | 6 | 0 | 8 | 0 | 10 | |
| | | AHCLKR/X ext | | 2 | 13.5 | 2 | 15 | 2 | 19 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| | **McBSP Electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for McBSP0** 30/ (see FIGURE 24) | | | | | | | | | | |
| 2 | Cycle time, CLKR/X | CLKR/X ext | $t_{c(CKRX)}$ 23/ | 2P or 20 31/ 32/ | | 2P or 20 31/ 32/ | | 2P or 26.6 31/ 32/ | | ns |
| 3 | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | $t_{w(CKRX)}$ 23/ | P-1 33/ | | P-1 33/ | | P-1 33/ | | |
| 5 | Setup time, external FSR high before CLKR low | CLKR int | $t_{su(FRH-CKRL)}$ | 14 | | 15.5 | | 20 | | |
| | | CLKR ext | | 4 | | 5 | | 5 | | |
| 6 | Hold time, external FSR high after CLKR low | CLKR int | $t_{h(CKRL-FRH)}$ 23/ | 6 | | 6 | | 6 | | |
| | | CLKR ext | | 3 | | 3 | | 3 | | |
| 7 | Setup time, DR valid before CLKR low | CLKR int | $t_{su(DRV-CKRL)}$ | 14 | | 15.5 | | 20 | | |
| | | CLKR ext | | 4 | | 5 | | 5 | | |
| 8 | Hold time, DR valid after CLKR low | CLKR int | $t_{h(CKRL-DRV)}$ 23/ | 3 | | 3 | | 3 | | |
| | | CLKR ext | | 3 | | 3 | | 3 | | |
| 10 | Setup time, external FSR high before CLKX low | CLKR int | $t_{su(FXH-CKXL)}$ | 14 | | 15.5 | | 20 | | |
| | | CLKR ext | | 4 | | 5 | | 5 | | |
| 11 | Hold time, external FSR high after CLKX low | CLKR int | $t_{h(CKXL-FXH)}$ | 6 | | 6 | | 6 | | |
| | | CLKR ext | | 3 | | 3 | | 3 | | |
| **Switching characteristics for McBSP0** 30/ 34/ (See FIGURE 24) | | | | | | | | | | |
| 1 | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | $t_{d(CKSH-CKRXH)}$ | 2 | 14.5 | 2 | 16 | 3 | 21.5 | |
| 2 | Cycle time, CLKR/X | CLKR/X int | $t_{c(CKRX)}$ 23/ | 2P or 20 31/ 32/ | | 2P or 20 31/ 32/ | | 2P or 26.6 31/ 32/ | | |
| 3 | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | $t_{w(CKRX)}$ 23/ | C-2 37/ | C+2 37/ | C-2 37/ | C+2 37/ | C-2 37/ | C+2 37/ | |
| 4 | Delay time, CLKR high to internal FSR valid | CLKR int | $t_{d(CKRH-FRV)}$ | -4 | 5.5 | -4 | 5.5 | -4 | 10 | |
| | | CLKR ext | | 2 | 14.5 | 2 | 16 | 2.5 | 21.5 | |
| 9 | Delay time, CLKX high to internal FSX valid | CLKR int | $t_{d(CKXH-FXV)}$ 23/ | -4 | 5.5 | -4 | 5.5 | -4 | 10 | |
| | | CLKR ext | | 2 | 14.5 | 2 | 16 | 2.5 | 21.5 | |
| 12 | Disable time, DX high impedance following last data bit from CLKX high | CLKR int | $t_{dis(CKXH-DXHZ)}$ 23/ | -4 | 7.5 | -5.5 | 7.5 | -4 | 10 | |
| | | CLKR ext | | -2 | 16 | -22 | 16 | -2 | 21.5 | |
| 13 | Delay time, CLKX high to DX valid | CLKR int | $t_{d(CKXH-DXV)}$ 23/ | -4+D1 38/ | 5.5+D2 38/ | -4+D1 38/ | 5.5+D2 38/ | -4+D1 38/ | 10+D2 38/ | |
| | | CLKR ext | | 2+D1 38/ | 14.5+D2 38/ | 2+D1 38/ | 16+D2 38/ | 2.5+D1 38/ | 21.5+D2 38/ | |
| 14 | Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode | CLKR int | $t_{d(FXH-DXV)}$ 23/ | -4 39/ | 5 39/ | -4 39/ | 5 39/ | -4 39/ | 5 39/ | |
| | | CLKR ext | | -2 39/ | 14.5 39/ | -2 39/ | 16 39/ | -2 39/ | 21.5 39/ | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **McBSP Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Timing requirements for McBSP1** 30/ (See FIGURE 24) | | | | | | | | | | |
| 2 | Cycle time, CLKR/X | CLKR/X ext | $t_{c(CKRX)}$ 23/ | 2P or 20 31/ 32/ | | 2P or 25 31/ 32/ | | 2P or 26.6 31/ 32/ | | ns |
| 3 | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | $t_{w(CKRX)}$ 23/ | P-1 33/ | | P-1 33/ | | P-1 33/ | | |
| 5 | Setup time, external FSR high before CLKR low | CLKR int | $t_{su(FRH-CKRL)}$ | 15 | | 18 | | 21 | | |
| | | CLKR ext | | 5 | | 5 | | 10 | | |
| 6 | Hold time, external FSR high after CLKR low | CLKR int | $t_{h(CKRL-FRH)}$ 23/ | 6 | | 6 | | 6 | | |
| | | CLKR ext | | 3 | | 3 | | 3 | | |
| 7 | Setup time, DR valid before CLKR low | CLKR int | $t_{su(DRV-CKRL)}$ | 15 | | 18 | | 21 | | |
| | | CLKR ext | | 5 | | 5 | | 10 | | |
| 8 | Hold time, DR valid after CLKR low | CLKR int | $t_{h(CKRL-DRV)}$ | 3 | | 3 | | 3 | | |
| | | CLKR ext | | 3 | | 3 | | 3 | | |
| 10 | Setup time, external FSR high before CLKX low | CLKR int | $t_{su(FXH-CKXL)}$ | 15 | | 18 | | 21 | | |
| | | CLKR ext | | 5 | | 5 | | 10 | | |
| 11 | Hold time, external FSR high after CLKX low | CLKR int | $t_{h(CKXL-FXH)}$ 23/ | 6 | | 6 | | 6 | | |
| | | CLKR ext | | 3 | | 3 | | 3 | | |
| **Switching characteristics for McBSP1** 30/ 34/ (see FIGURE 24) | | | | | | | | | | |
| 1 | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | $t_{d(CKSH-CKRXH)}$ | 0.5 | 16.5 | 1.5 | 18 | 1.5 | 23 | ns |
| 2 | Cycle time, CLKR/X | CLKR/X int | $t_{c(CKRX)}$ 23/ | 2P or 20 31/ 32/ | | 2P or 25 31/ 32/ | | 2P or 26.6 31/ 32/ | | |
| 3 | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | $t_{w(CKRX)}$ 23/ | C-2 37/ | C+2 37/ | C-2 37/ | C+2 37/ | C-2 37/ | C+2 37/ | |
| 4 | Delay time, CLKR high to internal FSR valid | CLKR int | $t_{d(CKRH-FRV)}$ | -4 | 6.5 | -4 | 13 | -4 | 13 | |
| | | CLKR ext | | 1 | 16.5 | 1 | 18 | 2.5 | 23 | |
| 9 | Delay time, CLKX high to internal FSX valid | CLKR int | $t_{d(CKXH-FXV)}$ 23/ | -4 | 6.5 | -4 | 13 | -4 | 13 | |
| | | CLKR ext | | 1 | 16.5 | 1 | 18 | 1 | 23 | |
| 12 | Disable time, DX high impedance following last data bit from CLKX high | CLKR int | $t_{dis(CKXH-DXHZ)}$ 23/ | -4 | 6.5 | -4 | 13 | -4 | 13 | |
| | | CLKR ext | | -2 | 16.5 | -2 | 18 | -2 | 23 | |
| 13 | Delay time, CLKX high to DX valid | CLKR int | $t_{d(CKXH-DXV)}$ 23/ | -4+D1 38/ | 6.5+D2 38/ | -4+D1 38/ | 13+D2 38/ | -4+D1 38/ | 13+D2 38/ | |
| | | CLKR ext | | 1+D1 38/ | 16.5+D2 38/ | 1+D1 38/ | 18+D2 38/ | 1+D1 38/ | 23+D2 38/ | |
| 14 | Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode | CLKR int | $t_{d(FXH-DXV)}$ 23/ | -4 39/ | 6.5 39/ | -4 39/ | 13 39/ | -4 39/ | 13 39/ | |
| | | CLKR ext | | -2 39/ | 16.5 39/ | -2 39/ | 18 39/ | -2 39/ | 23 39/ | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| **McBSP Electrical Data/Timing – Continued.** | | | | | | | | | |
| **Timing requirements for McBSP0 FSR when GSYNC = 1** 97/ (See FIGURE 25) | | | | | | | | | |
| 1 | Setup time, FSR high before CLKS high | $t_{su(FRH-CKSH)}$ | 4 | | 4.5 | | 5 | | ns |
| 2 | Hold time, FSR high after CLKS high | $t_{h(CKSH-FRH)}$ | 4 | | 4 | | 4 | | |
| **Timing requirements for McBSP1 FSR when GSYNC = 1** 97/ (See FIGURE 25) | | | | | | | | | |
| 1 | Setup time, FSR high before CLKS high | $t_{su(FRH-CKSH)}$ | 5 | | 5 | | 10 | | ns |
| 2 | Hold time, FSR high after CLKS high | $t_{h(CKSH-FRH)}$ | 4 | | 4 | | 4 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing** | | | | | | | | | | |
| **General timing requirements for SPI0 Master modes** 23/ 40/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 1 | Cycle time, SPI0_CLK, All master modes | | $t_{c(SPC)M}$ | 20 41/ | 256P | 30 41/ | 256P | 40 41/ | 256P | ns |
| 2 | Pulse width high, SPI0_CLK, All master modes | | $t_{w(SPCH)M}$ | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | |
| 3 | Pulse width low, SPI0_CLK, All master modes | | $t_{w(SPCL)M}$ | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | |
| 4 | Delay initial data bit valid on SPI0_SIMO after initial edge on SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(SIMO_SPC)M}$ | | 5 | | 5 | | 6 | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | | -0.5M +5 | | -0.5M +5 | | -0.5M +6 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | | 5 | | 5 | | 6 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | | -0.5M +5 | | -0.5M +5 | | -0.5M +6 | |
| 5 | Delay subsequent bits valid on SPI0_SIMO after transmit edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(SPC_SIMO)M}$ | | 5 | | 5 | | 6 | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | | 5 | | 5 | | 6 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | | 5 | | 5 | | 6 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | | 5 | | 5 | | 6 | |
| 6 | Output hold time, SPI0_SIMO valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{oh(SPC_SIMO)M}$ | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| 7 | Input setup time, SPI0_SOMI valid before receive edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{su(SOMI_SPC)M}$ | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 1.5 | | 1.5 | | 1.5 | | |
| 8 | Input hold time, SPI0_SOMI valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{ih(SPC_SOMI)M}$ | 4 | | 4 | | 5 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 4 | | 4 | | 5 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 4 | | 4 | | 5 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 4 | | 4 | | 5 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **General timing requirements for SPI0 Slave modes** 43/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 9 | Cycle time, SPI0_CLK, All slave modes | | $t_{c(SPC)S}$ 23/ | 40 41/ | | 50 41/ | | 60 41/ | | ns |
| 10 | Pulse width high, SPI0_CLK, All slave modes | | $t_{w(SPCH)S}$ 23/ | 18 | | 22 | | 27 | | |
| 11 | Pulse width low, SPI0_CLK, All slave modes | | $t_{w(SPCL)S}$ 23/ | 18 | | 22 | | 27 | | |
| 12 | Setup time, transmit data written to SPI before initial clock edge from master 44/ 45/ | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{su(SOMI_SPC)S}$ 23/ | 2P | | 2P | | 2P | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 2P | | 2P | | 2P | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | 2P | | 2P | | 2P | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 2P | | 2P | | 2P | | |
| 13 | Delay subsequent bits valid on SPI0_SOMI after transmit edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(SPC_SOMI)S}$ | | 17 | | 20 | | 27 | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | | 17 | | 20 | | 27 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | | 17 | | 20 | | 27 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | | 17 | | 20 | | 27 | |
| 14 | Output hold time, SPI0_SOMI valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{oh(SPC_SOMI)S}$ 23/ | 0.5S -6 | | 0.5S -16 | | 0.5S -20 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 0.5S -6 | | 0.5S -16 | | 0.5S -20 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 0.5S -6 | | 0.5S -16 | | 0.5S -20 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 0.5S -6 | | 0.5S -16 | | 0.5S -20 | | |
| 15 | Input setup time, SPI0_SIMO valid before receive edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{su(SIMO_SPC)S}$ | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 1.5 | | 1.5 | | 1.5 | | |
| 16 | Input hold time, SPI0_SIMO valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{ih(SPC_SIMO)S}$ 23/ | 4 | | 4 | | 5 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 4 | | 4 | | 5 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 4 | | 4 | | 5 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 4 | | 4 | | 5 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI0 master timings, 4-Pin enable option** 40/ 47/ 56/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 17 | Delay from slave assertion of $\overline{\text{SPI0_ENA}}$ active to first SPI1_CLK from master 48/ | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(ENA_SPC)M}$ | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | | 0.5M+ 3P+5 | | 0.5M+ 3P+5 | | 0.5M+ 3P+6 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | | 0.5M+ 3P+5 | | 0.5M+ 3P+5 | | 0.5M+ 3P+6 | |
| 18 | Max delay for slave to deassert $\overline{\text{SPI0_ENA}}$ after final SPI0_CLK edge to ensure master does not begin the next transfer. 49/ | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SPC_ENA)M}$ | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | | P+5 | | P+5 | | P+6 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | | P+5 | | P+5 | | P+6 | |
| **Additional SPI0 master timings, 4-Pin chip select option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 19 | Delay from $\overline{\text{SPI0_SCS}}$ active to first SPI0_CLK 50/ 51/ | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(SCS_SPC)M}$ | 2P-1 | | 2P-2 | | 2P-3 | | ns |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 0.5M +2P-1 | | 0.5M +2P-2 | | 0.5M +2P-3 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | 2P-1 | | 2P-2 | | 2P-3 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 0.5M +2P-1 | | 0.5M +2P-2 | | 0.5M +2P-3 | | |
| 20 | Delay from final SPI0_CLK edge to master deasserting $\overline{\text{SPI0_SCS}}$. 51/ 52/ | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SPC_SCS)M}$ | 0.5M +P-1 | | 0.5M +P-2 | | 0.5M +P-3 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | P-1 | | P-2 | | P-3 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 0.5M +P-1 | | 0.5M +P-2 | | 0.5M +P-3 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | P-1 | | P-2 | | P-3 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI0 master timings, 5-Pin option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 18 | Max delay for slave to deassert $\overline{\text{SPI0_ENA}}$ after final SPI0_CLK edge to ensure master does not begin the next transfer. 49/ | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SPC_ENA)M}$ | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | ns |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | | P+5 | | P+5 | | P+6 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | | P+5 | | P+5 | | P+6 | |
| 20 | Delay from final SPI0_CLK edge to master deasserting $\overline{\text{SPI0_SCS}}$. 52/ 62/ | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SPC_SCS)M}$ | 0.5M+ P-2 | | 0.5M+ P-2 | | 0.5M+ P-3 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | P-2 | | P-2 | | P-3 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 0.5M+ P-2 | | 0.5M+ P-2 | | 0.5M+ P-3 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | P-2 | | P-2 | | P-3 | | |
| 21 | Max delay for slave SPI to drive $\overline{\text{SPI0_ENA}}$ valid after master asserts $\overline{\text{SPI0_SCS}}$ to delay the master from beginning the next transfer. | | $t_{d(SCSL_ENAL)M}$ | | 55/ | | 55/ | | 55/ | |
| 22 | Delay from $\overline{\text{SPI0_SCS}}$ active to first SPI0_CLK 50/ 53/ 62/ | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(SCS_SPC)M}$ | 2P-2 | | 2P-2 | | 2P-3 | | ns |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | 0.5M +2P-2 | | 0.5M +2P-2 | | 0.5M +2P-3 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | 2P-2 | | 2P-2 | | 2P-3 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | 0.5M +2P-2 | | 0.5M +2P-2 | | 0.5M +2P-3 | | |
| 23 | Delay from assertion $\overline{\text{SPI0_ENA}}$ low to first SPI0_CLK edge. 54/ | Polarity = 0, Phase = 0 to SPI0_CLK rising | $t_{d(ENA_SPC)M}$ | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK rising | | | 0.5M +3P+5 | | 0.5M +3P+5 | | 0.5M +3P+6 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK falling | | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK falling | | | 0.5M +3P+5 | | 0.5M +3P+5 | | 0.5M +3P+6 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI0 slave timings, 4-Pin enable option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 24 | Delay from final SPI0_CLK edge to slave deassertion $\overline{\text{SPI0_ENA}}$ 48/ | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SPC_ENAH)S}$ | 1.5P-3 | 2.5P +17.5 | 1.5P-3 | 2.5P +20 | 1.5P-3 | 2.5P +27 | ns |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | -0.5M +1.5P-3 | -0.5M+ 2.5P+17.5 | -0.5M +1.5P-3 | -0.5M+ 2.5P+20 | -0.5M +1.5P-3 | -0.5M+ 2.5P+27 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 1.5P-3 | 2.5P +17.5 | 1.5P-3 | 2.5P +20 | 1.5P-3 | 2.5P +27 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | -0.5M +1.5P-3 | -0.5M+ 2.5P+17.5 | -0.5M +1.5P-3 | -0.5M+ 2.5P+20 | -0.5M +1.5P-3 | -0.5M+ 2.5P+27 | |
| **Additional SPI0 master timings, 4-Pin chip select option** 15/ 40/ 47/ 56/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 25 | Required delay from $\overline{\text{SPI0_SCS}}$ asserted at slave to first SPI0_CLK edge at slave | | $t_{d(SCSL_SPC)S}$ | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | Required delay from final SPI_CLK edge before $\overline{\text{SPI0_SCS}}$ is asserted | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SCSL_SCSH)S}$ | 0.5M+ P+4 | | 0.5M+ P+4 | | 0.5M+ P+5 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | P+4 | | P+4 | | P+5 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 0.5M+ P+4 | | 0.5M+ P+4 | | 0.5M+ P+5 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | P+4 | | P+4 | | P+5 | | |
| 27 | Delay from master asserting $\overline{\text{SPI0_SCS}}$ to slave driving SPI0_SOMI valid | | $t_{ena(SCSL_SOMI)S}$ | | P+17.5 | | P+20 | | P+27 | |
| 28 | Delay from master deasserting $\overline{\text{SPI0_SCS}}$ to slave 3-stating SPI0_SOMI | | $t_{dis(SCSH_SOMI)S}$ | | P+17.5 | | P+20 | | P+27 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI0 slave timings, 5-Pin option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 25 | Required delay from $\overline{\text{SPI0_SCS}}$ asserted at slave to first SPI0_CLK edge at slave | | $t_{d(SCSL_SPC)S}$ | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | Required delay from final SPI_CLK edge before $\overline{\text{SPI0_SCS}}$ is deasserted | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{d(SPC_SCSH)S}$ | 0.5M+ P+4 | | 0.5M+ P+4 | | 0.5M+ P+5 | | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | P+4 | | P+4 | | P+5 | | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | 0.5M+ P+4 | | 0.5M+ P+4 | | 0.5M+ P+5 | | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | P+4 | | P+4 | | P+5 | | |
| 27 | Delay from master asserting $\overline{\text{SPI0_SCS}}$ to slave driving SPI0_SOMI valid | | $t_{ena(SCSL_SOMI)S}$ | | P+17.5 | | P+20 | | P+27 | |
| 28 | Delay from master deasserting $\overline{\text{SPI0_SCS}}$ to slave 3-stating SPI0_SOMI | | $t_{dis(SCSH_SOMI)S}$ | | P+17.5 | | P+20 | | P+27 | |
| 29 | Delay from master deasserting $\overline{\text{SPI0_SCS}}$ to slave driving $\overline{\text{SPI0_ENA}}$ valid | | $t_{ena(SCSL_ENA)S}$ | | 17.5 | | 20 | | 27 | |
| 30 | Delay from final clock receive edge on SPI0_CLK to slave 3-stating or driving high $\overline{\text{SPI0_ENA}}$ 57/ | Polarity = 0, Phase = 0 to SPI0_CLK falling | $t_{dis(SPC_ENA)S}$ | | 2.5P +17.5 | | 2.5P +20 | | 2.5P +27 | |
| | | Polarity = 0, Phase = 1 to SPI0_CLK falling | | | 2.5P +17.5 | | 2.5P +20 | | 2.5P +27 | |
| | | Polarity = 1, Phase = 0 to SPI0_CLK rising | | | 2.5P +17.5 | | 2.5P +20 | | 2.5P +27 | |
| | | Polarity = 1, Phase = 1 to SPI0_CLK rising | | | 2.5P +17.5 | | 2.5P +20 | | 2.5P +27 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing** | | | | | | | | | | |
| **General timing requirements for SPI1 Master modes** 23/ 40/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 1 | Cycle time, SPI1_CLK, All master modes | | $t_{c(SPC)M}$ | 20 41/ | 256P | 30 41/ | 256P | 40 41/ | 256P | ns |
| 2 | Pulse width high, SPI1_CLK, All master modes | | $t_{w(SPCH)M}$ | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | |
| 3 | Pulse width low, SPI1_CLK, All master modes | | $t_{w(SPCL)M}$ | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | |
| 4 | Delay initial data bit valid on SPI1_SIMO after initial edge on SPI1_CLK 58/ | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(SIMO_SPC)M}$ | | 5 | | 5 | | 5 | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | | -0.5M +5 | | -0.5M +5 | | -0.5M +6 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | | 5 | | 5 | | 6 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | | -0.5M +5 | | -0.5M +5 | | -0.5M +6 | |
| 5 | Delay subsequent bits valid on SPI10_SIMO after transmit edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(SPC_SIMO)M}$ | | 5 | | 5 | | 6 | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | | 5 | | 5 | | 6 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | | 5 | | 5 | | 6 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | | 5 | | 5 | | 6 | |
| 6 | Output hold time, SPI1_SIMO valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{oh(SPC_SIMO)M}$ | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 0.5M -3 | | 0.5M -3 | | 0.5M -3 | | |
| 7 | Input setup time, SPI1_SOMI valid before receive edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{su(SOMI_SPC)M}$ | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 1.5 | | 1.5 | | 1.5 | | |
| 8 | Input hold time, SPI1_SOMI valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{ih(SPC_SOMI)M}$ | 4 | | 5 | | 6 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 4 | | 5 | | 6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 4 | | 5 | | 6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 4 | | 5 | | 6 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **General timing requirements for SPI1 Slave modes** 43/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 9 | Cycle time, SPI1_CLK, All slave modes | | $t_{c(SPC)S}$ 23/ | 40 41/ | | 50 41/ | | 60 41/ | | ns |
| 10 | Pulse width high, SPI1_CLK, All slave modes | | $t_{w(SPCH)S}$ 23/ | 18 | | 22 | | 27 | | |
| 11 | Pulse width low, SPI1_CLK, All slave modes | | $t_{w(SPCL)S}$ 23/ | 18 | | 22 | | 27 | | |
| 12 | Setup time, transmit data written to SPI before initial clock edge from master 45/ 58/ | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{su(SOMI_SPC)S}$ 23/ | 2P | | 2P | | 2P | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 2P | | 2P | | 2P | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | 2P | | 2P | | 2P | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 2P | | 2P | | 2P | | |
| 13 | Delay subsequent bits valid on SPI1_SOMI after transmit edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(SPC_SOMI)S}$ | | 15 | | 17 | | 19 | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | | 15 | | 17 | | 19 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | | 15 | | 17 | | 19 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | | 15 | | 17 | | 19 | |
| 14 | Output hold time, SPI1_SOMI valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{oh(SPC_SOMI)S}$ 23/ | 0.5S -4 | | 0.5S -10 | | 0.5S -12 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 0.5S -4 | | 0.5S -10 | | 0.5S -12 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 0.5S -4 | | 0.5S -10 | | 0.5S -12 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 0.5S -4 | | 0.5S -10 | | 0.5S -12 | | |
| 15 | Input setup time, SPI1_SIMO valid before receive edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{su(SIMO_SPC)S}$ 23/ | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 1.5 | | 1.5 | | 1.5 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 1.5 | | 1.5 | | 1.5 | | |
| 16 | Input hold time, SPI1_SIMO valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{ih(SPC_SIMO)S}$ 23/ | 4 | | 5 | | 6 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 4 | | 5 | | 6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 4 | | 5 | | 6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 4 | | 5 | | 6 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI1 master timings, 4-Pin enable option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 17 | Delay from slave assertion of $\overline{\text{SPI1_ENA}}$ active to first SPI1_CLK from master 59/ | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(ENA_SPC)M}$ | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | | 0.5M+ 3P+5 | | 0.5M+ 3P+5 | | 0.5M+ 3P+6 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | | 0.5M+ 3P+5 | | 0.5M+ 3P+5 | | 0.5M+ 3P+6 | |
| 18 | Max delay for slave to deassert $\overline{\text{SPI1_ENA}}$ after final SPI1_CLK edge to ensure master does not begin the next transfer. 60/ | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SPC_ENA)M}$ | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | | P+5 | | P+5 | | P+6 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | | P+5 | | P+5 | | P+6 | |
| **Additional SPI1 master timings, 4-Pin chip select option** 40/ 47/ | | | | | | | | | | |
| 19 | Delay from $\overline{\text{SPI1_SCS}}$ active to first SPI1_CLK 50/ 51/ | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(SCS_SPC)M}$ | 2P-1 | | 2P-5 | | 2P-6 | | ns |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 0.5M +2P-1 | | 0.5M +2P-5 | | 0.5M +2P-6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | 2P-1 | | 2P-5 | | 2P-6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 0.5M +2P-1 | | 0.5M +2P-5 | | 0.5M +2P-6 | | |
| 20 | Delay from final SPI1_CLK edge to master deasserting $\overline{\text{SPI1_SCS}}$. 62/ 63/ | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SPC_SCS)M}$ | 0.5M +P-1 | | 0.5M +P-5 | | 0.5M +P-6 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | P-1 | | P-5 | | P-6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 0.5M +P-1 | | 0.5M +P-5 | | 0.5M +P-6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | P-1 | | P-5 | | P-6 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI1 master timings, 5-Pin option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 18 | Max delay for slave to deassert $\overline{\text{SPI1_ENA}}$ after final SPI1_CLK edge to ensure master does not begin the next transfer. 60/ | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SPC_ENA)M}$ | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | ns |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | | P+5 | | P+5 | | P+6 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | | 0.5M+ P+5 | | 0.5M+ P+5 | | 0.5M+ P+6 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | | P+5 | | P+5 | | P+6 | |
| 20 | Delay from final SPI0_CLK edge to master deasserting $\overline{\text{SPI0_SCS}}$. 52/ 62/ | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SPC_SCS)M}$ | 0.5M+ P-1 | | 0.5M+ P-5 | | 0.5M+ P-6 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | P-1 | | P-5 | | P-6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 0.5M+ P-1 | | 0.5M+ P-5 | | 0.5M+ P-6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | P-1 | | P-5 | | P-6 | | |
| 21 | Max delay for slave SPI to drive $\overline{\text{SPI1_ENA}}$ valid after master asserts $\overline{\text{SPI1_SCS}}$ to delay the master from beginning the next transfer. | | $t_{d(SCSL_ENAL)M}$ | | 55/ | | 55/ | | 55/ | |
| 22 | Delay from $\overline{\text{SPI1_SCS}}$ active to first SPI1_CLK 51/ 61/ 64/ | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(SCS_SPC)M}$ | 2P-1 | | 2P-5 | | 2P-6 | | ns |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | 0.5M +2P-1 | | 0.5M +2P-5 | | 0.5M +2P-6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | 2P-1 | | 2P-5 | | 2P-6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | 0.5M +2P-1 | | 0.5M +2P-5 | | 0.5M +2P-6 | | |
| 23 | Delay from assertion $\overline{\text{SPI1_ENA}}$ low to first SPI1_CLK edge. 65/ | Polarity = 0, Phase = 0 to SPI1_CLK rising | $t_{d(ENA_SPC)M}$ | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK rising | | | 0.5M +3P+5 | | 0.5M +3P+5 | | 0.5M +3P+6 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK falling | | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK falling | | | 0.5M +3P+5 | | 0.5M +3P+5 | | 0.5M +3P+6 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI1 slave timings, 4-Pin enable option** 40/ 47/ 56/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 24 | Delay from final SPI1_CLK edge to slave deassertion $\overline{\text{SPI1_ENA}}$ | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SPC_ENAH)S}$ | 1.5P-3 | 2.5P +15 | 1.5P-10 | 2.5P +17 | 1.5P-12 | 2.5P +19 | ns |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | -0.5M +1.5P-3 | -0.5M+ 2.5P+15 | -0.5M+ 1.5P-10 | -0.5M+ 2.5P+17 | -0.5M+ 1.5P-12 | -0.5M+ 2.5P+19 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 1.5P-3 | 2.5P +15 | 1.5P-10 | 2.5P +17 | 1.5P-12 | 2.5P +19 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | -0.5M +1.5P-3 | -0.5M+ 2.5P+15 | -0.5M+ 1.5P-10 | -0.5M+ 2.5P+17 | -0.5M+ 1.5P-12 | -0.5M+ 2.5P+19 | |
| **Additional SPI0 master timings, 4-Pin chip select option** 15/ 40/ 47/ 56/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 25 | Required delay from $\overline{\text{SPI1_SCS}}$ asserted at slave to first SPI1_CLK edge at slave | | $t_{d(SCSL_SPC)S}$ | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | Required delay from final SPI_CLK edge before $\overline{\text{SPI1_SCS}}$ is asserted | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SCSL_SCSH)S}$ | 0.5M+ P+4 | | 0.5M+ P+5 | | 0.5M+ P+6 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | P+4 | | P+5 | | P+6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 0.5M+ P+4 | | 0.5M+ P+5 | | 0.5M+ P+6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | P+4 | | P+5 | | P+6 | | |
| 27 | Delay from master asserting $\overline{\text{SPI1_SCS}}$ to slave driving SPI1_SOMI valid | | $t_{ena(SCSL_SOMI)S}$ | | P+15 | | P+17 | | P+19 | |
| 28 | Delay from master deasserting $\overline{\text{SPI1_SCS}}$ to slave 3-stating SPI1_SOMI | | $t_{dis(SCSH_SOMI)S}$ | | P+15 | | P+17 | | P+19 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| **SPI Electrical Data/Timing – Continued.** | | | | | | | | | | |
| **Additional SPI0 slave timings, 5-Pin option** 40/ 46/ 47/ (see FIGURE 27 to 30) | | | | | | | | | | |
| 25 | Required delay from $\overline{\text{SPI1_SCS}}$ asserted at slave to first SPI1_CLK edge at slave | | $t_{d(SCSL_SPC)S}$ | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | Required delay from final SPI_CLK edge before $\overline{\text{SPI1_SCS}}$ is deasserted | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{d(SPC_SCSH)S}$ | 0.5M+ P+4 | | 0.5M+ P+5 | | 0.5M+ P+6 | | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | P+4 | | P+5 | | P+6 | | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | 0.5M+ P+4 | | 0.5M+ P+5 | | 0.5M+ P+6 | | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | P+4 | | P+5 | | P+6 | | |
| 27 | Delay from master asserting $\overline{\text{SPI1_SCS}}$ to slave driving SPI1_SOMI valid | | $t_{ena(SCSL_SOMI)S}$ | | P+15 | | P+17 | | P+19 | |
| 28 | Delay from master deasserting $\overline{\text{SPI1_SCS}}$ to slave 3-stating SPI1_SOMI | | $t_{dis(SCSH_SOMI)S}$ | | P+15 | | P+17 | | P+19 | |
| 29 | Delay from master deasserting $\overline{\text{SPI1_SCS}}$ to slave driving $\overline{\text{SPI1_ENA}}$ valid | | $t_{ena(SCSL_ENA)S}$ | | 15 | | 17 | | 19 | |
| 30 | Delay from final clock receive edge on SPI1_CLK to slave 3-stating or driving high $\overline{\text{SPI1_ENA}}$ 57/ | Polarity = 0, Phase = 0 to SPI1_CLK falling | $t_{dis(SPC_ENA)S}$ | | 2.5P +15 | | 2.5P +17 | | 2.5P +19 | |
| | | Polarity = 0, Phase = 1 to SPI1_CLK falling | | | 2.5P +15 | | 2.5P +17 | | 2.5P +19 | |
| | | Polarity = 1, Phase = 0 to SPI1_CLK rising | | | 2.5P +15 | | 2.5P +17 | | 2.5P +19 | |
| | | Polarity = 1, Phase = 1 to SPI1_CLK rising | | | 2.5P +15 | | 2.5P +17 | | 2.5P +19 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V, 1.1V, 1.0V | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard mode | | Fast mode | | |
| | | | Min | Max | Min | Max | |
| | **I2C Electrical Data/Timing** (see FIGURE 31 and 32) | | | | | | |
| **Timing requirements for I2C input** 23/ | | | | | | | |
| 1 | Cycle time, I2Cx_SCL | $t_{c(SCL)}$ | 10 | | 2.5 | | µs |
| 2 | Setup time, I2Cx_SCL high before I2Cx_SDA low | $t_{su(SCLH-SDAL)}$ | 4.7 | | 0.6 | | |
| 3 | Hold time, , I2Cx_SCL low after I2Cx_SDA low | $t_{h(SCLL-SDAL)}$ | 4 | | 0.6 | | |
| 4 | Pulse duration, I2Cx_SCL low | $t_{w(SCLL)}$ | 4.7 | | 1.3 | | |
| 5 | Pulse duration, I2Cx_SCL high | $t_{w(SCLH)}$ | 4 | | 0.6 | | |
| 6 | Setup time, I2Cx_SDA before I2Cx_SCL high | $t_{su(SDA-SCLH)}$ | 250 | | 100 | | |
| 7 | Hold time, I2Cx_SDA after I2Cx_SCL low | $t_{h(SDA-SCLL)}$ | 0 | | 0 | 0.9 | |
| 8 | Pulse duration, I2Cx_SDA high | $t_{w(SDAH)}$ | 4.7 | | 1.3 | | |
| 9 | Rise time, I2Cx_SDA | $t_{r(SDA)}$ | | 1000 | $20+0.1C_b$ | 300 | ns |
| 10 | Rise time, I2Cx_SCL | $t_{r(SCL)}$ | | 1000 | $20+0.1C_b$ | 300 | |
| 11 | Fall time, I2Cx_SDA | $t_{f(SDA)}$ | | 300 | $20+0.1C_b$ | 300 | |
| 12 | Fall time, I2Cx_SCL | $t_{f(SCL)}$ | | 300 | $20+0.1C_b$ | 300 | |
| 13 | Setup time, I2Cx_SCL high before I2Cx_SDA high | $t_{su(SCLH-SDAH)}$ | 4 | | 0.6 | | µs |
| 14 | Pulse duration, spike (must be suppressed) | $t_{w(SP)}$ | N/A | | 0 | 50 | ns |
| 15 | Capacitive load for each bus line | $C_b$ | | 400 | | 400 | pF |
| **Switching characteristics for I2C input** 23/ 67/ | | | | | | | |
| 16 | Cycle time, I2Cx_SCL | $t_{c(SCL)}$ | 10 | | 2.5 | | µs |
| 17 | Setup time, I2Cx_SCL high before I2Cx_SDA low | $t_{su(SCLH-SDAL)}$ | 4.7 | | 0.6 | | |
| 18 | Hold time, , I2Cx_SCL low after I2Cx_SDA low | $t_{h(SCLL-SDAL)}$ | 4 | | 0.6 | | |
| 19 | Pulse duration, I2Cx_SCL low | $t_{w(SCLL)}$ | 4.7 | | 1.3 | | |
| 20 | Pulse duration, I2Cx_SCL high | $t_{w(SCLH)}$ | 4 | | 0.6 | | |
| 21 | Setup time, I2Cx_SDA valid before I2Cx_SCL high | $t_{su(SDA-SCLH)}$ | 250 | | 100 | | |
| 22 | Hold time, I2Cx_SDA valid after I2Cx_SCL low | $t_{h(SDA-SCLL)}$ | 0 | | 0 | 0.9 | |
| 23 | Pulse duration, I2Cx_SDA high | $t_{w(SDAH)}$ | 4.7 | | 1.3 | | |
| 28 | Setup time, I2Cx_SCL high before I2Cx_SDA high | $t_{su(SCLH-SDAH)}$ | 4 | | 0.6 | | |

| No. | Test | Symbol | Test conditions 2/ | 1.3V, 1.2V, 1.1V, 1.0V | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| | **UART Electrical Data/Timing** | | | | | |
| **Timing requirements for UART receive** 23/ 68/ (See FIGURE 33) | | | | | | |
| 4 | Pulse duration, receive data bit (RXDn) | $t_{w(URXDB)}$ | | 0.96U | 1.05U | ns |
| 5 | Pulse duration, receive start bit | $t_{w(URXSB)}$ | | 0.96U | 1.05U | |
| **Switching characteristics for UARTx transmit** 23/ 68/ (See FIGURE 33) | | | | | | |
| 1 | Maximum programmable baud rate | f(baud) | | | D/E 69/ 70 | MBaud 71/ |
| 2 | Pulse duration, transmit data bit (TXDn) | $t_{w(UTXDB)}$ | | U-2 | U+2 | ns |
| 3 | Pulse duration, transmit start bit | $t_{w(UTXSB)}$ | | U-2 | U+2 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test 2/ | Symbol | 1.3V, 1.2V, 1.1V, 1.0V | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Low Speed 1.5 Mbps | | Full Speed 12 Mbps | | High Speed 480 Mbps | | |
| | | | Min | Max | Min | Max | Min | Max | |
| | **USB0 [USB2.0] Electrical Data/Timing** | | | | | | | | |
| **Switching characteristics for USB0 [USB2.0]** 23/ (See FIGURE 34) | | | | | | | | | |
| 1 | Rise time, USB_DP and USB_DM signals 72/ | $t_{r(D)}$ | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 2 | Fall time, USB_DP and USB_DM signals 72/ | $t_{f(D)}$ | 75 | 300 | 4 | 20 | 0.5 | | |
| 3 | Rise/Fall time matching 73/ | $t_{rf(M)}$ | 80 | 120 | 90 | 111 | - | - | % |
| 4 | Output signal cross-over voltage 72/ | $V_{CRS}$ | 1.3 | 2 | 1.3 | 2 | - | - | V |
| 5 | Source (Host) Driver jitter, nest transition | $t_{jr(source)NT}$ | | 2 | | 2 | | | ns 74/ |
| | Function driver jitter, paired transition 75/ | $t_{jr(FUNC)NT}$ | | 25 | | 2 | | 74/ | ns |
| 6 | Source (Host) Driver jitter, nest transition | $t_{jr(source)PT}$ | | 1 | | 1 | | 74/ | |
| | Function driver jitter, paired transition 75/ | $t_{jr(FUNC)PT}$ | | 10 | | 1 | | 74/ | |
| 7 | Pulse duration, EOP transmitter | $t_{w(EOPT)}$ | 1250 | 1500 | 160 | 175 | - | - | |
| 8 | Pulse duration, EOP receiver | $t_{w(EOPR)}$ | 670 | | 82 | | - | | |
| 9 | Data rate | $t_{(DRATE)}$ | | 1.5 | | 12 | | 480 | Mb/s |
| 10 | Driver output resistance | $Z_{DRV}$ | - | - | 40.5 | 49.5 | 40.5 | 49.5 | Ω |
| 11 | Receiver input impedance | $Z_{INP}$ | 100k | | 100k | | - | - | |
| | **Universal Serial Bus Host Controller (USB1) [USB1.1 OHCI]** | | | | | | | | |
| **Switching characteristics for USB1 [USB1.1]** 23/ | | | | | | | | | |
| U1 | Rise time, USB.DP and USB.DM signals 72/ | $t_r$ | 75 | 300 | 4 | 20 | | | ns |
| U2 | Fall time, USB.DP and USB.DM signals 72/ | $t_f$ | 75 | 300 | 4 | 20 | | | |
| U3 | Rise/Fall time matching 73/ | $t_{RFM}$ | 80 | 120 | 90 | 110 | | | % |
| U4 | Output signal cross-over voltage 72/ | $V_{CRS}$ | 1.3 | 2 | 1.3 | 2 | | | V |
| U5 | Differential propagation jitter 75/ | $t_j$ | -25 | 25 | -2 | 2 | | | ns |
| U6 | Operating frequency 76/ | $f_{op}$ | | 1.5 | | 12 | | | MHz |

| No. | Test | Symbol | 1.3V, 1.2V, 1.1 V | | | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | 10 Mbs | | 100 Mbs | | 10 Mbs | | |
| | | | Min | Max | Min | Max | Min | Max | |
| | **EMAC Electrical Data/Timing** | | | | | | | | |
| **Timing requirements for MII_RXCLK** 23/ (see FIGURE 35) | | | | | | | | | |
| 1 | Cycle time, MII_RXCLK | $t_{c(MII_RXCLK)}$ | 400 | | 40 | | 400 | | ns |
| 2 | Pulse duration, MII_RXCLK high | $t_{w(MII_RXCLKH)}$ | 140 | | 14 | | 140 | | |
| 3 | Pulse duration, MII_RXCLK low | $t_{w(MII_RXCLKL)}$ | 140 | | 14 | | 140 | | |
| **Timing requirements for MII_TXCLK** 23/ (see FIGURE 36) | | | | | | | | | |
| 1 | Cycle time, MII_TXCLK | $t_{c(MII_TXCLK)}$ | 400 | | 40 | | 400 | | ns |
| 2 | Pulse duration, MII_TXCLK high | $t_{w(MII_TXCLKH)}$ | 140 | | 14 | | 140 | | |
| 3 | Pulse duration, MII_TXCLK low | $t_{w(MII_TXCLKL)}$ | 140 | | 14 | | 140 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | 1.3V, 1.2V, 1.1 V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| | **EMAC Electrical Data/Timing – Continued.** | | | | | | |
| **Timing requirements for EMAC MII receive 10/100 Mbit/s** 23/ 77/ (see FIGURE 37) | | | | | | | |
| 1 | Setup time, receive selected signals valid before MII_RXCLK high | $t_{su(MRXD_RXCLKH)}$ | 8 | | 8 | | ns |
| 2 | Hold time, receive selected signals valid after MII_RXCLK high | $t_{h(MII_RXCLKH-MRXD)}$ | 8 | | 8 | | |
| **Switching characteristics for EMAC MII transmit 10/100 Mbit/s** 23/ 78/ (see FIGURE 38) | | | | | | | |
| 1 | Delay time, MII_TXCLK high to transmit selected signals valid | $t_{d(MII_TXCLKH-MTXD)}$ | 2 | 25 | 2 | 32 | ns |
| **Timing requirements for EMAC RMII** 23/ 79/ (see FIGURE 39) | | | | | | | |
| 1 | Cycle time, RMII_MHz_50_CLK | $t_{c(REFCLK)}$ | 20 TYP | | | | ns |
| 2 | Pulse width, RMII_MHz_50_CLK high | $t_{w(REFCLKH)}$ | 7 | 13 | | | |
| 3 | Pulse width, RMII_MHz_50_CLK low | $t_{w(REFCLKL)}$ | 7 | 13 | | | |
| 6 | Input setup time, RXD valid before RMII_MHz_50_CLK high | $t_{su(RXD-REFCLK)}$ | 4 | | | | |
| 7 | Input hold time, RXD valid after RMII_MHz_50_CLK high | $t_{h(REFCLK-RXD)}$ | 2 | | | | |
| 8 | Input setup time, CRSDV valid before RMII_MHz_50_CLK high | $t_{su(CRSDV-REFCLK)}$ | 4 | | | | |
| 9 | Input hold time, CRSDV valid after RMII_MHz_50_CLK high | $t_{h(REFCLK-CRSDV)}$ | 2 | | | | |
| 10 | Input setup time, RXER valid before RMII_MHz_50_CLK high | $t_{su(RXER-REFCLK)}$ | 4 | | | | |
| 11 | Input hold time, RXER valid after RMII_MHz_50_CLK high | $t_{h(REFCLK-RXER)}$ | 2 | | | | |
| **Switching characteristics for EMAC RMII** 23/ 79/ (see FIGURE 39) | | | | | | | |
| 4 | Output delay time, RMII_MHz_50_CLK high to TXD valid | $t_{h(REFCLK-TXD)}$ | 2.5 | 13 | | | ns |
| 5 | Output delay time, RMII_MHz_50_CLK high to TXEN valid | $t_{h(REFCLK-TXEN)}$ | 2.5 | 13 | | | |
| | **Management data Input/Output (MDIO) electrical Data/Timing** | | | | | | |
| **Timing requirements for MDIO Input** 23/ (see FIGURE 40 and 41) | | | | | | | |
| 1 | Cycle time, MCCLK | $t_{c(MDCLK)}$ | 400 | | 400 | | ns |
| 2 | Pulse duration, MDCLK | $t_{w(MDCLK)}$ | 180 | | 180 | | |
| 3 | Transition time, MDCLK | $t_{t(MDCLK)}$ | | 5 | | 5 | |
| 4 | Setup time, MDIO data input valid before MDCLK high | $t_{su(MDIO-MDCLKH)}$ | 16 | | 21 | | |
| 5 | Hold time, MDIO data input valid after MDCLK high | $t_{h(MDCLKH-MDDIO)}$ | 0 | | 0 | | |
| **Switching characteristics for MDOI Output** 23/ (see FIGURE 41) | | | | | | | |
| 7 | Delay time, MDCLK low to MDIO data output valid | $t_{d(MDCLKL-MDIO)}$ | 0 | 100 | 0 | 100 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | 1.3V, 1.2V, 1.1 V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| | **LCD Interface Display Driver (LIDD Mode)** | | | | | | |
| **Timing requirements for LCD LIDD Mode** 23/ | | | | | | | |
| 16 | Setup time, LCD_D[15:0] valid before LCD_CLK (SYSCLK2) high | $t_{su(LCD_D)}$ | 7 | | 8 | | ns |
| 17 | Hold time, LCD_D[15:0] valid after LCD_CLK (SYSCLK2) high | $t_{h(LCD_D)}$ | 0 | | 0 | | |
| **Switching characteristics for LCD LIDD Mode** 23/ | | | | | | | |
| 4 | Delay time, LCD_CLK (SYSCLK2) high toLCD_D[15:0] valid (write) | $t_{d(LCD_D_V)}$ | 0 | 7 | 0 | 9 | ns |
| 5 | Delay time, LCD_CLK (SYSCLK2) high toLCD_ D[15:0] invalid (write) | $t_{d(LCD_D_I)}$ | 0 | 7 | 0 | 9 | |
| 6 | Delay time, LCD_CLK (SYSCLK2) high to $\overline{LCD_AC_ENB_CS}$ low | $t_{d(LCD_E_A)}$ | 0 | 7 | 0 | 9 | |
| 7 | Delay time, LCD_CLK (SYSCLK2) high to $\overline{LCD_AC_ENB_CS}$ high | $t_{d(LCD_E_I)}$ | 0 | 7 | 0 | 9 | |
| 8 | Delay time, LCD_CLK (SYSCLK2) high to LCD_VSYNC low | $t_{d(LCD_A_A)}$ | 0 | 7 | 0 | 9 | |
| 9 | Delay time, LCD_CLK (SYSCLK2) high to LCD_VSYNC high | $t_{d(LCD_A_I)}$ | 0 | 7 | 0 | 9 | |
| 10 | Delay time, LCD_CLK (SYSCLK2) high to LCD_HSYNC low | $t_{d(LCD_W_A)}$ | 0 | 7 | 0 | 9 | |
| 11 | Delay time, LCD_CLK (SYSCLK2) high to LCD_HSYNC high | $t_{d(LCD_W_I)}$ | 0 | 7 | 0 | 9 | |
| 12 | Delay time, LCD_CLK (SYSCLK2) high to LCD_PCLK active | $t_{d(LCD_STRB_A)}$ | 0 | 7 | 0 | 9 | |
| 13 | Delay time, LCD_CLK (SYSCLK2) high to LCD_ PCLK inactive | $t_{d(LCD_STRB_I)}$ | 0 | 7 | 0 | 9 | |
| 14 | Delay time, LCD_CLK (SYSCLK2) high to LCD_ D[15:0] in 3-state | $t_{d(LCD_D_Z)}$ | 0 | 7 | 0 | 9 | |
| 15 | Delay time, LCD_CLK (SYSCLK2) high to LCD_ D[15:0] (valid from 3-sate) | $t_{d(Z_LCD_D)}$ | 0 | 7 | 0 | 9 | |
| | **LCD Raster Mode** | | | | | | |
| **Switching characteristics for LCD Raster Mode** 23/ (see FIGURE 42 to 46) | | | | | | | |
| 1 | Cycle time, pixel clock | $t_{c(PIXEL_CLK)}$ | 26.66 | | 33.33 | | ns |
| 2 | Pulse duration, pixel clock high | $t_{w(PIXEL_CLK_H)}$ | 10 | | 10 | | |
| 3 | Pulse duration, pixel clock low | $t_{w(PIXEL_CLK_L)}$ | 10 | | 10 | | |
| 4 | Delay time, LCD_PCLK high to LCD_D[15:0] valid (write) | $t_{d(LCD_D_V)}$ | 0 | 7 | 0 | 9 | |
| 5 | Delay time, LCD_PCLK high toLCD_ D[15:0] invalid (write) | $t_{d(LCD_D_IV)}$ | 0 | 7 | 0 | 9 | |
| 6 | Delay time, LCD_PCLK low to $\overline{LCD_AC_ENB_CS}$ high | $t_{d(LCD_AC_ENB_CS_A)}$ | 0 | 7 | 0 | 9 | |
| 7 | Delay time, LCD_PCLK low to $\overline{LCD_AC_ENB_CS}$ low | $t_{d(LCD_AC_ENB_CS_I)}$ | 0 | 7 | 0 | 9 | |
| 8 | Delay time, LCD_PCLK low to LCD_VSYNC high | $t_{d(LCD_VSYNC_A)}$ | 0 | 7 | 0 | 9 | |
| 9 | Delay time, LCD_PCLK low to LCD_VSYNC low | $t_{d(LCD_VSYNC_I)}$ | 0 | 7 | 0 | 9 | |
| 10 | Delay time, LCD_PCLK high to LCD_HSYNC high | $t_{d(LCD_HSYNC_A)}$ | 0 | 7 | 0 | 9 | |
| 11 | Delay time, LCD_PCLK high to LCD_HSYNC low | $t_{d(LCD_HSYNC_I)}$ | 0 | 7 | 0 | 9 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | Symbol | 1.3V, 1.2V, 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| | **HPI Electrical Data/Timing** (se FIGURE 47-50) | | | | | | |
| | **Timing requirements for Host Port Interface HPI Electrical Data/Timing [1.2V, 1.1V]** 23/ 80/ 81/ | | | | | | |
| 1 | Setup time, select signals 82/ valid before $\overline{\text{UHPI_HSTROBE}}$ low | $t_{su(SELV-HSTBL)}$ | 5 | | 5 | | ns |
| 2 | Hold time, select signals 82/ valid after $\overline{\text{UHPI_HSTROBE}}$ low | $t_{h(HSTBL-SELV)}$ | 2 | | 2 | | |
| 3 | Pulse duration, $\overline{\text{UHPI_HSTROBE}}$ active low | $t_{w(HSTBL)}$ | 15 | | 15 | | |
| 4 | Pulse duration, $\overline{\text{UHPI_HSTROBE}}$ inactive high between consecutive accesses | $t_{w(HSTBH)}$ | 2M | | 2M | | |
| 9 | Setup time, selects signals valid before $\overline{\text{UHPI_HAS}}$ low | $t_{su(SELV-HASL)}$ | 5 | | 5 | | |
| 10 | Hold time, selects signals valid after $\overline{\text{UHPI_HAS}}$ low | $t_{h(HASL-SELV)}$ | 2 | | 2 | | |
| 11 | Setup time, host data valid before $\overline{\text{UHPI_HSTROBE}}$ high | $t_{su(HDV-HSTBH)}$ | 5 | | 5 | | |
| 12 | Hold time, host data valid after $\overline{\text{UHPI_HSTROBE}}$ high | $t_{h(HSTBH-HDV)}$ | 2 | | 2 | | |
| 13 | Setup time, $\overline{\text{UHPI_HSTROBE}}$ high after $\overline{\text{UHPI_HRDY}}$ low, $\overline{\text{UHPI_HSTROBE}}$ should not be inactivated until $\overline{\text{UHPI_HRDY}}$ is active (low); otherwise, HPI writes will not complete properly. | $t_{h(HRDYL-HSTBH)}$ | 2 | | 2 | | |
| 16 | Setup time, $\overline{\text{UHPI_HAS}}$ low before $\overline{\text{UHPI_HSTROBE}}$ low | $t_{su(HASL-HSTBL)}$ | 5 | | 5 | | |
| 17 | Hold time, $\overline{\text{UHPI_HAS}}$ low after $\overline{\text{UHPI_HSTROBE}}$ low | $t_{h(HSTBL-HASH)}$ | 2 | | 2 | | |

| No. | Test | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | **Switching for Host Port Interface** 23/ 81/ 83/ 84/ | | | | | | | | |
| 5 | Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ valid 85/ | $t_{d(HSTBL-HRDYV)}$ | | 15 | | 17 | | 22 | ns |
| 5a | Delay time, $\overline{\text{HAS}}$ low to $\overline{\text{HRDY}}$ valid | $t_{d(HASL-HRDYV)}$ | | 15 | | 17 | | 22 | |
| 6 | Enable time, HD driven from $\overline{\text{HSTROBE}}$ low | $t_{en(HSTBL-HDLZ)}$ | 1.5 | | 1.5 | | 1.5 | | |
| 7 | Delay time, $\overline{\text{HRDY}}$ low to HD valid | $t_{d(HRDYL-HDV)}$ | | 0 | | 0 | | 0 | |
| 8 | Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high | $t_{oh(HSTBH-HDV)}$ | 1.5 | | 1.5 | | 1.5 | | |
| 14 | Disable time, HD high impedance from $\overline{\text{HSTROBE}}$ high | $t_{dis(HSTBH-HDHV)}$ | | 15 | | 17 | | 22 | |
| 15 | Delay time, $\overline{\text{HSTROBE}}$ low to HD valid 86/ | $t_{d(HSTBL-HDV)}$ | | 15 | | 17 | | 22 | |
| 18 | Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ valid 87/ | $t_{d(HSTBH-HRDYV)}$ | | 15 | | 17 | | 22 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| | **µPP Electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for µPP** (see FIGURE 51 to 54) 23/ | | | | | | | | | | |
| 1 | Cycle time, CHn_CLK | SDR mode | $t_{c(INCLK)}$ | 13.33 | | 20 | | 26.66 | | ns |
| | | DDR mode | | 26.66 | | 40 | | 53.33 | | |
| 2 | Pulse width, CHn_CLK high | SDR mode | $t_{w(INCLKH)}$ | 5 | | 8 | | 10 | | |
| | | DDR mode | | 10 | | 16 | | 20 | | |
| 3 | Pulse width, CHn_CLK low | SDR mode | $t_{w(INCLKL)}$ | 5 | | 8 | | 10 | | |
| | | DDR mode | | 10 | | 16 | | 20 | | |
| 4 | Setup time, CHn_START valid before CHn_CLK high | | $t_{su(STV-INCLKH)}$ | 4 | | 5.5 | | 6.5 | | |
| 5 | Hold time, CHn_START valid after CHn_CLK high | | $t_{h(INCLKH-STV)}$ | 0.8 | | 0.8 | | 0.8 | | |
| 6 | Setup time, CHn_ENABLE valid before CHn_CLK high | | $t_{su(ENV-INCLKH)}$ | 4 | | 5.5 | | 6.5 | | |
| 7 | Hold time, CHn_ENABLE valid after CHn_CLK high | | $t_{h(INCLKH-ENV)}$ | 0.8 | | 0.8 | | 0.8 | | |
| 8 | Setup time, CHn_DATA/XDATA valid before CHn_CLK high | | $t_{su(DV-INCLKH)}$ | 4 | | 5.5 | | 6.5 | | |
| 9 | Hold time, CHn_DATA/XDATA valid after CHn_CLK high | | $t_{h(INCLKH-DV)}$ | 0.8 | | 0.8 | | 0.8 | | |
| 10 | Setup time, CHn_DATA/XDATA valid before CHn_CLK low | | $t_{su(DV-INCLKl)}$ | 4 | | 5.5 | | 6.5 | | |
| 11 | Hold time, CHn_DATA/XDATA valid after CHn_CLK low | | $t_{h(INCLKL-DV)}$ | 0.8 | | 0.8 | | 0.8 | | |
| 19 | Setup time, CHn_WAITvalid before CHn_CLK high | | $t_{su(WTV-INCLKH)}$ | 10 | | 12 | | 14 | | |
| 20 | Hold time, CHn_WAIT valid after CHn_CLK high | | $t_{h(INCLKH-WTV)}$ | 0.8 | | 0.8 | | 0.8 | | |
| 21 | Cycle time, 2xTXCLK input clock 88/ | | $t_{c(2xTXCLK)}$ | 6.66 | | 10 | | 13.33 | | |
| **Switching characteristics for µPP** (see FIGURE 51 to 54) 23/ | | | | | | | | | | |
| 12 | Cycle time, CHn_CLK | SDR mode | $t_{c(OUTCLK)}$ | 13.33 | | 20 | | 26.66 | | ns |
| | | DDR mode | | 26.66 | | 40 | | 53.33 | | |
| 13 | Pulse width, CHn_CLK high | SDR mode | $t_{w(OUTCLKH)}$ | 5 | | 8 | | 10 | | |
| | | DDR mode | | 10 | | 16 | | 20 | | |
| 14 | Pulse width, CHn_CLK low | SDR mode | $t_{w(OUTCLKL)}$ | 5 | | 8 | | 10 | | |
| | | DDR mode | | 10 | | 16 | | 20 | | |
| 15 | Delay time, CHn_START valid after CHn_CLK high | | $t_{d(OUTCLKH-STV)}$ | 2 | 11 | 2 | 15 | 2 | 21 | |
| 16 | Delay time, CHn_ENABLE valid after CHn_CLK high | | $t_{d(OUTCLKH-ENV)}$ | 2 | 11 | 2 | 15 | 2 | 21 | |
| 17 | Delay time, CHn_DATA/XDATA valid after CHn_CLK high | | $t_{d(OUTCLKH-DV)}$ | 2 | 11 | 2 | 15 | 2 | 21 | |
| 18 | Delay time, CHn_DATA/XDATA valid after CHn_CLK low | | $t_{d(OUTCLKL-DV)}$ | 2 | 11 | 2 | 15 | 2 | 21 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | | Symbol | 1.3V | | 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| | **VPIF Electrical Data/Timing** | | | | | | | | | | | |
| **Timing requirements for VPIF VP_CLKINx Inputs** (see FIGURE 55) 23/ 89/ | | | | | | | | | | | | |
| 1 | Cycle time, VP_CLKIN0 | | $t_{c(VKI)}$ | 13.3 | | 13.3 | | 20 | | 37 | | ns |
| | Cycle time, VP_CLKIN1/2/3 | | | 13.3 | | 13.3 | | 20 | | 37 | | |
| 2 | Pulse duration, VP_CLKINx high | | $t_{w(VKIH)}$ | 0.4C | | 0.4C | | 0.4C | | 0.4C | | |
| 3 | Pulse duration, VP_CLKINx low | | $t_{w(VKIL)}$ | 0.4C | | 0.4C | | 0.4C | | 0.4C | | |
| 4 | Transition time, VP_CLKINx | | $t_{t(VKI)}$ | | 5 | | 5 | | 5 | | 5 | |
| **Timing requirements for VPIF channels 0/1 Video capture data and control Inputs** (see FIGURE 56) | | | | | | | | | | | | |
| 1 | Setup time, VP_DINx valid before VP_OSCIN0/1 high | | $t_{su(VDINV-VKIH)}$ | 4 | | 4 | | 6 | | 7 | | ns |
| 2 | Hold time, VP_DINx valid after VP_OSCIN0/1 high | | $t_{h(VKIH-VDINV)}$ | 0.5 | | 0 | | 0 | | 0 | | |
| **Switching characteristics for video data shown with respect to VP_CLKOUT2/3** (see FIGURE 57) 23/ 90/ | | | | | | | | | | | | |
| 1 | Cycle time, VP_CLKOUT2/3 | | $t_{c(VKO)}$ | 13.3 | | 13.3 | | 20 | | 37 | | ns |
| 2 | Pulse duration, VP_CLKOUT2/3 high | | $t_{w(VKOH)}$ | 0.4C | | 0.4C | | 0.4C | | 0.4C | | |
| 3 | Pulse duration, VP_CLKOUT2/3 high | | $t_{w(VKOL)}$ | 0.4C | | 0.4C | | 0.4C | | 0.4C | | |
| 4 | Transition time, VP_CLKOUT2/3 | | $t_{t(VKO)}$ | | 5 | | 5 | | 5 | | 5 | |
| 11 | Delay time, VP_CLKOUT2/3 high to VP_DOUTx valid | | $t_{d(VKOH-VPDOUTV)}$ | | 8.5 | | 8.5 | | 12 | | 17 | |
| 12 | Hold time, VP_CLKOUT2/3 high to VP_DOUTx invalid | | $t_{d(VCLKOH-VPDOUTIV)}$ | 1.5 | | 1.5 | | 1.5 | | 1.5 | | |
| | **Enhanced Capture (eCAP) Electrical Data/timng** | | | | | | | | | | | |
| **Timing requirements for Enhanced Capture (eCAP)** (see FIGURE 58) 23/ | | | | | | | | | | | | |
| | Capture input pulse width | Asynchronous | tw(CAP) | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | cycles |
| | | Synchronous | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | |
| **Switching for eCAP** 23/ | | | | | | | | | | | | |
| | Pulse duration, APWMx output high/low | | $t_{w(APWM)}$ | 20 | | 20 | | 20 | | 20 | | ns |
| | **Enhanced Pulse width Modulator (eHRPWM) Timing** | | | | | | | | | | | |
| **Timing requirements for eHRPWM** 23/ | | | | | | | | | | | | |
| | Sync input pulse width | Asynchronous | $t_{w(SYNCIN)}$ | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | cycles |
| | | Synchronous | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | |
| **Switching characteristics for eHRPWM** 23/ | | | | | | | | | | | | |
| | Pulse duration, PWMx output high/low | | $t_{w(PWM)}$ | 20 | | 20 | | 20 | | 26.6 | | ns |
| | Sync output pulse width | | $t_{w(SYNCOUT)}$ | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | cycles |
| | Delay time, trip input active to PWM forced high/low | no pin load, no additional programmable delay | $t_{d(PWM)TZA}$ | | 25 | | 25 | | 25 | | 25 | ns |
| | Delay time, trip input active to PWM Hi-Z | no additional programmable delay | $t_{d(TZ-PWM)HZ}$ | | 20 | | 20 | | 20 | | 20 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

| No. | Test | | Symbol | 1.3V, 1.2V | | 1.1V | | 1.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| | **Trip Zone input timing** | | | | | | | | | |
| **Trip zone input timing requirements** 23/ (see FIGURE 59) | | | | | | | | | | |
| | Pulse duration, $\overline{TZx}$ input low | Asynchronous | $t_{w(TZ)}$ | $1t_{c(SCO)}$ | | $1t_{c(SCO)}$ | | $1t_{c(SCO)}$ | | cycles |
| | | Synchronous | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | $2t_{c(SCO)}$ | | |
| **High resolution PWM characteristics at SYSCLKOUT = (60 – 100 MHz)** 23/ | | | | | | | | | | |
| | Micro edge positioning (MEP) step size 91/ | | | 200 TYP | | 200 TYP | | 200 TYP | | ps |
| | **Timer electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for Timer Input** 23/ 92/ 93/ (see FIGURE 60) | | | | | | | | | | |
| 1 | Cycle time, TM64Px_IN12 | | $t_{c(TM64Px_IN12)}$ | 4P | | 4P | | 4P | | ns |
| 2 | Pulse duration, TM64Px_IN12 high | | $t_{w(TINPH)}$ | 0.45C | 0.55C | 0.45C | 0.55C | 0.45C | 0.55C | |
| 3 | Pulse duration, TM64Px_IN12 low | | $t_{w(TINPL)}$ | 0.45C | 0.55C | 0.45C | 0.55C | 0.45C | 0.55C | |
| 4 | Transition time, TM64Px_IN12 | | $t_{t(TM64Px_IN12)}$ | | 0.25P or 10 94/ | | 0.25P or 10 94/ | | 0.25P or 10 94/ | |
| **Switching characteristics for Timer Output** 23/ 92/ (see FIGURE 61) | | | | | | | | | | |
| 5 | Pulse duration, TM64Px_IN12 high | | $t_{w(TINPH)}$ | 4P | | 4P | | 4P | | ns |
| 6 | Pulse duration, TM64Px_IN12 low | | $t_{w(TINPL)}$ | 4P | | 4P | | 4P | | |
| | **GPIO peripheral Input/Output Electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for GPIO Inputs** 23/ 95/ 96/ (see FIGURE 62) | | | | | | | | | | |
| 1 | Pulse duration, GPn[m] as input high | | $t_{w(GPIH)}$ | 2C | | 2C | | 2C | | ns |
| 2 | Pulse duration, GPn[m] as input low | | $t_{w(GPIL)}$ | 2C | | 2C | | 2C | | |
| **Switching characteristics for GPIO Outputs** 23/ (see FIGURE 62) | | | | | | | | | | |
| 3 | Pulse duration, GPn[m] as input high 95/ 96/ | | $t_{w(GPIH)}$ | 2C | | 2C | | 2C | | ns |
| 4 | Pulse duration, GPn[m] as input low | | $t_{w(GPIL)}$ | 2C | | 2C | | 2C | | |
| | **GPIO peripheral external Interrupt Electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for External Interrupts** 23/ 95/ 96/ (see FIGURE 63) | | | | | | | | | | |
| 1 | Width of the external interrupt pulse low | | $t_{w(LOW)}$ | 2C | | 2C | | 2C | | ns |
| 2 | Width of the external interrupt pulse high | | $t_{w(HIGH)}$ | 2C | | 2C | | 2C | | |
| | **JTAG test port Electrical Data/Timing** | | | | | | | | | |
| **Timing requirements for JTAG test port** 23/ (see FIGURE 64) | | | | | | | | | | |
| 1 | Cycle time, TCK | | $t_{c(TCK)}$ | 40 | | 50 | | 66.6 | | ns |
| 2 | Pulse duration, TCK high | | $t_{w(TCKH)}$ | 16 | | 20 | | 26.6 | | |
| 3 | Pulse duration, TCK low | | $t_{w(TCKL)}$ | 16 | | 20 | | 26.6 | | |
| 4 | Cycle time, RTCK | | $t_{c(RTCK)}$ | 40 | | 50 | | 66.6 | | |
| 5 | Pulse duration, RTCK high | | $t_{w(RTCKH)}$ | 16 | | 20 | | 26.6 | | |
| 6 | Pulse duration, RTCK low | | $t_{w(RTCKL)}$ | 16 | | 20 | | 26.6 | | |
| 7 | Setup time, TDI/TMS/$\overline{TRST}$ valid before RTCK high | | $t_{d(TDIV-RTCKH)}$ | 4 | | 4 | | 4 | | |
| 8 | Hold time, TDI/TMS/$\overline{TRST}$ valid after RTCK high | | $t_{h(RTCKH-TDIV)}$ | 4 | | 6 | | 8 | | |
| **Switching characteristics for JAG test port port** 23/ (see FIGURE 64) | | | | | | | | | | |
| 9 | Delay time, RTCK low to TDO valid | | $t_{d(RTCKL-TDOV)}$ | | 18 | | 23 | | 31 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Recommended ranges of supply voltage and operating junction temperature (unless otherwise noted).
3/ These IO specifications apply to the dual voltage IOs only and do not apply to DDR2/mDDR or SATA in terfaces. DDR2/mDDR IOs are 1.8 V IOs and adhere to the JESD79-2A standard. USB0 i/os adhere to the USB2.0 standard. USB1 I/Os adhere to the USB1.1 standard. SATA I/Os adhere to the SATA-I and SATA-II standards.
4/ $I_I$ applies to the input only pins and bi-directional pins. For input only pins, $I_I$ indicates the input leakage current. For bi-directional pins, $I_I$ indicates the input leakage current and of state (Hi-Z) output leakage current.
5/ Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor. The pullup and pulldown strengths shown represent the minimum and maximum strength across process variation.
6/ to $\overline{\text{RESETOUT}}$ is multiplexed with other oins functions. See manufacturer data for more information.
7/ For power-on reset (POR), the reset timings in this table refer to $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ together. For warm reset, the reset timings in this table refers to $\overline{\text{RESET}}$ only ($\overline{\text{TRST}}$ is held high).
8/ Parameters are characterized from -45°C to 105°C unless otherwise noted.
9/ OSCIN cycles.
10/ Crystal oscillator cannot be operated beyond -40°C to 105°C.
11/ Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise on input signals.
12/ The time that the application has to wait for the PLL to acquire lock before setting PLLEN, after changing PREDIV, PLLM, or OSCIN.
13/ Max PLL lock time = $\frac{2000\ \text{N}}{\sqrt{\text{m}}}$ where N = Pre-divider ratio; M = PLL multiplier.
The multiplier values must be chosen such that the PLL output frequency (at PLLOUT) is between 300 and 600 MHz, but the frequency going into the SYSCLK dividers (after the post divider) cannot exceed the maximum clock frequency defined for the device at a given voltage operating point.
14/ 30 (if internal oscillator is used); 50(if external clock is used).
15/ These parameters are not production tested and are specified by design to work from -40°C to 125°C.
16/ E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL0 output clock divided by 4.5. As an example when SYSCLK3 is selected and set to 100 MHz, E = 10 ns.
17/ Setup before end of STROBE phase (if no extended wait state are inserted) by which EM_WAIT must be asserted to add extended wait states. FIGURE 15 and FIGURE16 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.
18/ TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = write setup, WST = Write strobe, WH = Write hold, WEWC = Maximum external wait cycles. These parameters are programmed via Asynchronous Bank and Asynchronous Wait cycles Configuration Registers. These support the following range values: TA[4-1], RS[6-1], RST[64-1], RH[8-1], WS[6-1], WST[64-1], WH[8-1], and MEW[1-256].
19/ EWC = external wait cycles determined by EMA_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before time out is specified by bit field WEWC in Asynchronous Wait Cycle Configuration Register.
20/ DDR2 is not supported at this voltage operating point.
21/ ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
22/ P = SYSCLK2 period.
23/ Parameters are characterized from -40°C to 105°C unless otherwise noted.
24/ This timing is limited by the timing shown or 2P, whichever is greater.

TABLE I. Electrical performance characteristics - Continued. 1/

25/ McASP0 ACLKXCTL.ASYNC = 1; Receiver is clocked by its own ACLKR0.
26/ McASP0 ACLKXCTL.ASYNC = 0; Receiver is clocked by transmitter's ACLKX0.
27/ McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
28/ AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
29/ A = (ACLKR/X period)/2 in ns. For example, when ACLKR/X period is 25 ns, use A = 12.5 ns.
30/ CLKRP = CLKXP =FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
31/ P = ASYNC3 period in ns. For example when the ASYNC clock domain is running at 100 MHz, use 10 ns.
32/ Use whichever value is greater. Minimum CLKR/X cycle time must be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
33/ This parameter applies to the maximum McBSP frequency. Operate serial clock (CLKR/X) in the reasonable range of 40/60 duty cycle.
34/ Minimum delay times also represent minimum output hold times.
35/ Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
36/ Use whichever value is greater.
37/ C = H or L.
S = Sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1)*S if CLKGDV is even
H = (CLKGDV +1)/2 * S if CKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV +1)/2 * S if CKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see 35/ above).
38/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 6P, D2 = 12P.
39/ Extra delay from FSX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 6P, D2 = 12P.
40/ P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period).
41/ This timing is limited by the timing shown or 3P, whichever is greater.
42/ First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI0_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI0_SOMI.
43/ P = SYSCLK2 period; S = $t_{c(SPC)S}$ (SPI slave bit clock period).
44/ First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI0_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI0_SIMO
45/ Measured from the termination of the write of new data to the SPI module. In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by the CPU.
46/ These parameters are in addition to the general timings for SPI master mode table.
47/ Figure shown only Polarity = 0, Phase = 0 as an example. Tables gives parameters for all four master clocking modes.
48/ In the case where the master SPI is ready with new data before $\overline{\text{SPI0_ENA}}$ assertion.
49/ In the case where the master SPI is ready with new data before $\overline{\text{SPI0_ENA}}$ deassertion.
50/ In the case where the master SPI is ready with new data before $\overline{\text{SPI0_SCS}}$ assertion.
51/ This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].

52/ Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, $\overline{\text{SPI0_SCS}}$ will remain asserted.
53/ If $\overline{\text{SPI0_ENA}}$ is asserted immediately such that the transmission is not delay by $\overline{\text{SPI0_ENA}}$.
54/ If $\overline{\text{SPI0_ENA}}$ was initial deasserted high and SPI0_CLK is delayed.
55/ C2TDELAY+P.
56/ These parameters are in addition to the general timings for SPI slave mode table.
57/ $\overline{\text{SPI0_ENA}}$ is driven low after the transmission completed if the SPINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.
58/ First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI1_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI1_SOMI.
59/ In the case where the master SPI is ready with new data before $\overline{\text{SPI1_ENA}}$ assertion.
60/ In the case where the master SPI is ready with new data before $\overline{\text{SPI1_ENA}}$ deassertion.
61/ In the case where the master SPI is ready with new data before $\overline{\text{SPI1_SCS}}$ assertion.
62/ This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
63/ Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, $\overline{\text{SPI1_SCS}}$ will remain asserted.
64/ If $\overline{\text{SPI1_ENA}}$ is asserted immediately such that the transmission is not delay by $\overline{\text{SPI1_ENA}}$.
65/ If $\overline{\text{SPI1_ENA}}$ was initial deasserted high and SPI1_CLK is delayed.
66/ $\overline{\text{SPI1_ENA}}$ is driven low after the transmission completed if the SPINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.
67/ I2C must be configured correctly to meet the timings in this table.
68/ U = UART baud time = 1/programmed baud rate.
69/ D = UART input clock in MHz
For UART, the UART input clock is SYSCLK2.
For UART1 or UART2, the UART input clock is ASYNC3 (either PLL0_SYSCLK2 or PLL1_SYSCLK2).
70/ E = UART divisor x UART sampling rate. The UART divisor is set through the UART divisor latch register (DLL and DLH). The UART sampling rate is set through the over-sampling mode select bit (OSM_SEL) of the UART mode definition register (MDR).
71/ Baud rate is not indicative of data rate. Actual data rate will be limited by system factors such as EDMA loading, EMIF/DDR loading system frequency, etc.
72/ Low speed: $C_L$ = 200 pF, Full speed: $C_L$ = 50 pF, High speed: $C_L$ = 50 pF.
73/ $t_{RFM} = (t_r/t_f) \times 100$. (Excluding the first transition from the Idle state).
74/ For more detail information, see manufacture data.
75/ $t_{jr} = t_{px(1)} - t_{px(0)}$
76/ $f_{op} = 1/t_{per}$
77/ Receive selected signals include: MII_RXD[3]-MII_RXD[0], MII_RXDV, and MII_RXER.
78/ Transmit selected signals include: MTXD3-MTXD0, and MII_TXEN
79/ RMII is not supported at operating points below 1.1 V nominal.
80/ $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and:[NOT ($\overline{\text{UHPI_HDS1}}$ XOR $\overline{\text{UHPI_HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.
81/ M = SYSCLK2 period in ns.
82/ Select signals include: HCNTLI[1:0], HR/$\overline{\text{W}}$ and HHWIL.
83/ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and$\overline{\text{HDS2}}$:[NOT ($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$
84/ By design, $\overline{\text{HCS}}$, is driven inactive (high), HPI will drive $\overline{\text{HRDY}}$ active (low).

85/ **For HPI Write**. $\overline{\text{HRDY}}$ can go high (not ready) for these HPI Write conditions; otherwise, $\overline{\text{HRDY}}$ stays low (ready):
Case 1: Back to back HPIA writes (can be either first or second half word)
Case 2: HPIA write following a **PERFETCH** command (can be either first or second half word)
Case 3: HPIA write when FIFO is full or flushing (can be either first or second half word)
Case 4: HPIA write and Write FIFO not empty.
**For HPI Read**. $\overline{\text{HRDY}}$ can go high (not ready) for these HPI Read conditions:
Case 1: HPID read (with auto increment) and data not in Read FIFO (can only happen to first half word of HPID access)
Case 2: First half word access of HPID Read without auto increment.
**For HPID Read**, $\overline{\text{HRDY}}$ stays low (ready) for these HPI Read conditions:
Case 1: HPID read with auto increment and data is already in Read FIFO (applies to either half word of HPID access)
Case 2: HPID read without auto increment and data is already in Read FIFO (always applies to second half word of HPID access)
Case 3: HPIC or HPIA read (applies to either half word access)

86/ **For HPI Read**. Applies to conditions where data is already residing in HPID/FIFO:
Case 1: HPIC or HPIA read
Case 2: First half word of HPID read with auto increment and data is already in Read FIFO
Case 3: Second half word of HPID read with or without auto increment

87/ **For HPI Write**. $\overline{\text{HRDY}}$ can go high (not ready) for these HPI Write conditions; otherwise, $\overline{\text{HRDY}}$ stays low (ready):
Case 1: HPID write when Write FIFO is full (can happen to either half word)
Case 2: HPIA write (can happen to either half word)
Case 3: HPID write without auto increment (only happens to second half word)

88/ 2xTXCLK is an alternate transmit clock source that must be at least 2 times the required µPP transmit clock rate (as it is divided down by 2 inside the µPP). 2xTXCLK has no specified skew relationship to the CHn_CLOCK and therefore is not shown in the timing diagram.

89/ C = VP_CLKINx period in ns

90/ C = VP_CLKO2/3period in ns

91/ MEP step size will increase with low voltage and high temperature and decrease with high voltage and cold temperature.

92/ P = OSCIN cycle time in ns.

93/ C = TM64P0_IN12 cycle time in ns.

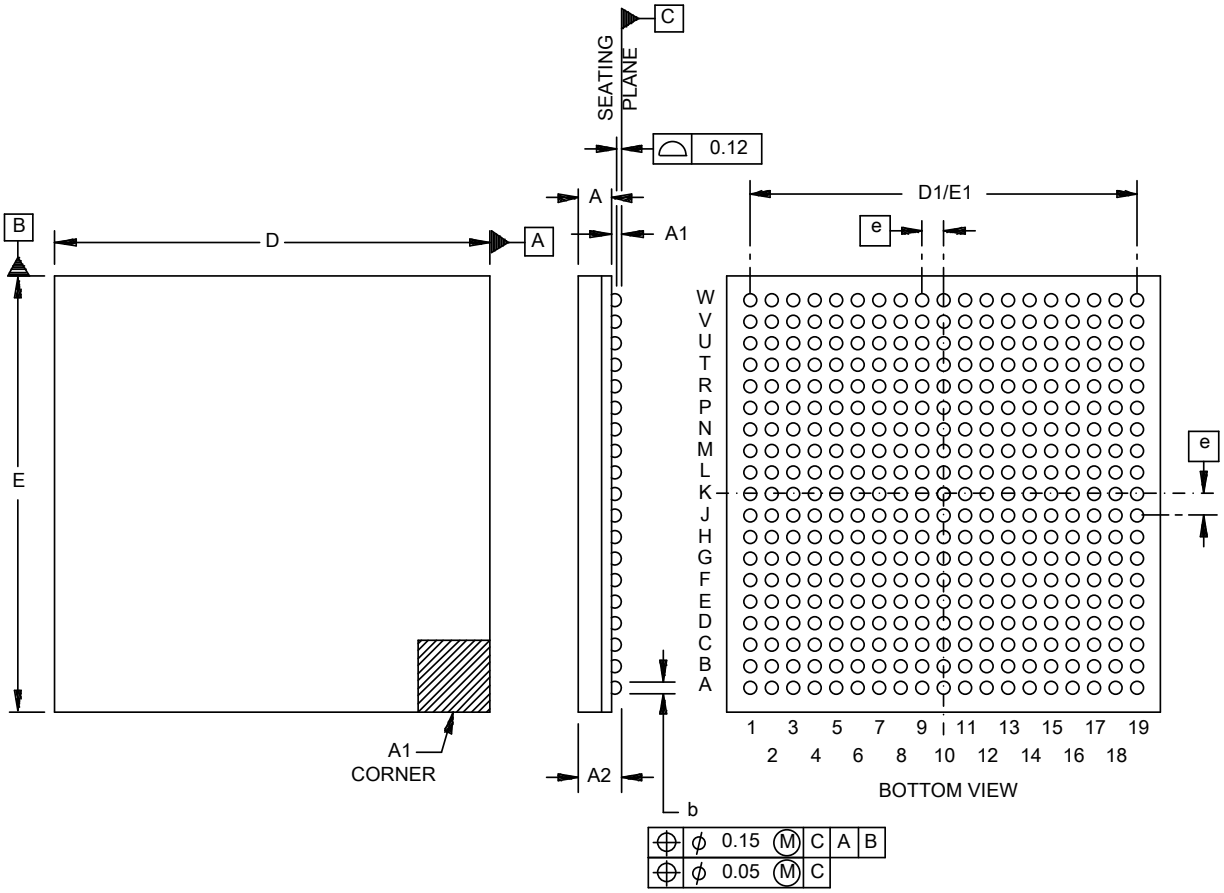
94/ Whichever is smaller, P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

95/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to allow the device enough time to access the GPIO register through the internal bus.

96/ C = SYSCLK4 period in ns.

97/ These parameters are not production tested and are specified by design to work from -40°C to 125°C.

Case X




| Dimensions | | | | | |
|---|---|---|---|---|---|
| Symbol | Millimeters | | Symbol | Millimeters | |
| | Min | Max | | Min | Max |
| A | 0.84 | 0.95 | D/E | 15.90 | 16.10 |
| A1 | 0.35 | 0.45 | D1/E1 | 14.40 TYP | |
| A2 | 1.19 | 1.40 | e | 0.80 BSC | |
| b | 0.45 | 0.55 | | | |

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.
4. Falls within JEDEC MO-275.

FIGURE 1. Case outlines.

Case X

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| W | VP_DOUT[0]/ LCD_D[0]/ UPP_XD[8]/ GP7[8]/ PRU1_R31[8] | VP_DOUT[13]/ LCD_D[13]/ UPP_XD[5]/ GP7[5]/ PRU1_R31[9] | VP_DOUT[2]/ LCD_D[2]/ UPP_XD[10]/ GP7[10]/ PRU1_R31[10] | DDR_A[10] | DDR_A[6] | DDR_A[2] | $\overline{\text{DDR_CLKN}}$ | DDR_CLKP | $\overline{\text{DDR_RAS}}$ | DDR_D[15] | W |
| V | VP_DOUT[3]/ LCD_D[113]/ UPP_XD[11]/ GP7[11]/ PRU1_R31[11] | VP_DOUT[4]/ LCD_D[4]/ UPP_XD[12]/ GP7[12]/ PRU1_R31[12] | VP_DOUT[5]/ LCD_D[5]/ UPP_XD[13]/ GP7[13]/ PRU1_R31[13] | DDR_A[12] | DDR_A[5] | DDR_A[3] | DDR_CKE | DDR_BA[0] | $\overline{\text{DDR_CS}}$ | DDR_D[13] | V |
| U | VP_DOUT[6]/ LCD_D[6]/ UPP_XD[14]/ GP7[14]/ PRU1_R31[14] | VP_DOUT[7]/ LCD_D[7]/ UPP_XD[15]/ GP7[15]/ PRU1_R31[15] | VP_DOUT[8]/ LCD_D[8]/ UPP_XD[0]/ GP7[0]/ BOOT[0] | DDR_A[8] | DDR_A[4] | DDR_A[7] | DDR_A[0] | DDR_BA[2] | $\overline{\text{DDR_CAS}}$ | DDR_D[12] | U |
| T | VP_DOUT9]/ LCD_D[9]/ UPP_XD[1]/ GP7[1]/ BOOT[1] | VP_DOUT[10]/ LCD_D[10]/ UPP_XD[2]/ GP7[2]/ BOOT[2] | VP_DOUT[11]/ LCD_D[11]/ UPP_XD[3]/ GP7[3]/ BOOT[3] | DDR_A[11] | DDR_A[13] | DDR_A[9] | DDR_A[1] | $\overline{\text{DDR_WE}}$ | DDR_BA[1] | DDR_D[10] | T |
| R | VP_DOUT[12]/ LCD_D[12]/ UPP_XD[4]/ GP7[4]/ BOOT[4] | VP_DOUT[13]/ LCD_D[13]/ UPP_XD[5]/ GP7[5]/ BOOT[5] | VP_DOUT[14]/ LCD_D[14]/ UPP_XD[6]/ GP7[6]/ BOOT[6] | DVDD3318_C | $\overline{\text{LCD_AC_ENB_CS}}$/ GP6[0]/ PRU1_R31[28] | DDR_VREF | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | DDR_DQM[1] | R |
| P | SATA_VDD | SATA_VDD | SATA_VDDR | VP_DOUT[15]/ LCD_D[15]/ UPP_XD[7]/ GP7[7]/ BOOT[7] | DVDD3318_C | DVDD3318_C | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | P |
| N | $\overline{\text{SATA_REFCLKN}}$ | SATA_REFCLKP | SATA_REQ | SATA_VDD | VSS | DDR_DVDD18 | RVDD | CVDD | DDR_DVDD18 | DDR_DVDD18 | N |
| M | SATA_VSS | SATA_VDD | NC | VSS | VSS | VSS | VSS | CVDD | CVDD | VSS | M |
| L | SATA_RXP | $\overline{\text{SATA_RXN}}$ | SATA_VSS | DVDD3318_C | VSS | DVDD18 | VSS | VSS | VSS | VSS | L |
| K | SATA_VSS | SATA_VSS | VP_CLKOUT2/ MMCSD1_DAT[2]/ PRU1_R30[2]/ GP6[3]/ PRU1_R31[3] | VP_CLKOUT3/ PRU1_R30[0]/ GP6[1]/ PRU1_R31[1] | DVDD18 | CVDD | VSS | VSS | VSS | VSS | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

FIGURE 2. Terminal connections.

| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|---|---|---|---|---|---|---|---|---|---|---|
| W | DDR_D[7] | DDR_D[6] | DDR_DQM[0] | VP_CLKIN0/ UHPI_HCS/ PRU1_R30[10]/ GP6[7]/ UPP_2xTXCLK | PRU0_R30[28]/ UHPI_HCNTL1/ UPP_CHA_START/ GP6[10] | VP_DIN[4]/ UHPI_HD[12]/ UPP_D[12]/ RMII_RXD[1]/ PRU0_R31[26] | VP_DIN[2]/ UHPI_HD[10]/ UPP_D[10]/ RMII_RXER/ PRU0_R31[24] | VP_DIN[1]/ UHPI_HD[9]/ UPP_D[9]/ RMII_MHZ_50/ CLK_ PRU0_R31[23] | VP_DIN[0]/ UHPI_HD[8]/ UPP_D[8]/ RMII_CRS_DV/ PRU1_R31[29] | W |
| V | DDR_DQS[1] | DDR_D[5] | DDR_D[4] | DDR_D[2] | VP_CLKIN1/ UHPI_HDS1/ PRU1_R30[9]/ GP6[6]/ PRU1_R31[16] | VP_DIN[6]/ UHPI_HD[14]/ UPP_D[14]/ RMII_TXD[0]/ PRU0_R31[28] | VP_DIN[3]/ UHPI_HD[11]/ UPP_D[11]/ RMII_RXD[0]/ PRU0_R31[25] | VP_DIN[15]/ VSYNC/ UHPI_HD[7]/ RMII_TXD[7]/ PRU0_R30[15]/ PRU0_R31[15] | VP_DIN[14]/ HSYNC/ UHPI_HD[6]/ UPP_D[6]/ PRU0_R30[14]/ PRU0_R31[14] | V |
| U | DDR_D[14] | DDR_ZP | DDR_D[3] | DDR_D[1] | DDR_D[0] | PRU0_R30[27]/ UHPI_HHWIL/ UPP_CHA _ENABLE/ GP6[9] | PRU0_R30[29]/ UHPI_HCNTL0/ UPP_CHA_CLOCK/ GP6[11] | VP_DIN[7]/ UHPI_HD[15]/ UPP_D[15]/ RMII_TXD[1]/ PRU0_R31[29] | VP_DIN[13]/ FIELD/ UHPI_HD[5]/ UPP_D[5]/ PRU0_R30[13]/ PRU0_R31[13] | U |
| T | DDR_D[9] | DDR_D[11] | DDR_D[8] | DDR_DQS[0] | PRU0_R30[26]/ UHPI_HRW/ UPP_CHA_WAIT/ GP6[8] PRU1_R31[17] | VP_DIN[12]/ UHPI_HD[4]/ UPP_D[4]/ PRU0_R30[12]/ PRU0_R31[12] | RESETOUT/ UHPI_HAS/ PRU1_R30[14]/ GP6[15] | CLKOUT/ UHPI_HDS2/ PRU1_R30[13]/ GP6[14] | RSV2 | T |
| R | DDR_DQGATE0 | DDR_DQGATE1 | DVDD18 | VP_DIN[5]/ UHPI_HD[13]/ UPP_D[13]/ RMII_TXEN/ PRU0_R31[27] | VP_DIN[9]/ UHPI_HD[1]/ UPP_D[1]/ PRU0_R30[9]/ PRU0_R31[9] | PRU0_R30[30]/ UHPI_HINT/ PRU1_R30[11]/ GP6[12] | PRU0_R30[31]/ UHPI_HRDY/ PRU1_R30[12]/ GP6[13] | VP_DIN[11]/ UHPI_HD[3]/ UPP_D[3]/ PRU0_R30[11]/ PRU0_R31[11] | VP_DIN[10]/ UHPI_HD[2]/ UPP_D[2]/ PRU0_R30[10]/ PRU0_R31[10] | R |
| P | VSS | DVDD3318_C | DVDD18 | USB1_VDDA18 | USB1_VDDA33 | USB0_ID | VP_DIN[8]/ UHPI_HD[D]/ UPP_D[0]/ GP6[5]/ PRU1_R31[0] | USB1_DM | USB1_DP | P |
| N | VSS | VSS | DVDD3318_C | USB0_VDDA18 | PLL1_VDDA | NC | USB0_VDDA12 | USB0_VDDA33 | USB0_VBUS | N |
| M | VSS | USB_CVDD | DVDD3318_C | NC | PLL1_VSSA | TD1 | PLL0_VSSA | USB0_DM | USB0_DP | M |
| L | VSS | CVDD | DVDD3318_C | RTC_CVDD | PLL0_VDDA | TMS | TRST | OSCVSS | OSCIN | L |
| K | VSS | CVDD | DVDD3318_C | RESET | DVDD3318_B | EMU1 | RTCK/ GP8[0] | USB0_DRVVBUS | OSCOUT | K |
| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

FIGURE 2. Terminal connections - Continued.

| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|---|---|---|---|---|---|---|---|---|---|---|
| J | VSS | CVDD | DVDD18 | DVDD3318_B | TCK | EMU0 | NMI | TDO | RTC_XI | J |
| H | CVDD | CVDD | CVDD | RVDD | VSS | SPI1_ENA/ GP2[12] | SPI1_SOMI/ GP2[11] | RTC_VSS | RTC_XO | H |
| G | DVDD18 | DVDD18 | CVDD | DVDD3318_A | DVDD3318_A | SPI1_SCS[7]/ I2C0_SCL/ TM64P2_OUT12/ GP1[5] | SPI1_SIMO/ GP2[10] | SPI1_SCS[6]/ I2C0_SDA/ TM64P3_OUT12/ GP1[4] | SPI1_CLK/ GP2[13] | G |
| F | DVDD3318_B | DVDD3318_B | DVDD3318_B | DVDD18 | DVDD3318_A | SPI1_SCS[4]/ UART2_TXD/ I2C1SDA/ GP1[2] | SPI1_SCS[5]/ UART2_RXD/ I2C1_SCL/ GP1[3] | SPI1_SCS[1]/ EPWM1A/ PRU0_R30[8]/ GP2[15] TM64P2_IN12 | SPI1_SCS[2]/ UART1_TXD/ SATA_CP_POD/ GP1[0] | F |
| E | EMA_A[18]/ MMCSD0_DAT[3]/ PRU1_R30[26]/ GP4[2] | EMA_A[16]/ MMCSD0_DAT[5]/ PRU1_R30[24]/ GP4[0] | EMA_A[6]/ GP5[6] | DVDD3318_B | CVDD | SPI0_SCS[1]/ TM64P0_OUT12/ GP1[7]/ MDIO_CLK/ TM64P0_IN12 | SPI0_SCS[3]/ UART0_CTS/ GP8[2]/ MII_RXD[1]/ SATA_MP_SWITCH | SPI1_SCS[3]/ UART1_RXD/ SATA_LED/ GP1[1] | SPI1_SCS[0]/ EPWM1B/ PRU0_R30[7]/ GP2[14]/ TM64P3_IN12 | E |
| D | EMA_A[13]/ PRU0_R30[21]/ PRU1_R30[21]/ GP5[13]/ PRU1_R31[21] | EMA_A[9]/ PRU1_R30[17]/ GP5[9] | EMA_A[12]/ PRU1_R30[20]/ GP5[12]/ PRU1_R31[20] | EMA_A[3]/ GP5[3] | EMA_A[1]/ GP5[1] | SPI0_SCS[2]/ UART0_RTS/ GP8[1]/ MII_RXD[0]/ SATA_CP_DET | SPI0_SCS[0]/ TM64P1_OUT12/ MDIO_D/ TM64P1_IN12 | SPI0_SCS[4]/ UART0_TXD/ GP8[3]/ MII_RXD[2] | SPI0_CLK/ EPWM0A/ GP1[8]/ MII_RXCLK | D |
| C | EMA_A[15]/ MMCSD0_DAT[6]/ PRU1_R30[23]/ GP5[15]/ PRU1_R31[23] | EMA_A[10]/ PRU1_R30[18]/ GP5[10]/ PRU1_R31[18] | EMA_A[5]/ GP5[5] | EMA_A[0]/ GP5[0] | EMA_BA[0]/ GP2[8] | SPI0_SOMI/ EPWMSYNCI/ GP8[6]/ MII_RXER | SPI0_ENA/ EPWM0B/ PRU0_R30[6]/ MII_RXDV | SPI0_SIMO/ EPWMSYNCO/ GP8[5]/ MII_CRS | SPI0_SCS[5]/ UART0_RXD/ GP8[4]/ MII_RXD[3] | C |
| B | EMA_A[17]/ MMCSD0_DAT[4]/ PRU1_R30[25] GP4[1]/ | EMA_A[11]/ PRU1_R30[19]/ GP5[11]/ PRU1_R31[19] | EMA_A[7]/ PRU1_R30[15]/ GP5[7] | EMA_A[2]/ GP5[2] | EMA_OE/ GP3[10] | EMA_CS[5]/ GP3[12] | EMA_CS[2]/ GP3[15] | EMA_WAIT[0]/ PRU0_R30[0]/ GP3[8]/ PRU0_R31[0] | EMA_WAIT[1]/ PRU0_R30[1]/ GP2[1]/ PRU0_R31[1] | B |
| A | EMA_A[20]/ MMCSD0_DAT[1]/ PRU1_R30[28] GP4[4]/ | EMA_A[14]/ MMCSD0_DAT[7]/ PRU1_R30[22]/ GP5[14]/ PRU1_R31[22] | EMA_A[8]/ PRU1_R30[16]/ GP5[8] | EMA_A[4]/ GP5[4] | EMA_BA[1]/ GP2[9] | EMA_RAS/ PRU0_R30[3]/ GP2[5]/ PRU0_R31[3] | EMA_CS[3]/ GP3[14] | EMA_CS[0]/ GP2[0] | VSS | A |
| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

FIGURE 2. Terminal connections - Continued.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| J | SATA_TXP | SATA_TXN | VP_CLKIN3/ MMCSD1_DAT[1]/ PRU1_R30[1]/ GP6[2]/ PRU1_R31[2] | PRU0_R30[23]/ MMCSD1_CMD/ UPP_CHB_ENABLE/ GP8[13]/ PRU1_R31[25] | DVDD3318_C | CVDD | VSS | VSS | VSS | VSS | J |
| H | SATA_VSS | SATA_VSS | VP_CLKIN2/ MMCSD1_DAT[3]/ PRU1_R30[3]/ GP6[4]/ PRU1_R31[4] | MMCSD1_DAT[5]/ LCD_HSYNC/ PRU1_R30[5]/ GP8[9]/ PRU1_R31[6] | DVDD3318_A | CVDD | CVDD | VSS | VSS | CVDD | H |
| G | PRU0_R30[25]/ MMCSD1_DAT[0]/ UPP_CHB_CLOCK/ GP8[15]/ PRU1_R31[27] | PRU0_R30[24]/ MMCSD1_CLK/ UPP_CHB_START/ GP8[14]/ PRU1_R31[26] | PRU0_R30[22]/ PRU1_R30[8]/ UPP_CHB_WAIT/ GP8[12]/ PRU1_R31[24] | MMCSD1_DAT[4]/ LCD_VSYNC/ PRU1_R30[4]/ GP8[8]/ PRU1_R31[5] | DVDD3318_A | DVDD18 | CVDD | CVDD | DVDD3318_B | DVDD18 | G |
| F | MMCSD1_DAT[7]/ LCD_PCLK/ PRU1_R30[7]/ GP8[11]/ | MMCSD1_DAT[6]/ LCD_MCLK/ PRU1_R30[6]/ GP8[10]/ PRU1_R31[7] | AXR0/ ECAP0_APWM0/ GP8[7]/ MII_TXD[0]/ CLKSO | RTC ALARM/ UART2_CTS/ GP0[8]/ DEEPSLEEP | DVDD3318_A | DVDD3318_B | DVDD3318_B | DVDD3318_B | EMA_CS[4]/ GP3[13] | DVDD3318_B | F |
| E | AXR1/ DX0/ GP1[9]/ MII_TXD[1] | AXR2/ DX0/ GP1[10]/ MII_TXD[2] | AXR3/ FSX0/ GP1[11]/ MII_TXD[3] | AXR8/ CLKS1 ECAP1_APWM1/ GP0[0]/ PRU0_R31[8] | RVDD | EMA_D[15]/ GP3[7] | EMA_D[5]/ GP4[13] | EMA_D[3]/ GP4[11] | MMCSD0_CLK/ PRU1_R30[31]/ GP4[7] | EMA_D[8]/ GP3[0] | E |
| D | AXR4/ FSR0/ GP1[12]/ MII_COL | AXR7/ EPWM1TZ[0]/ PRU0_R30[17] GP1[15]/ PRU0_R31[7] | AXR5/ CLKX0/ GP1[13]/ MII_TXCLK | AXR10/ DR1/ GP0[2] | AMUTE/ PRU0_R30[16]/ UART2_RTS/ GP0[9]/ PRU0_R31[16] | EMA_D[11]/ GP3[3] | EMA_D[7]/ GP4[15] | EMA_SOCKE/ PRU0_R30[4]/ GP2[6]/ PRU0_R31[4] | EMA_D[9]/ GP3[1] | EMA_A_RW/ GP3[9] | D |
| C | AXR6/ CLKR0/ GP1[14]/ MII_TXEN/ PRU0_R31[6] | AFSR/ GP0[13]/ PRU0_R31[20] | AXR9/ DX1/ GP0[1] | AXR12/ FSR1/ GP0[4] | AXR11/ FSX1/ GP0[3] | EMA_D[6]/ GP4[14] | EMA_D[14]/ GP3[6] | EMA_WEN_DQM[0]/ GP2[3] | EMA_D[0]/ GP4[8] | EMA_A[19]/ MMCSD0_DAT[2]/ PRU1_R30[27]/ GP4[3] | C |
| B | ACLKX/ PRU0_R30[19]/ GP0[14]/ PRU0_R31[21] | AFSX/ GP0[12]/ PRU0_R31[19] | AXR13/ CLKX1/ GP0[5] | AXR14/ CLKR1/ GP0[6] | EMA_D[4]/ GP4[12] | EMA_D[13]/ GP3[5] | EMA_CLK/ PRU0_R30[5]/ GP2[7]/ PRU0_R31[5] | EMA_D[2]/ GP4[10] | EMA_WE/ GP3[11] | EMA_A[21]/ MMCSD0_DAT[0]/ PRU1_R30[29]/ GP4[5] | B |
| A | ACLKR/ PRU0_R30[20]/ GP0[15]/ PRU0_R31[22] | AHCLKR/ PRU0_R30[18]/ UART1_RTS/ GP0[11]/ PRU0_R31[18] | AHCLKX/ USB_REFCLKIN/ UART1_CTS/ GP0[10]/ PRU0_R31[17] | AXR15/ EPWM0TZ[0]/ ECAP2_APWM2/ GP0[7] | EMA_WEN_DQM[1]/ GP2[2] | EMA_D[12]/ GP3[4] | EMA_D[10]/ GP3[2] | EMA_D[1]/ GP4[9] | EMA_CAS/ PRU0_R30[2]/ GP2[4] PRU0_R31[2] | EMA_A[22]/ MMCSD0_CMD/ PRU1_R30[30]/ GP4[6] | A |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

FIGURE 2. Terminal connections - Continued.

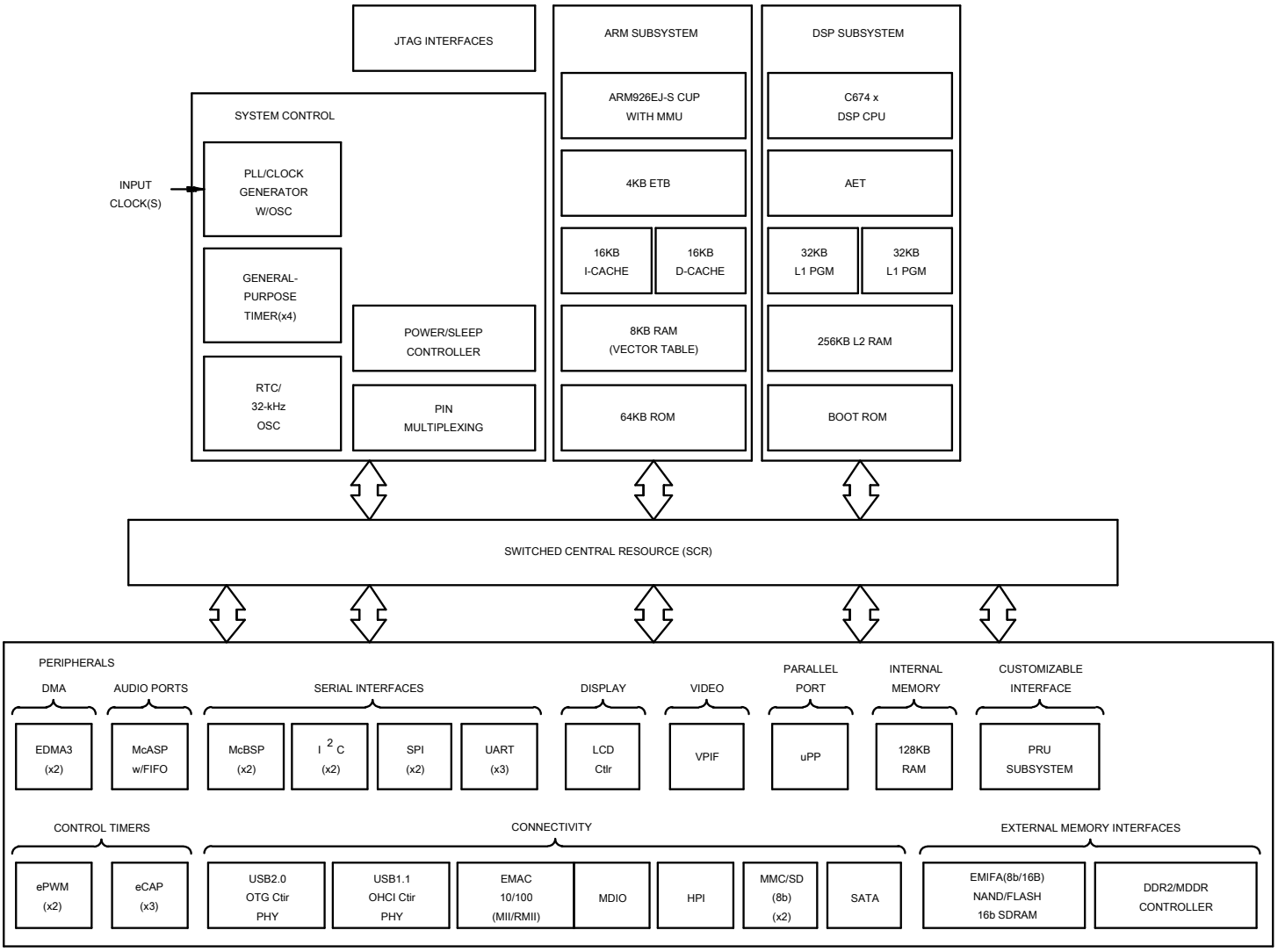



FIGURE 3. Functional block diagram.

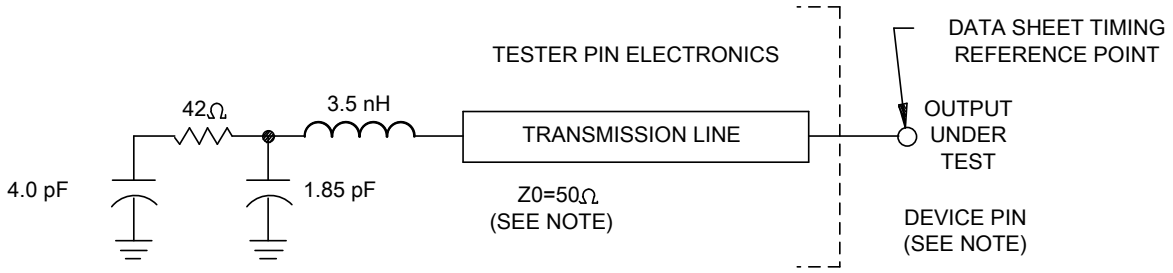



FIGURE 4. Test load circuit for AC timing measurements.

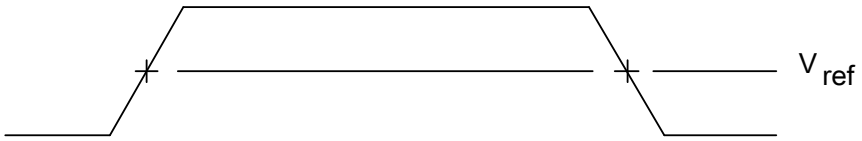



FIGURE 5. Input and Output voltage reference levels for AC timing measurements.

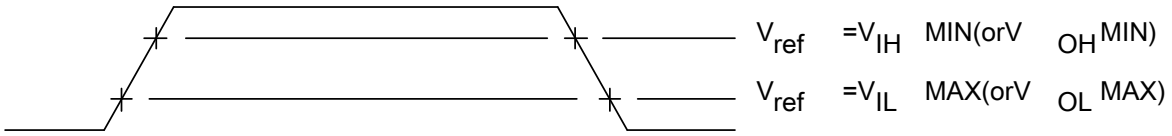



FIGURE 6. Rise and Fall transaction time voltage reference levels.

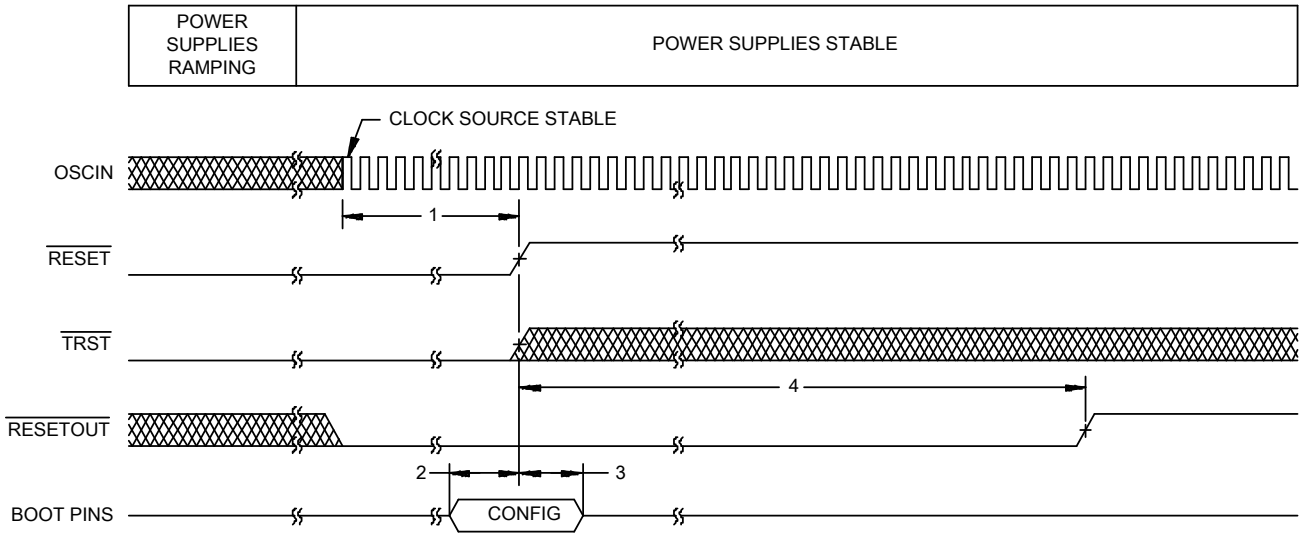



FIGURE 7. Power ON reset (RESET and TRST active) timing.

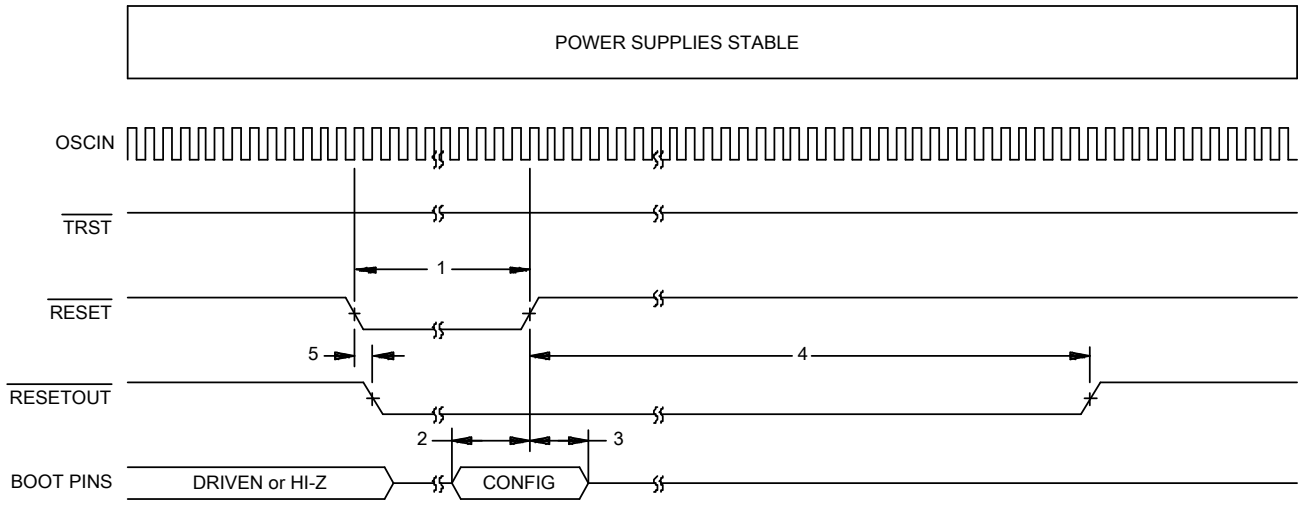



FIGURE 8. Warm Reset (RESET active, TRST high) Timing.

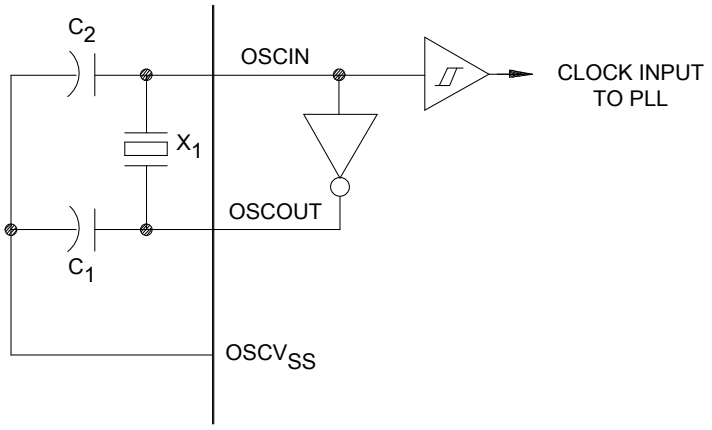



FIGURE 9. Oscillator timing requirements.

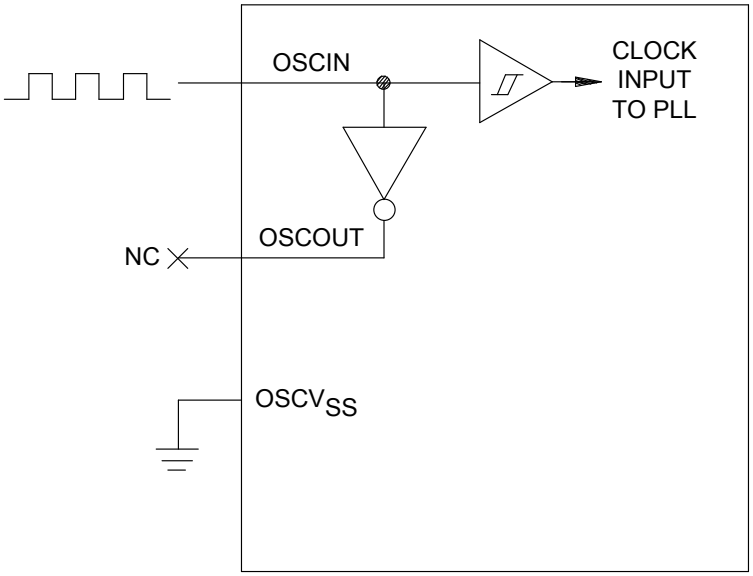



FIGURE 10. External 1.2 V clock source.

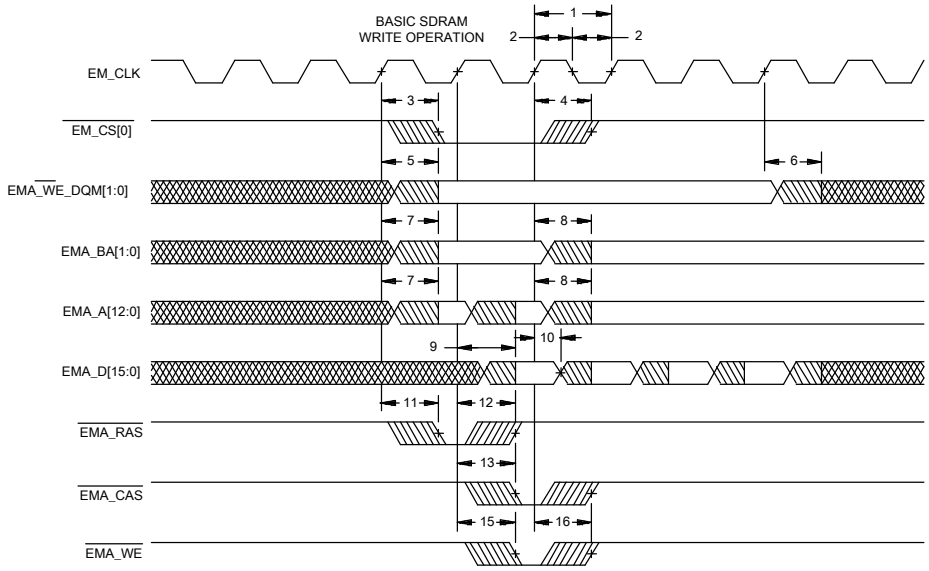



FIGURE 11. EMIFA basic SDRAM Write operation.

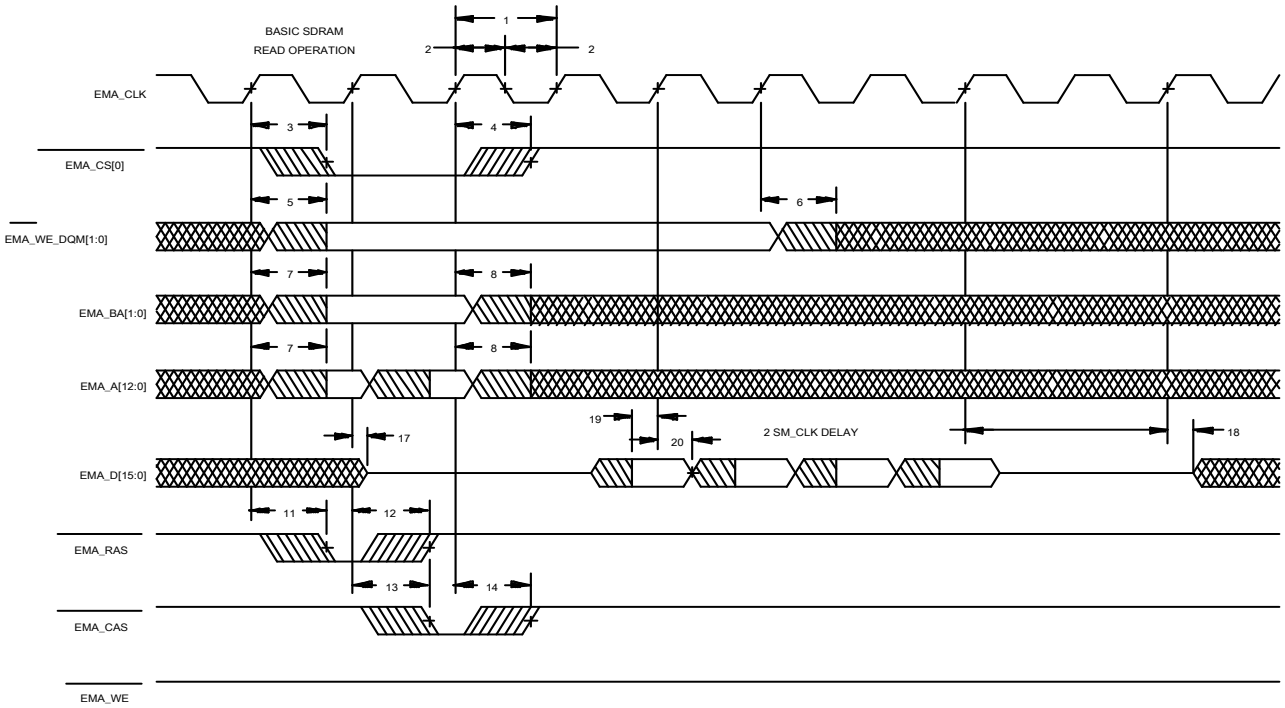



FIGURE 12. EMIFA basic SDRAM Read operation.

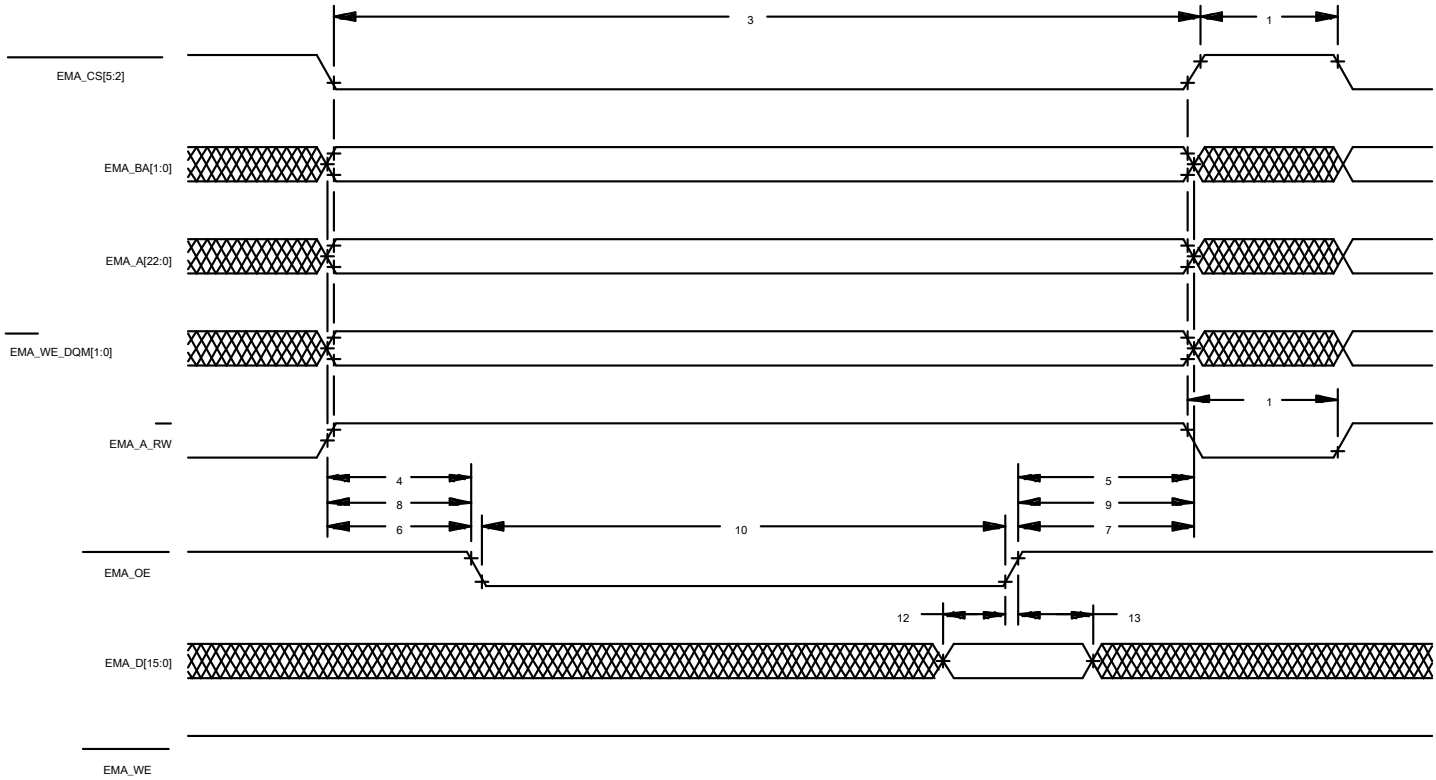



FIGURE 13. Asynchronous Memory Read timing for EMIFA.

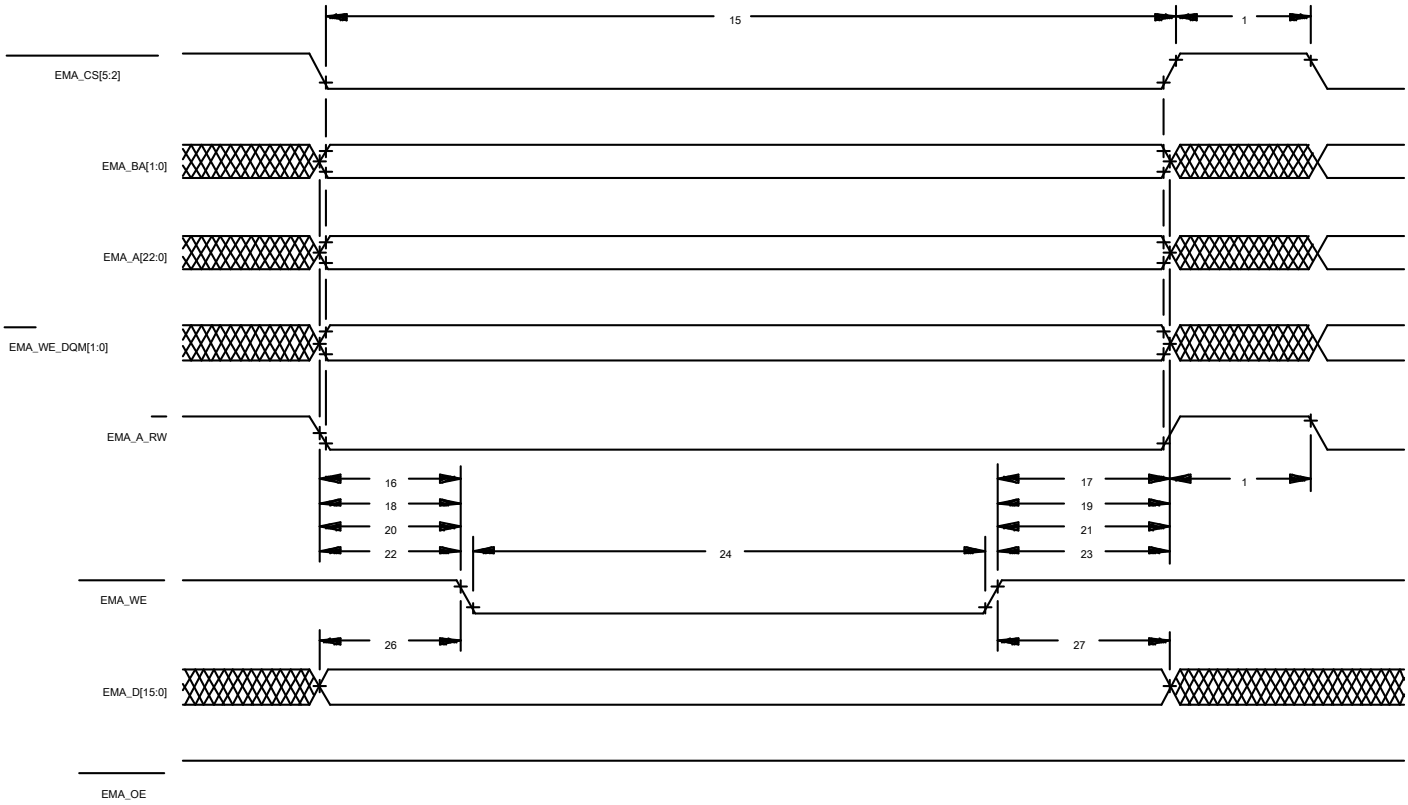



FIGURE 14. Asynchronous Memory Write timing for EMIFA.

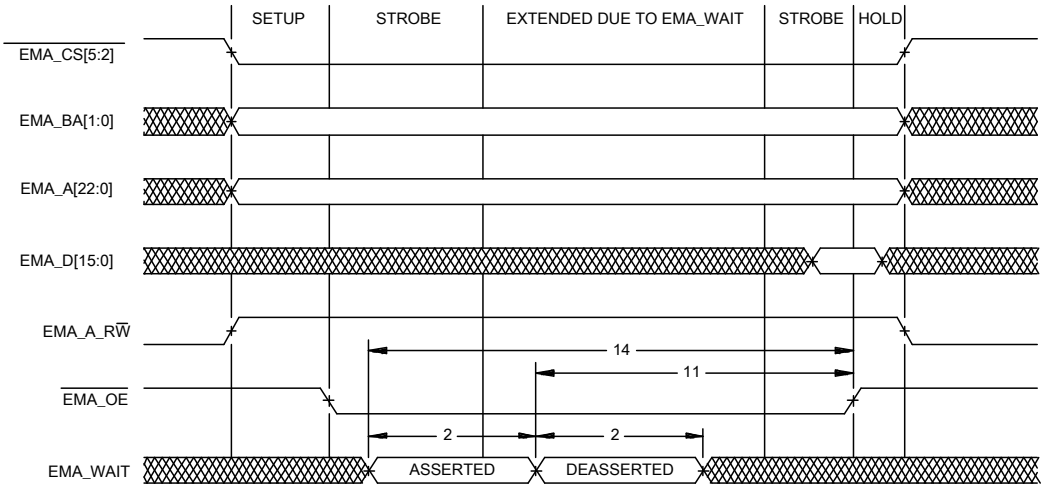



FIGURE 15. EMA_WAIT Read timing requirements.

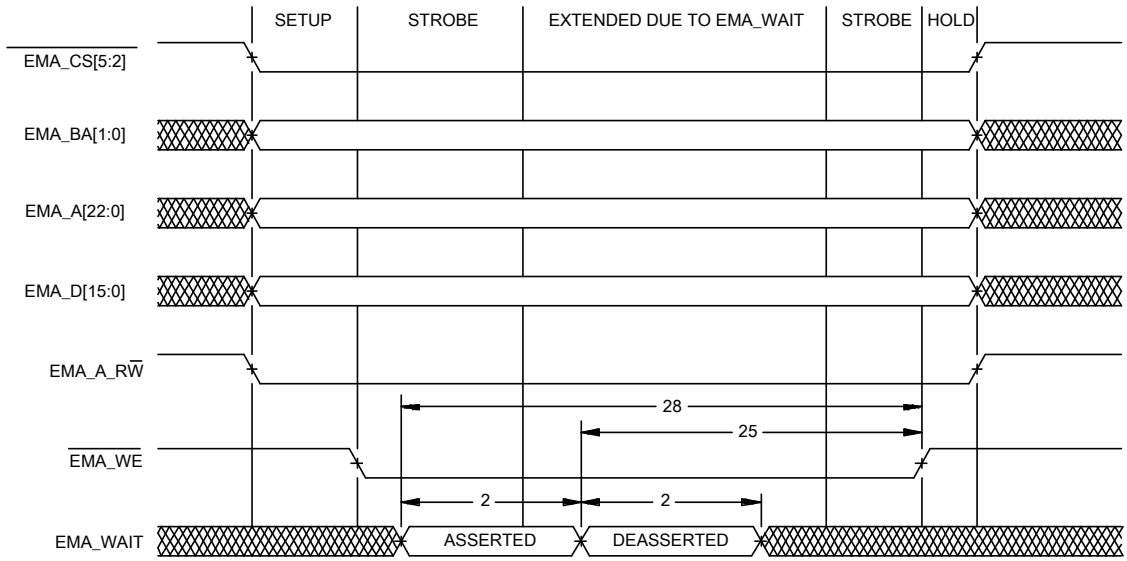



FIGURE 16. EMA_WAIT Write timing requirements.

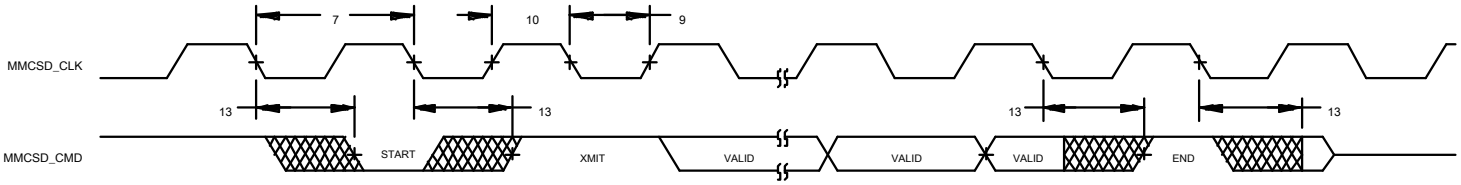



FIGURE 17. MMC/SD Host command timing.

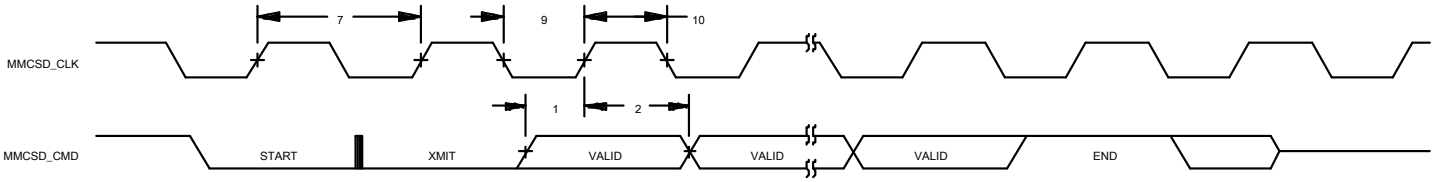



FIGURE 18. MMC/SD Card response timing.

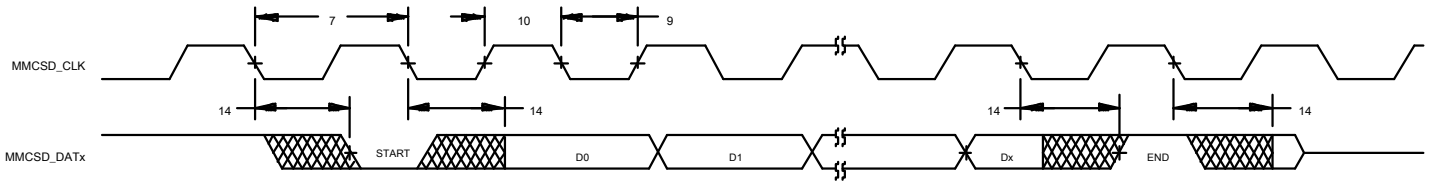



FIGURE 19. MMC/SD Host Write timing.

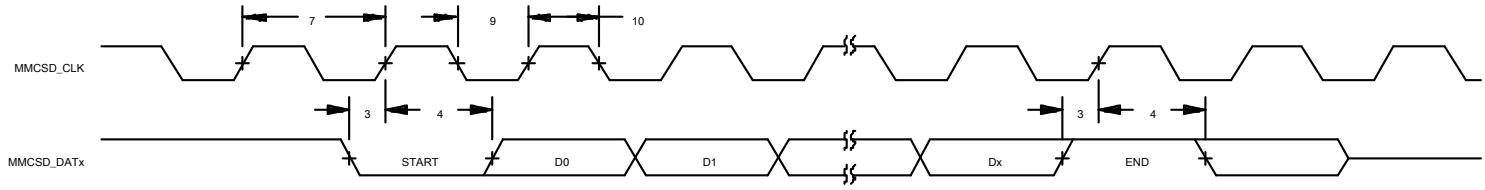



FIGURE 20. MMC/SD Host Read and Card Status timing.

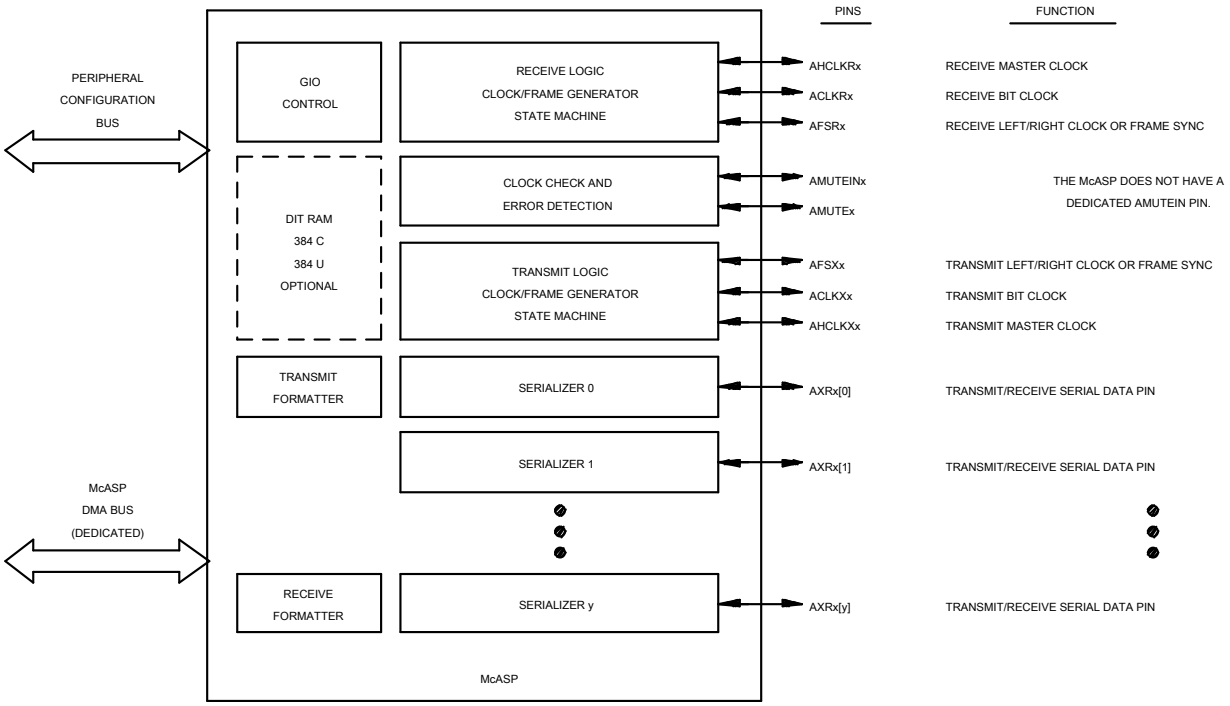
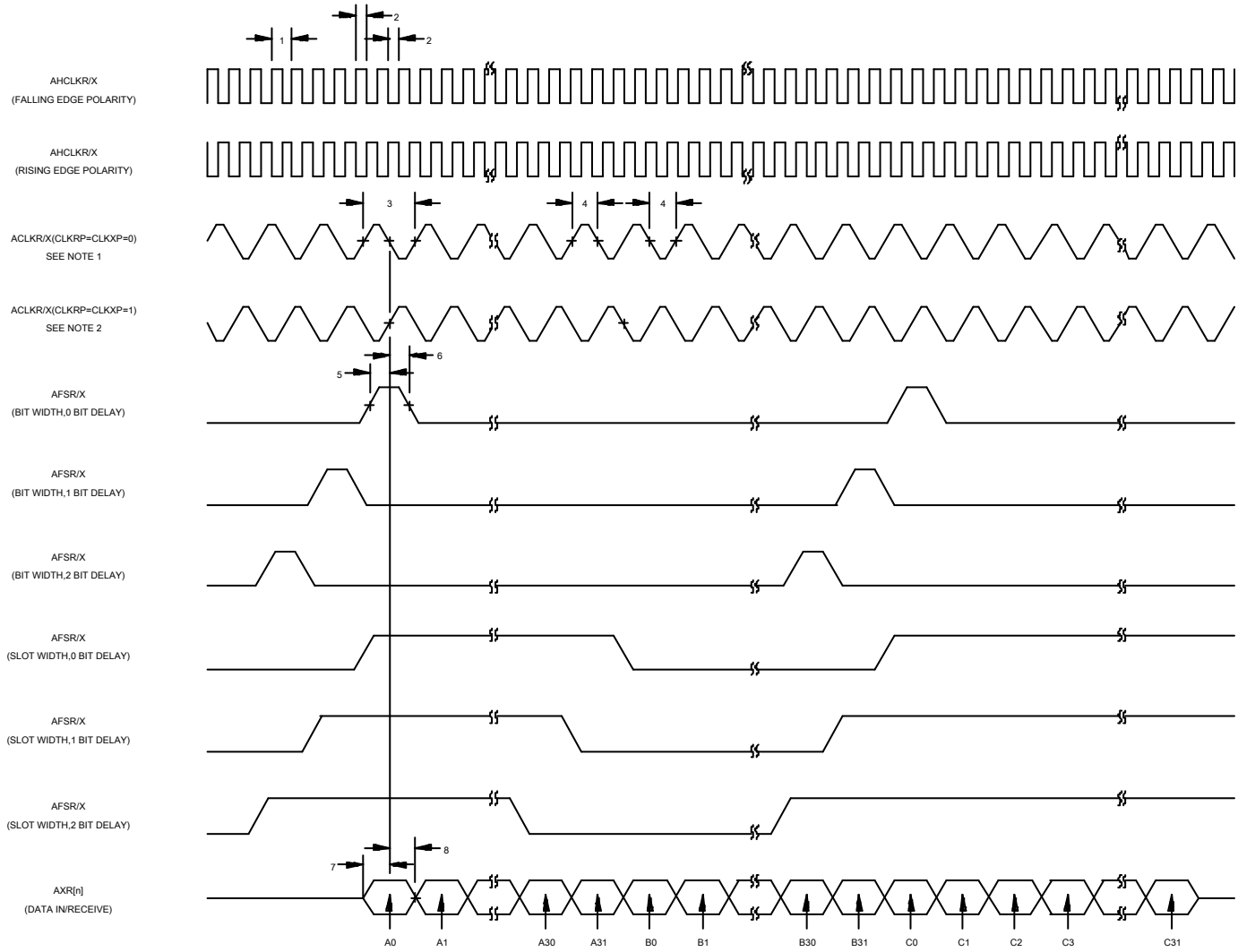


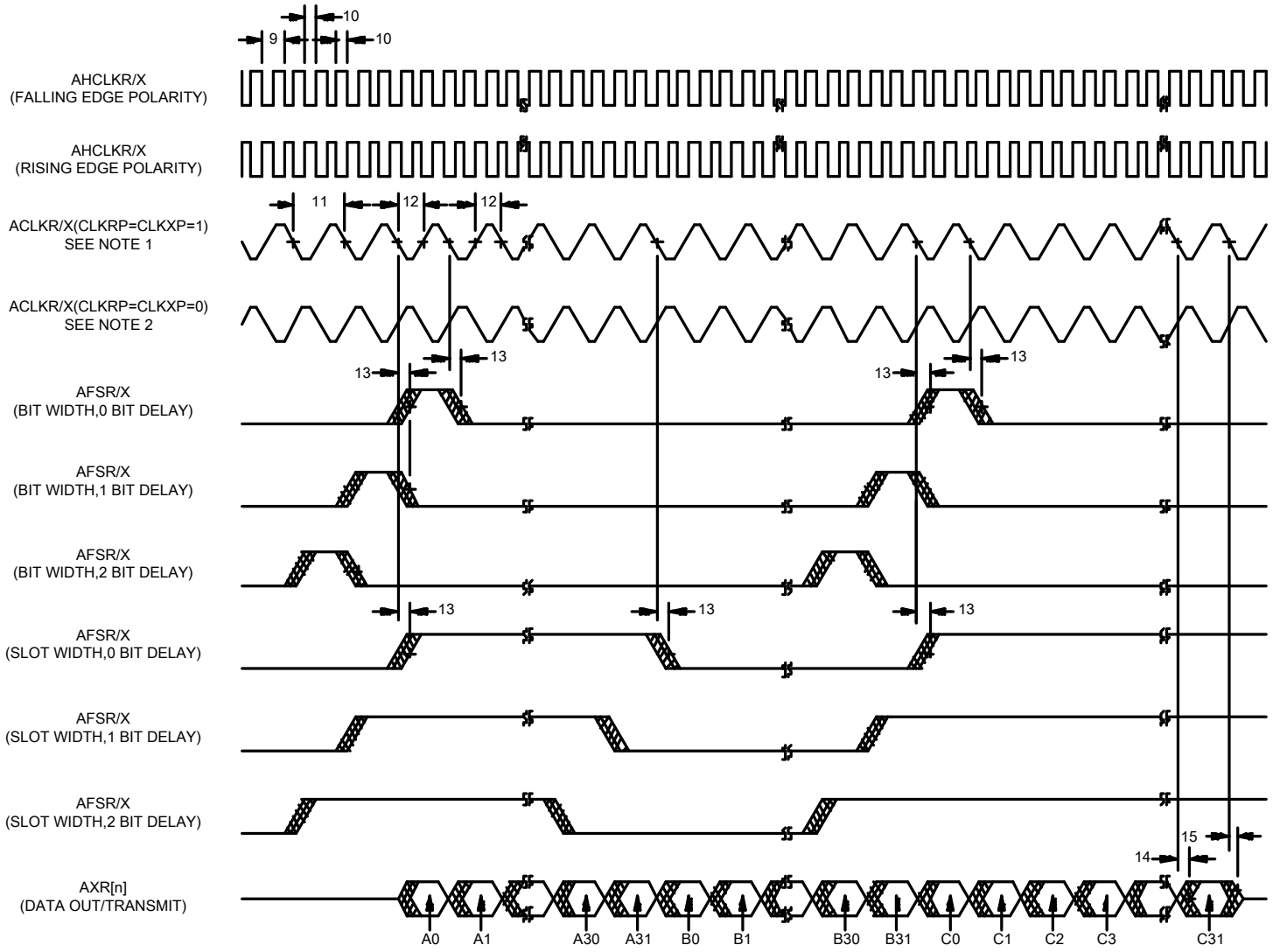

FIGURE 21. McASP Block Diagram




NOTES:

1. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).
2. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in)

FIGURE 22. McASP Input timings




NOTES:

1. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in)
2. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

FIGURE 23. McASP Output timings

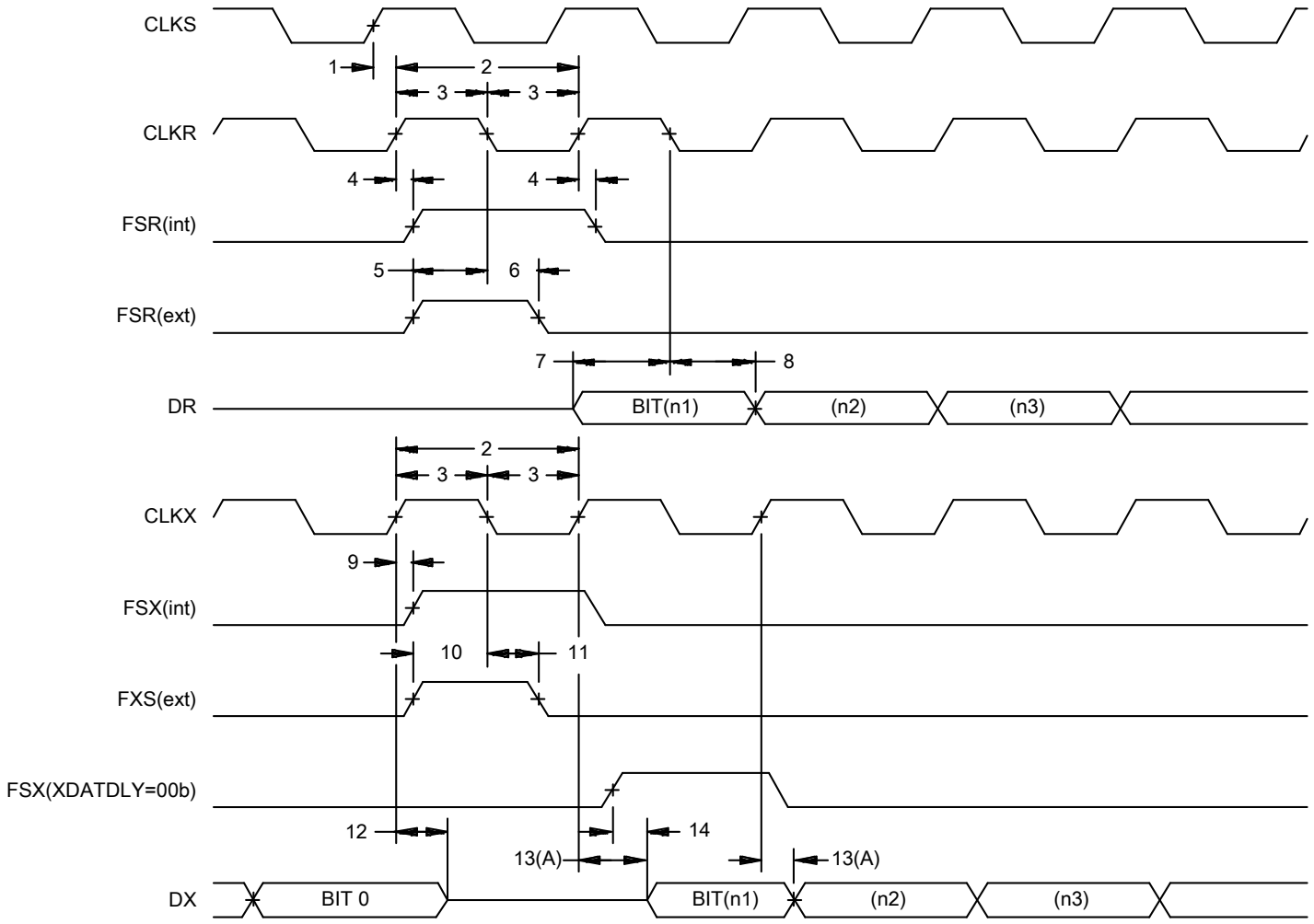



FIGURE 24. McBSP timings

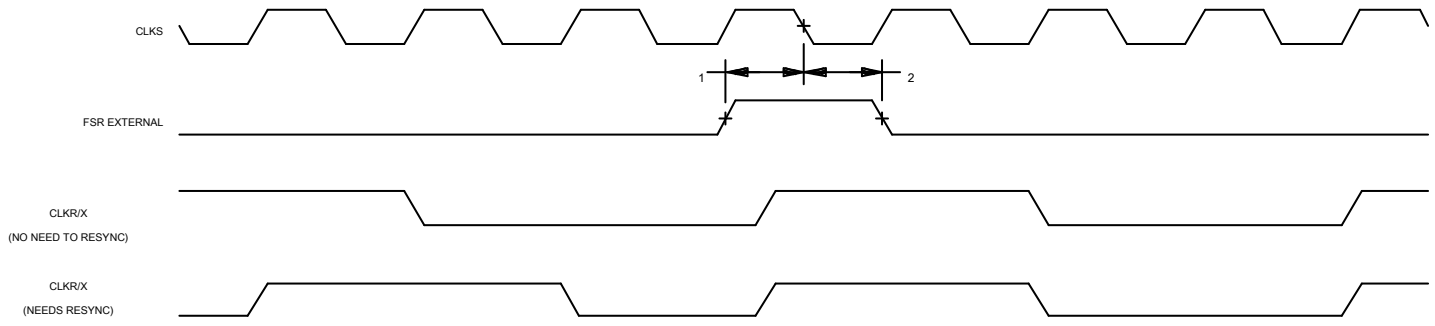



FIGURE 25. FSR timing when GSYNC = 1

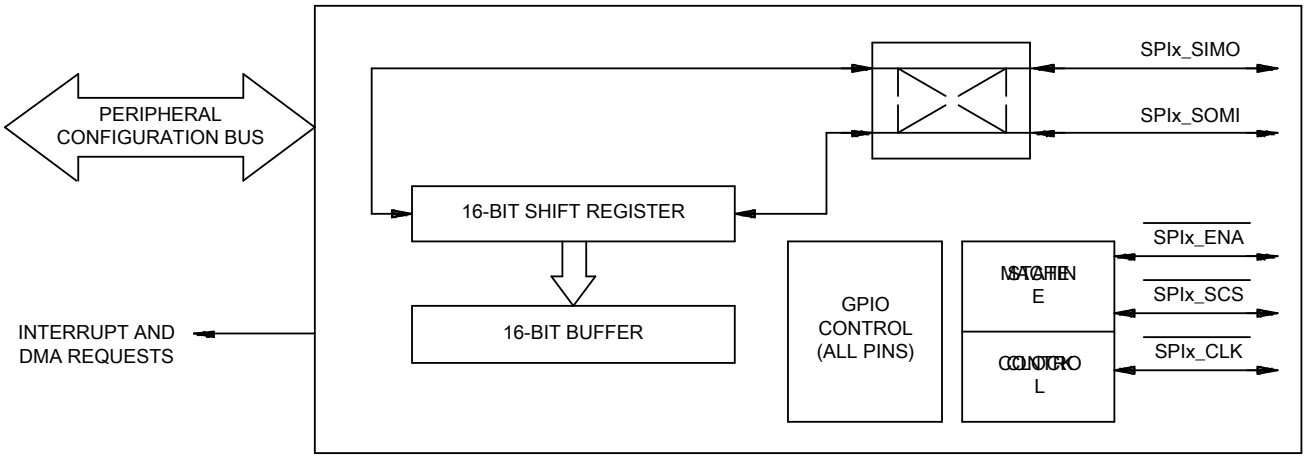



FIGURE 26. Block diagram of SPI module.

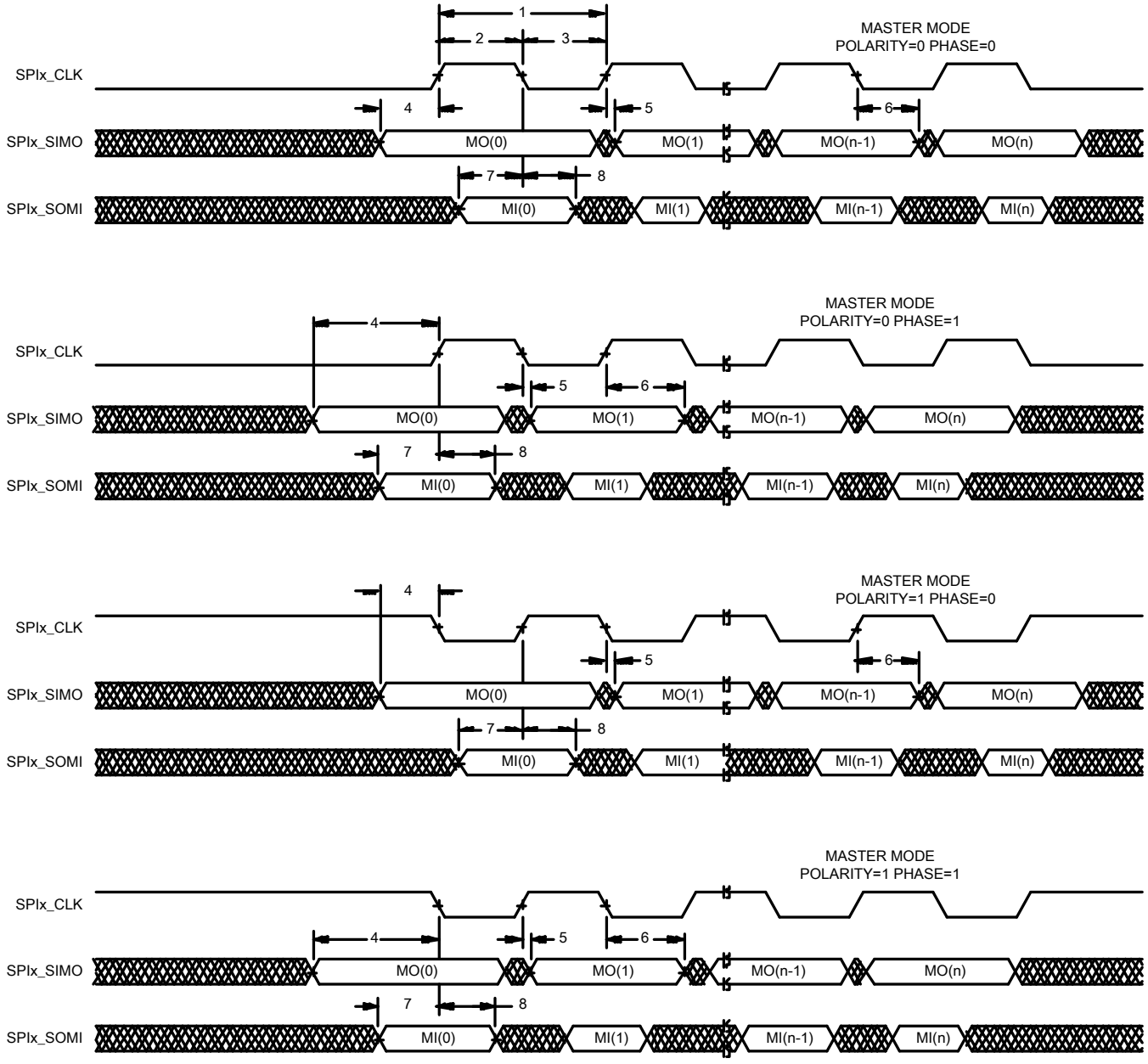



FIGURE 27. SPI Timings – Master mode.

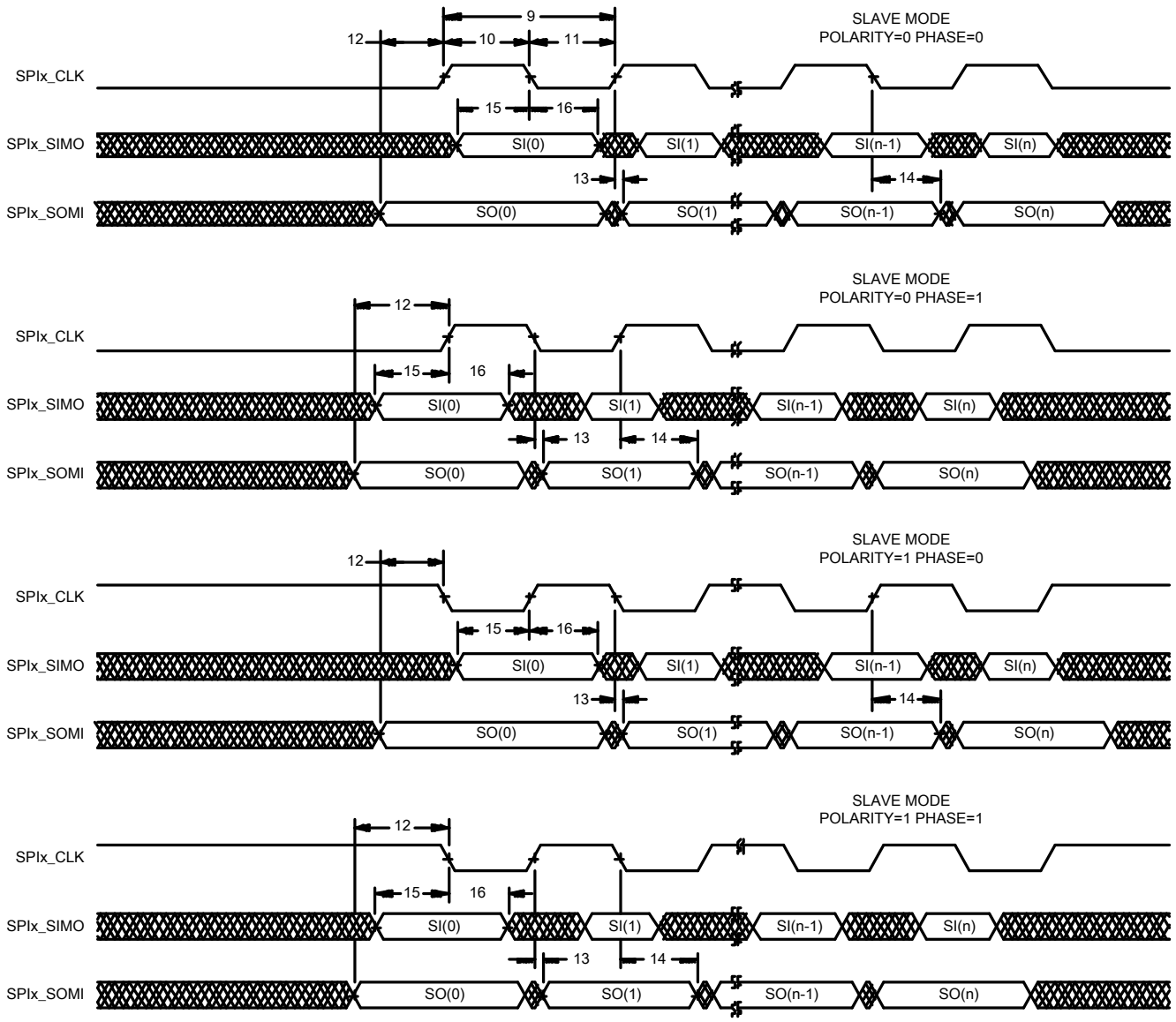
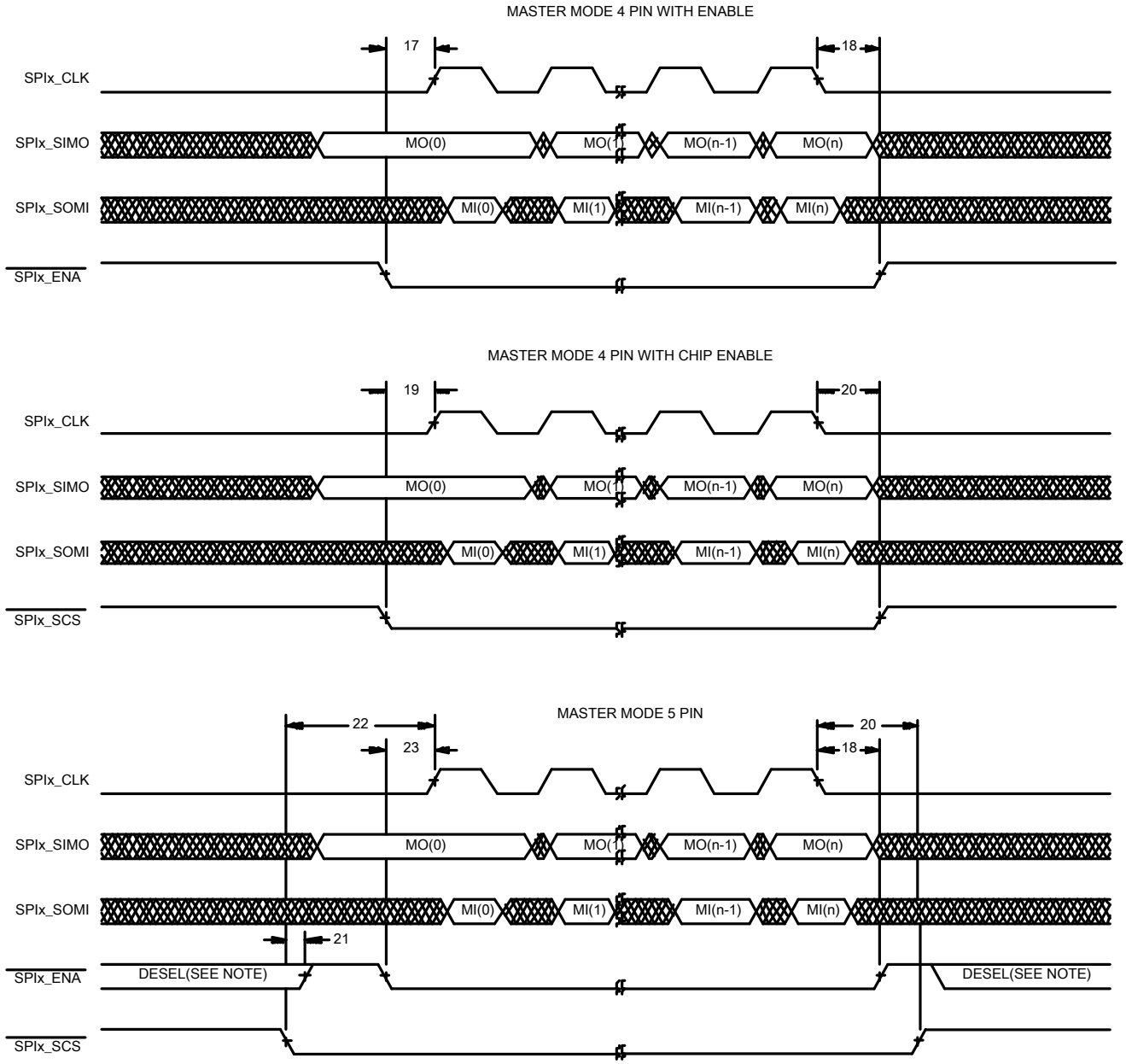
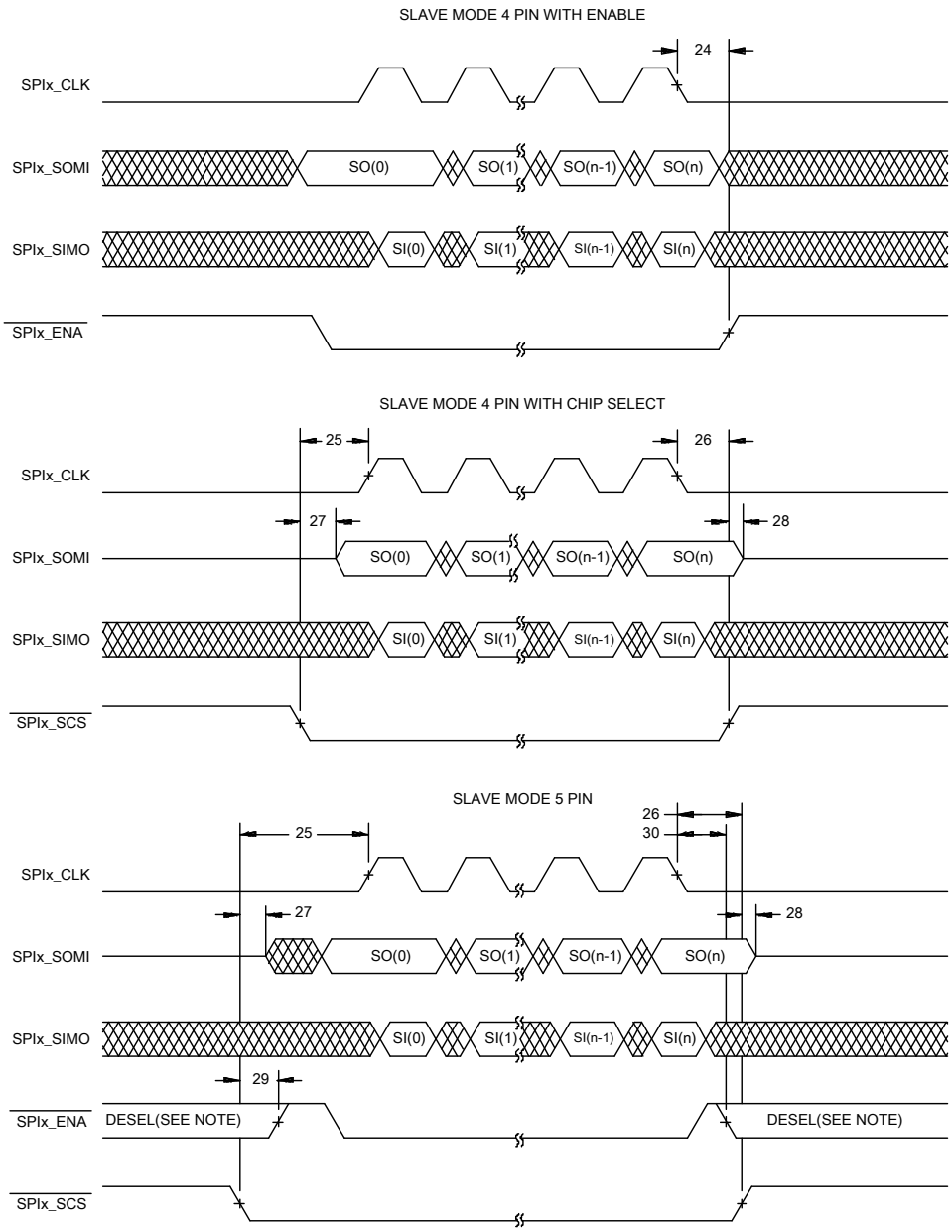



FIGURE 28. SPI Timings – Slave mode.




NOTE:
1. A deselected is programmable either high or 3-state (Required external pullup)

FIGURE 29. SPI Timings – Master mode (4-Pin and 5-Pin).




NOTE:

1. A deselected is programmable either high or 3-state (Required external pullup)

FIGURE 30. SPI Timings – Slave mode (4-Pin and 5-Pin).

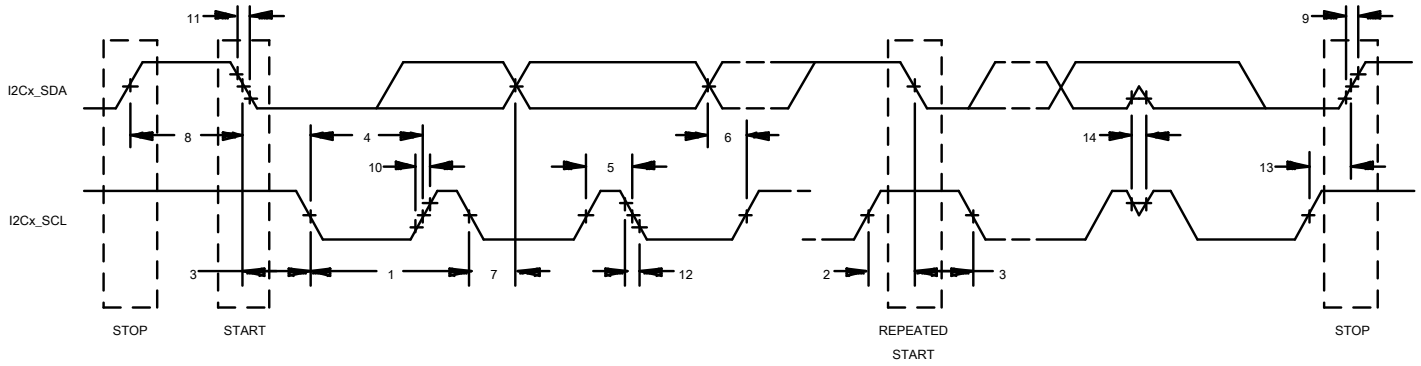



FIGURE 31. I2C Receive timings.

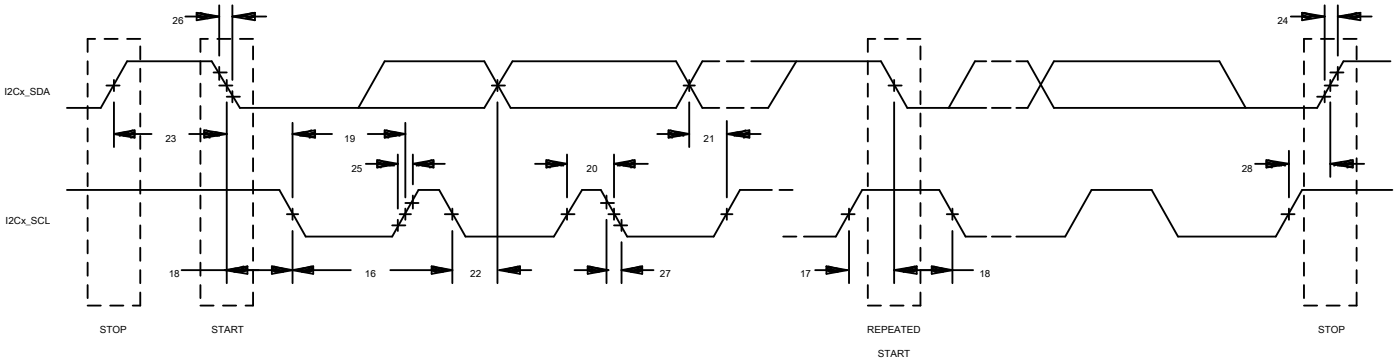



FIGURE 32. I2C Transmit timings.

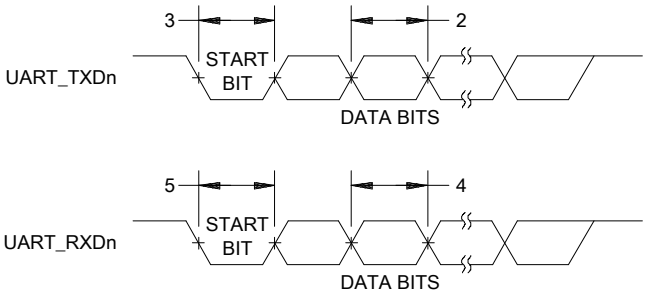



FIGURE 33. UART Transmit/Receive timing.

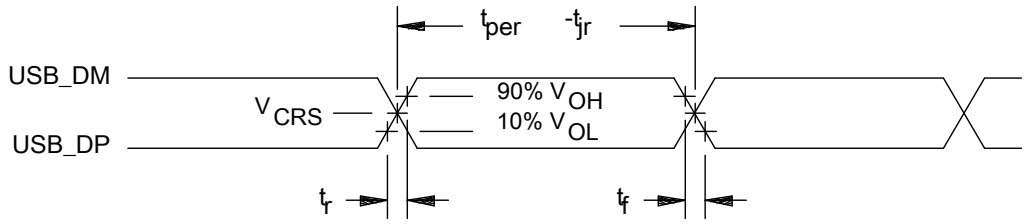



FIGURE 34. USB2.0 Integrated Transceiver Interface timing.

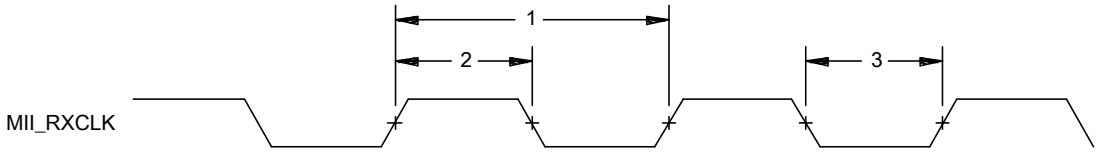



FIGURE 35. MII_RXCLK timing (EMAC – Receive).

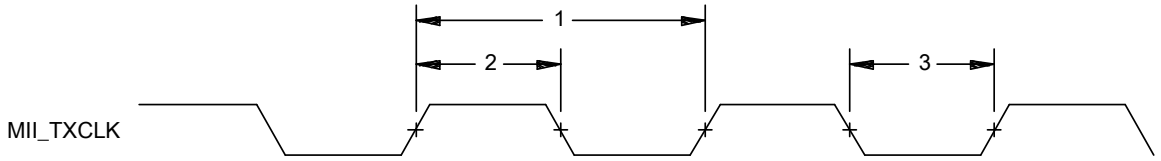



FIGURE 36. MII_TXCLK timing (EMAC – Transmit).

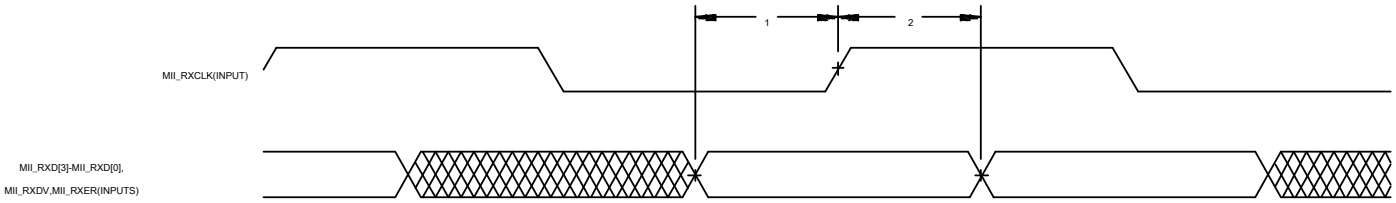



FIGURE 37. EMAC Receive Interface timing.

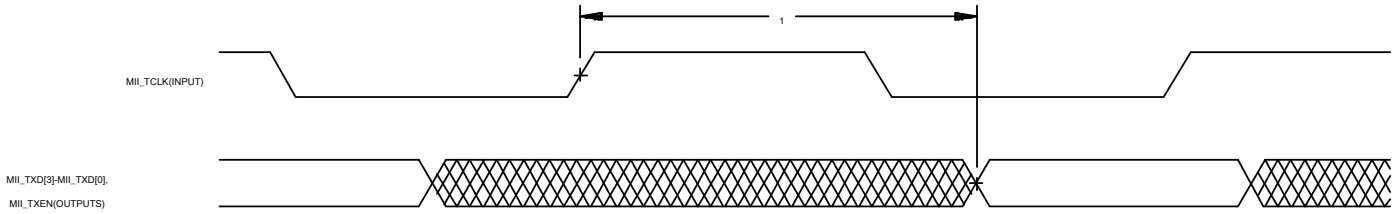



FIGURE 38. EMAC Transmit Interface timing.

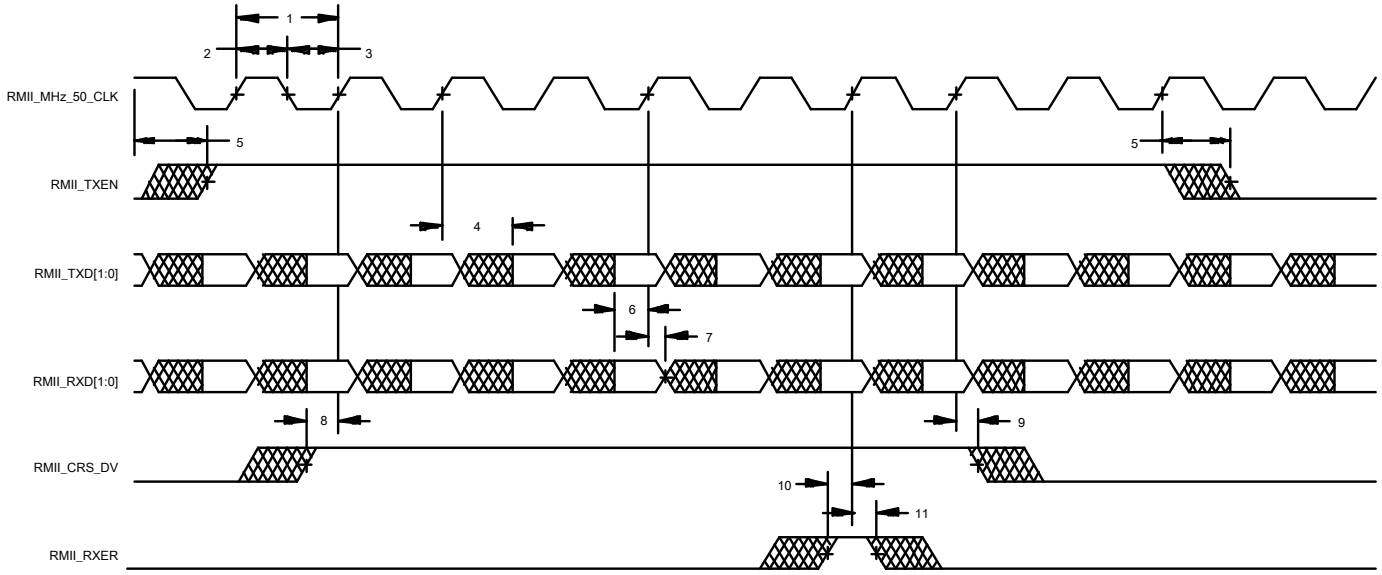



FIGURE 39. RMII Timing diagram

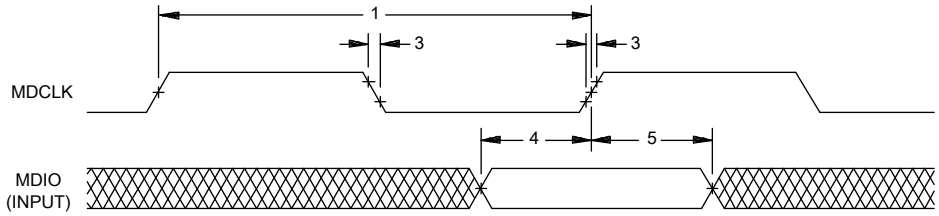



FIGURE 40. MDIO Input timing.

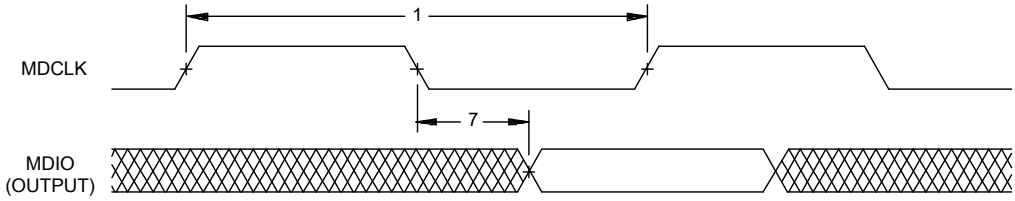



FIGURE 41. MDIO Output timing.

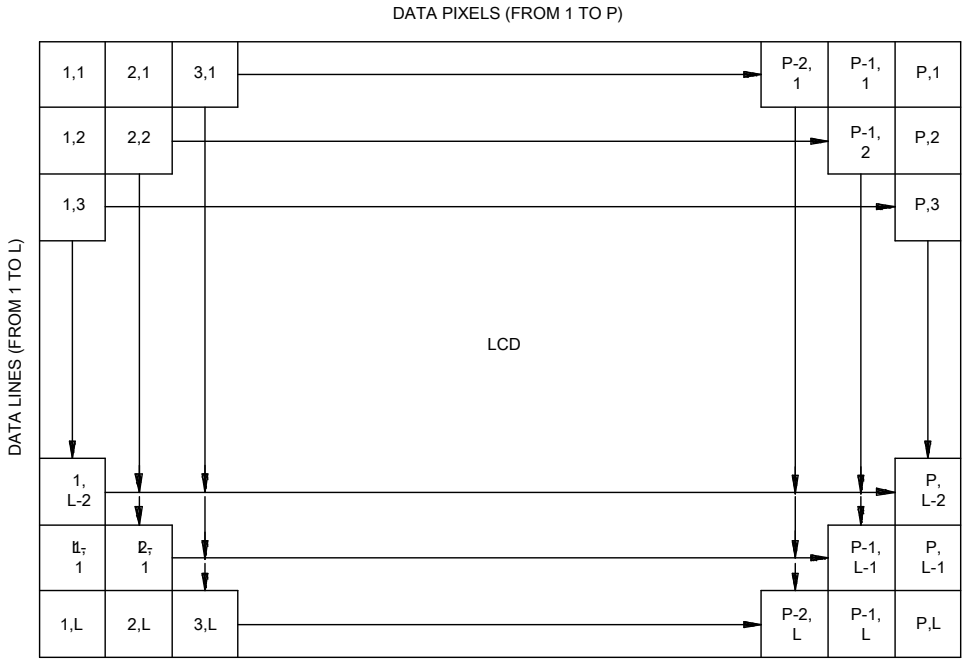



FIGURE 42. LCD Raster Mode display format.

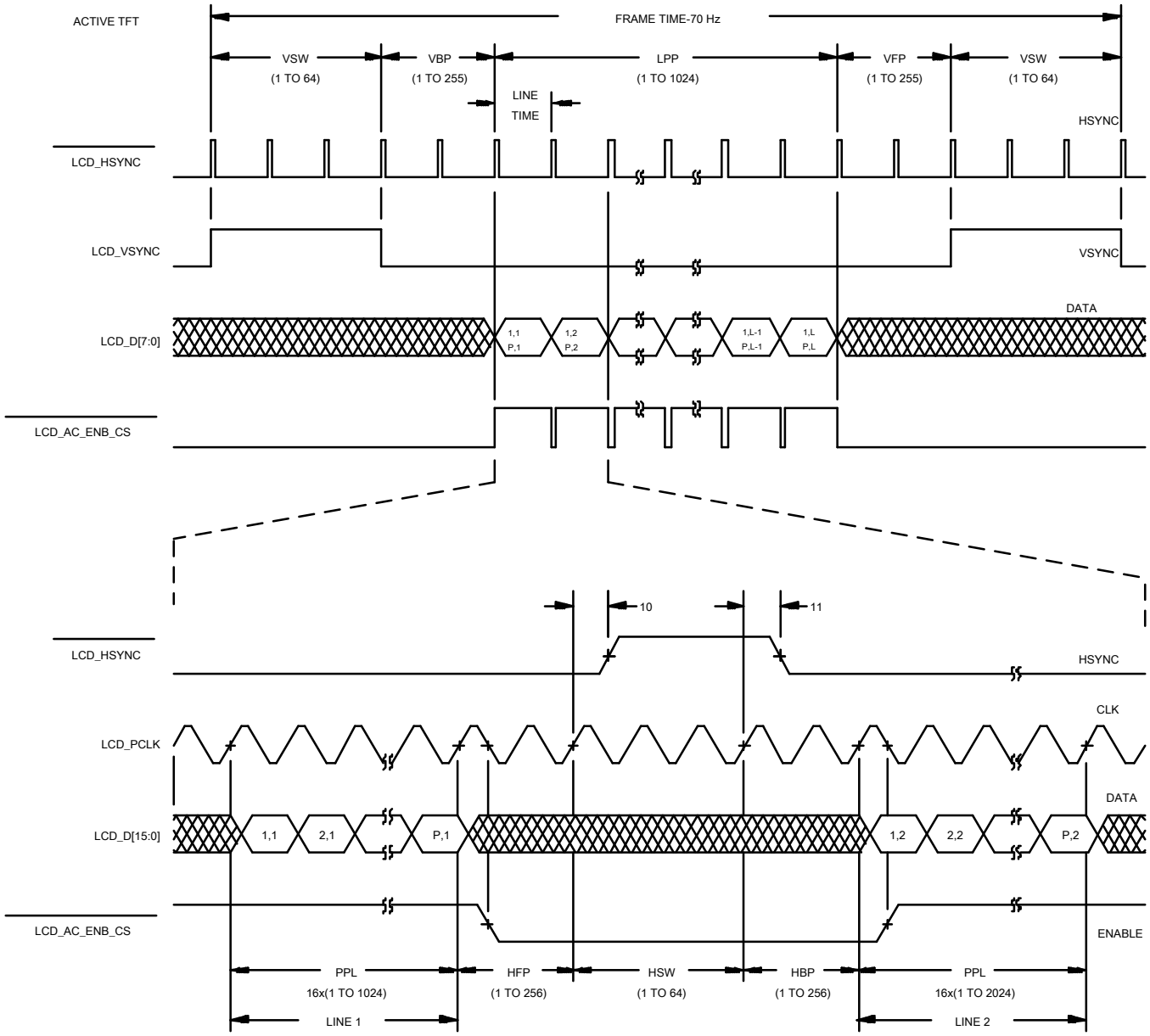



FIGURE 43. LCD Raster Mode Active.

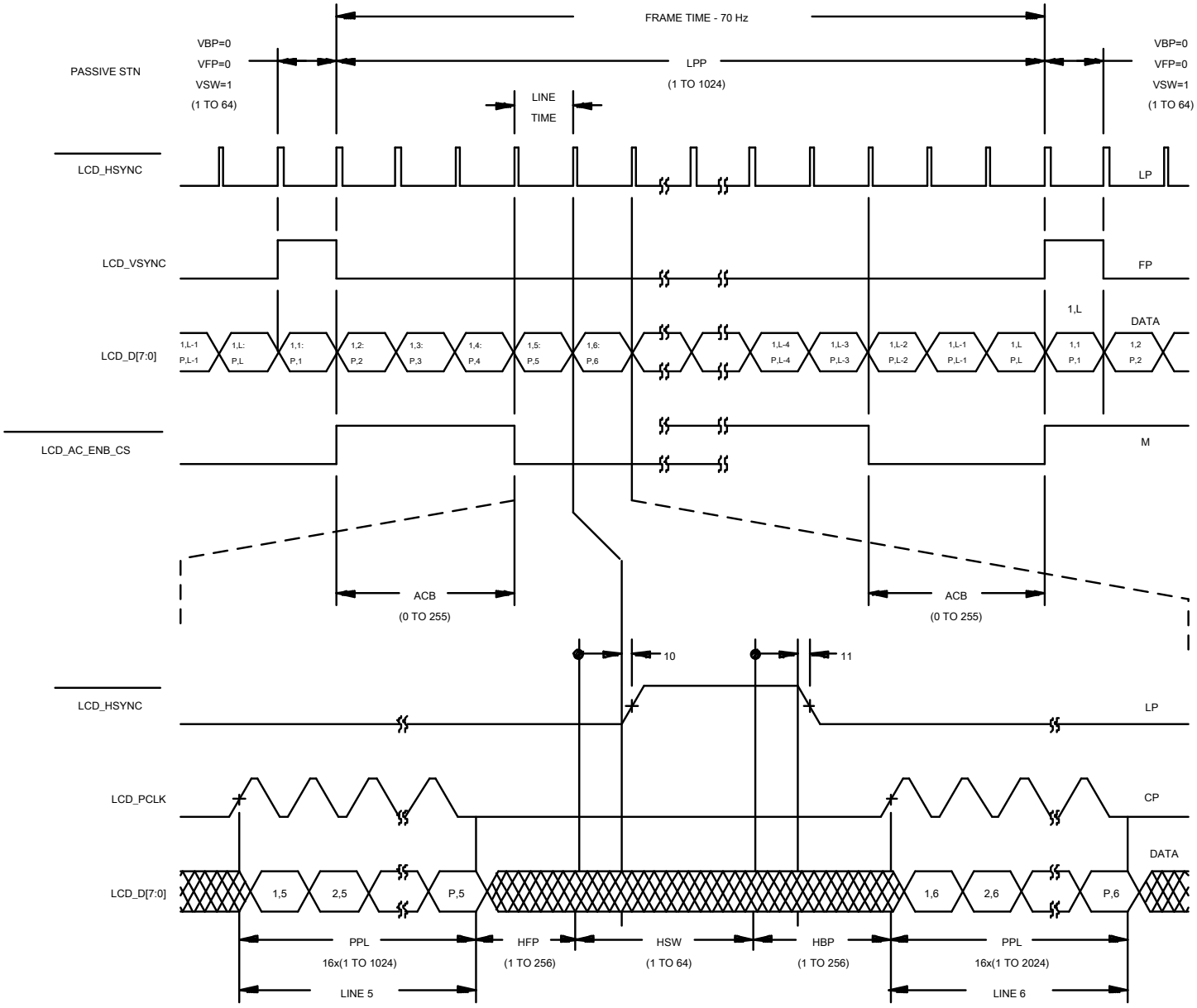



FIGURE 44. LCD Raster Mode Passive.

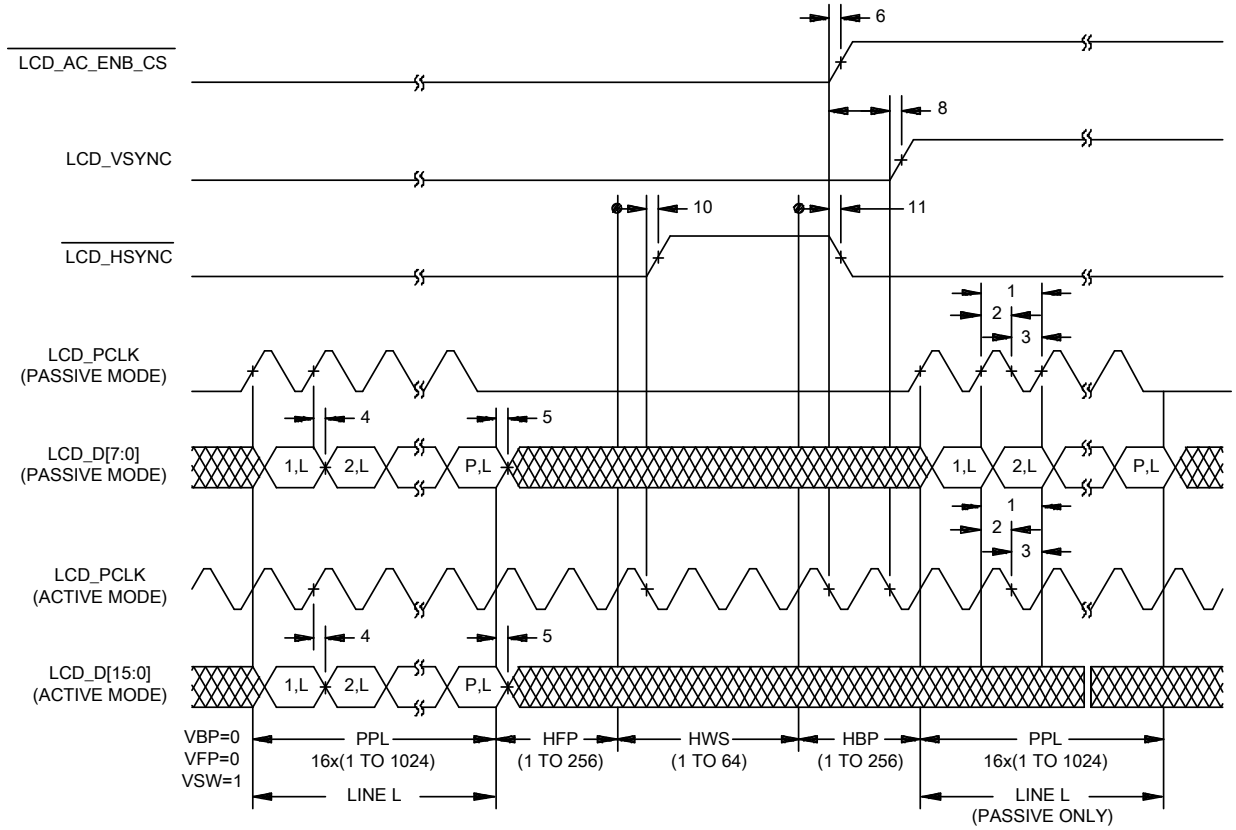



FIGURE 45. LCD Raster Mode Control signal activation.

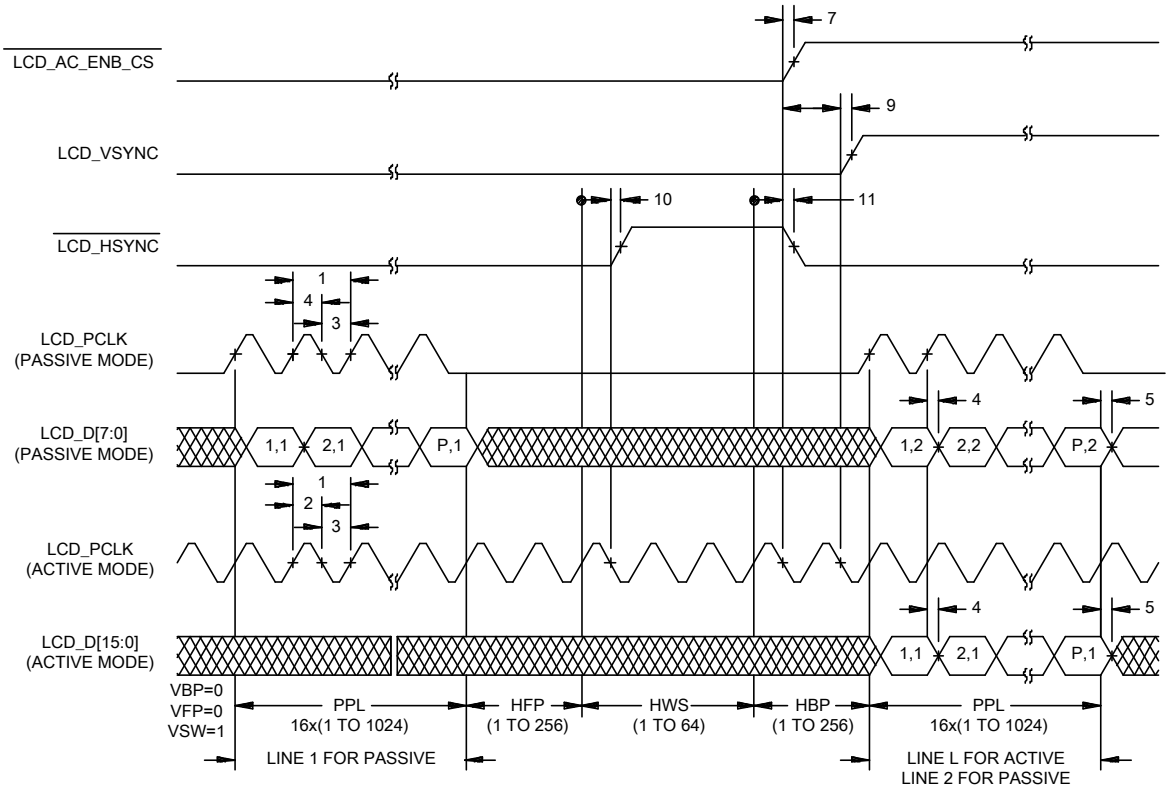
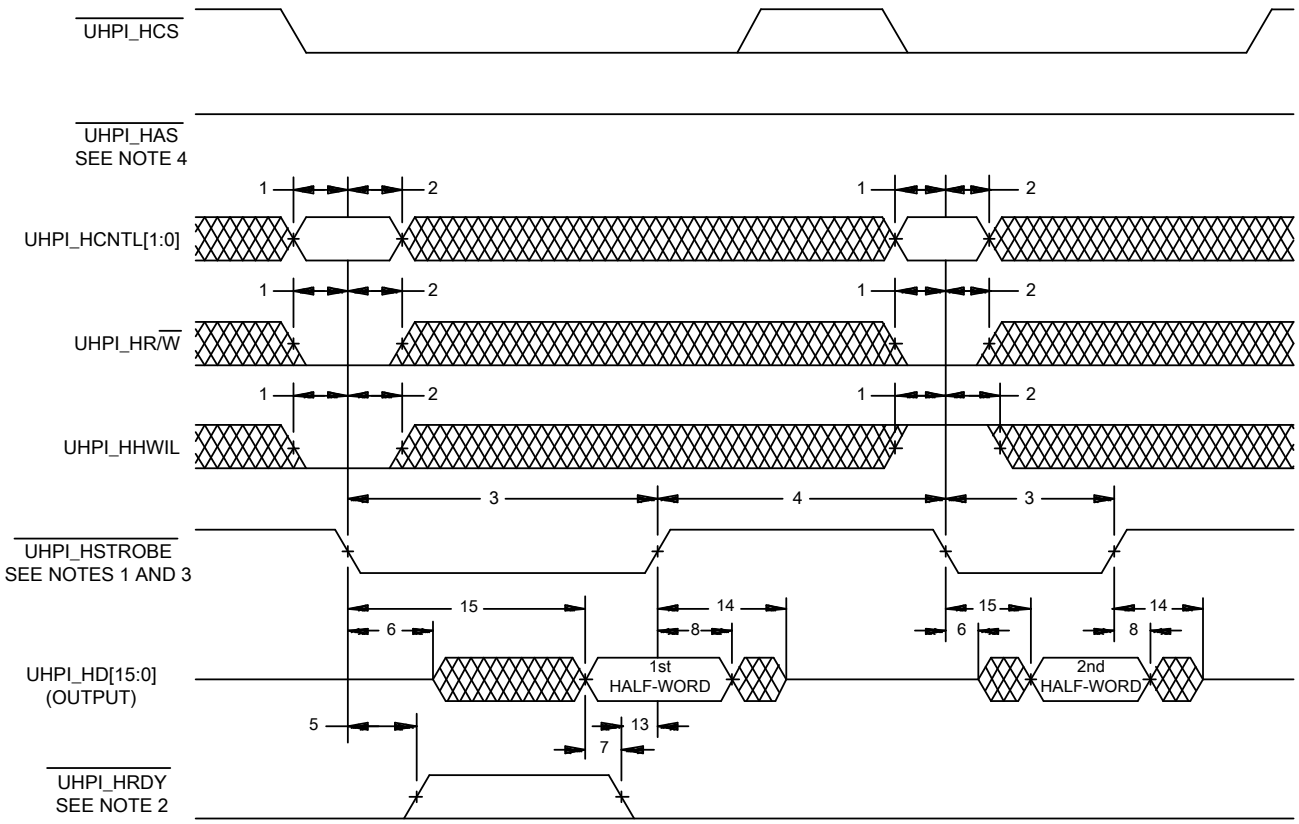


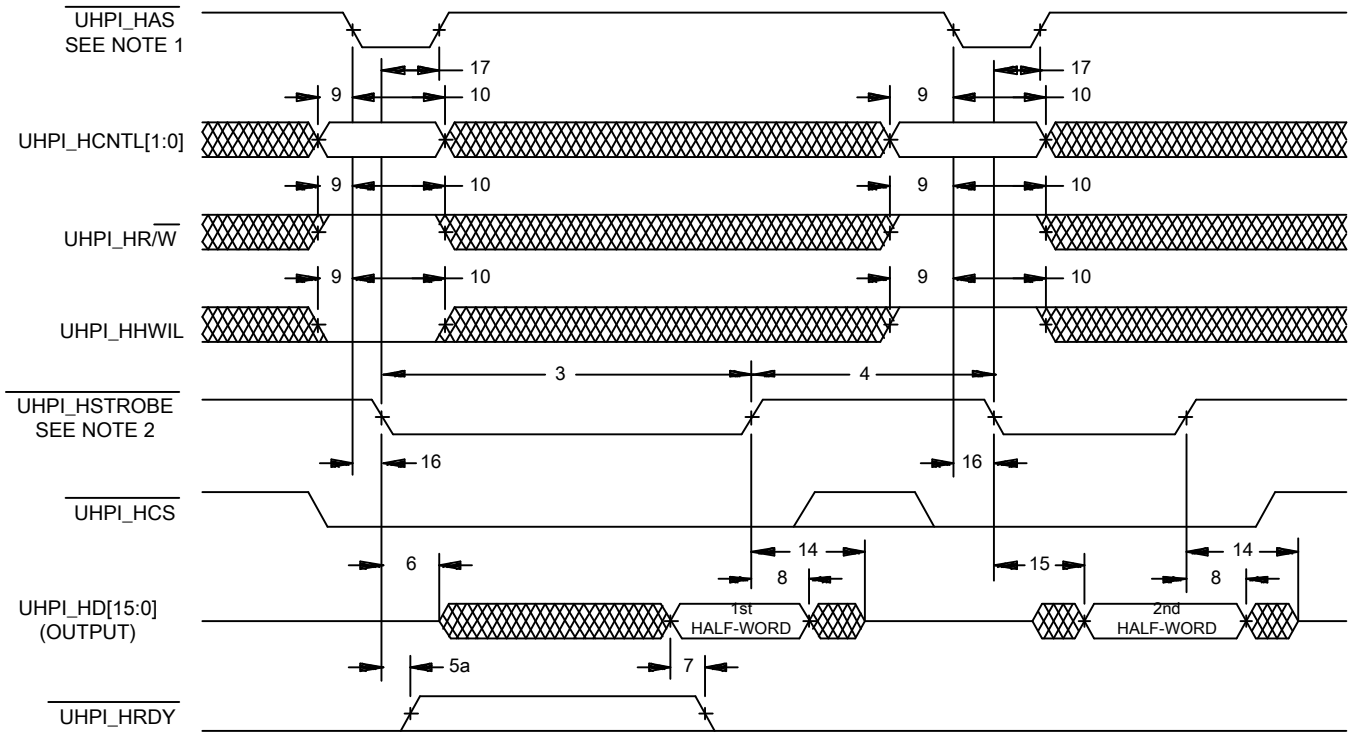

FIGURE 46. LCD Raster Mode Control signal deactivation.




NOTES:

1. $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$ [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transaction on $\overline{\text{UHPI_HRDY}}$ may or may not occur.
3. $\overline{\text{UHPI_HCS}}$ reflects typical $\overline{\text{UHPI_HCS}}$ behavior when $\overline{\text{UHPI_HSTROBE}}$ assertion is cause by $\overline{\text{UHPI_HDS1}}$ or $\overline{\text{UHPI_HDS2}}$, $\overline{\text{UHPI_HCS}}$ timing requirements are reflected by parameters for $\overline{\text{UHPI_HSTROBE}}$.
4. The diagram above assumes $\overline{\text{UHPI_HAS}}$ has pulled high.

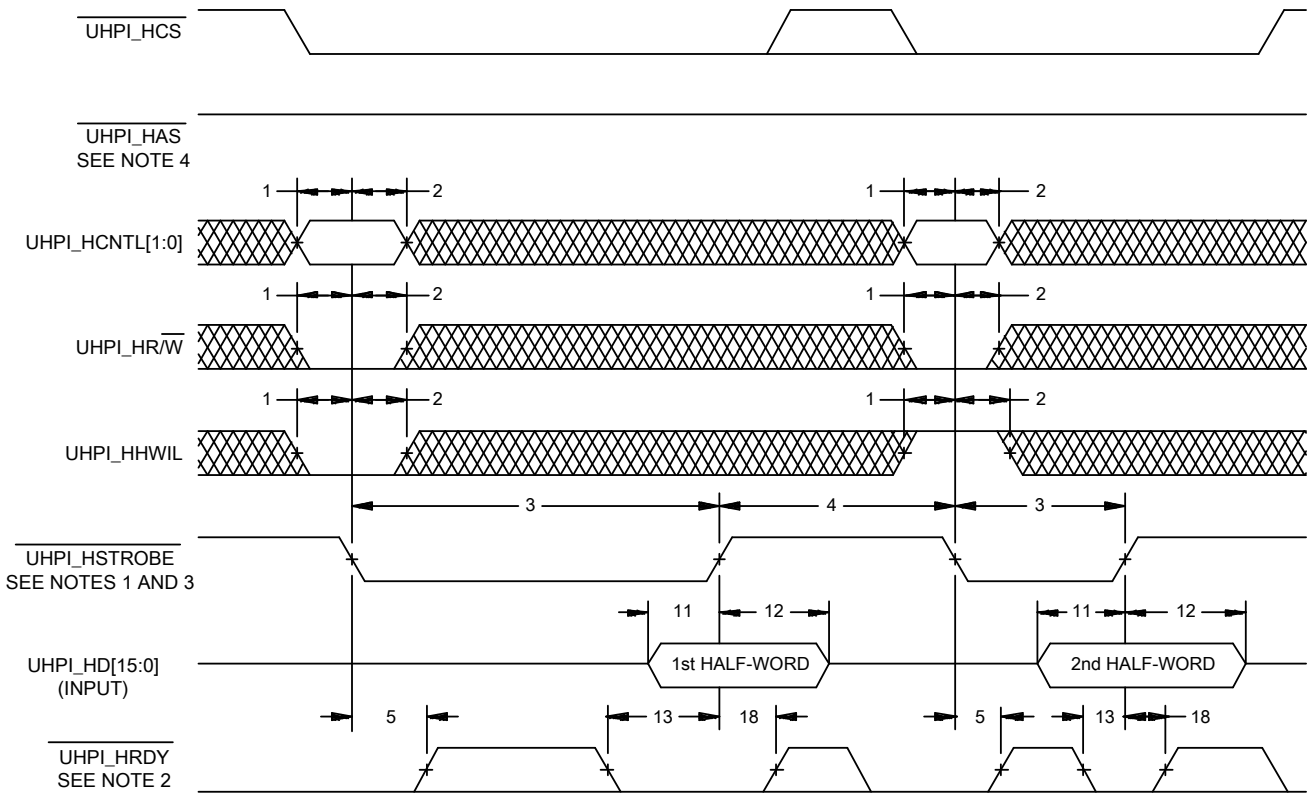
FIGURE 47. UHPI Read timing ($\overline{\text{HAS}}$ not used, Tied high).




NOTES:

1. For correct operation, strobe the s $\overline{\text{UHPI_HAS}}$ signal only once per $\overline{\text{UHPI_HSTROBE}}$ active cycle.
2. $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$ [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.

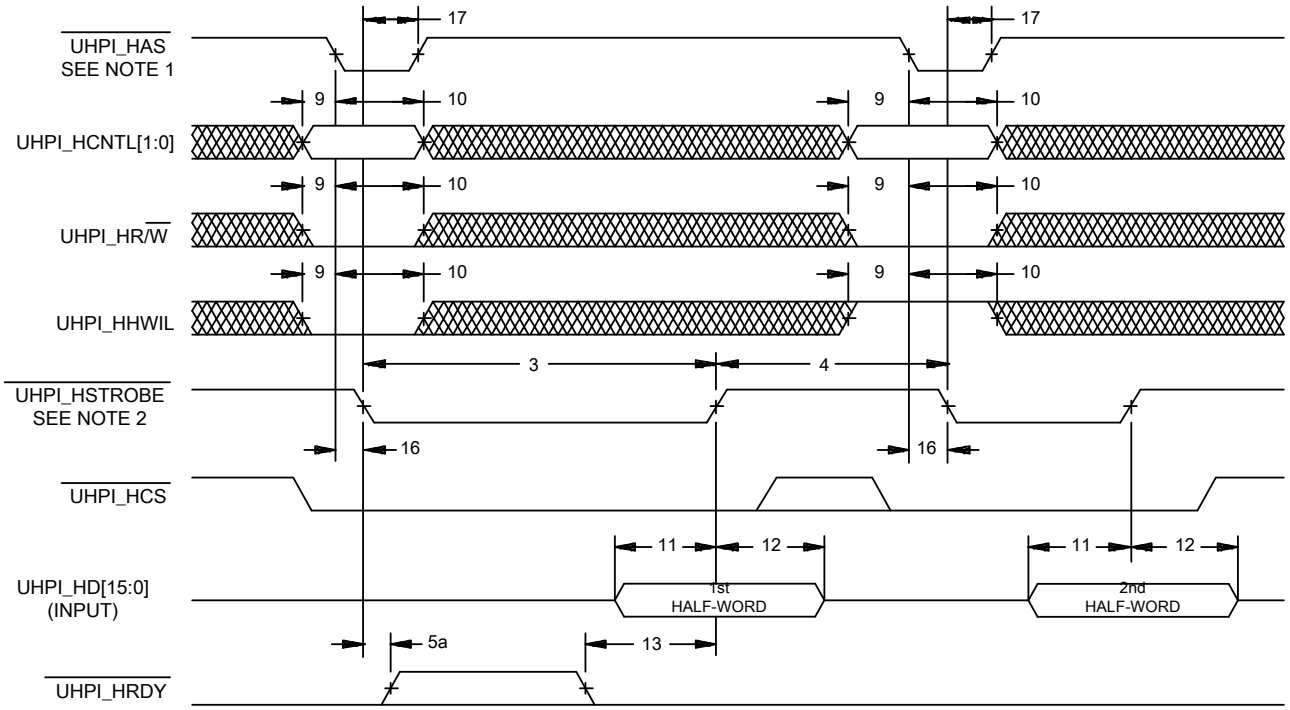
FIGURE 48. UHPI Read timing ($\overline{\text{HAS}}$ used).




NOTES:

1. $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$ [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transaction on $\overline{\text{UHPI_HRDY}}$ may or may not occur.
3. $\overline{\text{UHPI_HCS}}$ reflects typical $\overline{\text{UHPI_HCS}}$ behavior when $\overline{\text{UHPI_HSTROBE}}$ assertion is cause by $\overline{\text{UHPI_HDS1}}$ or $\overline{\text{UHPI_HDS2}}$, $\overline{\text{UHPI_HCS}}$ timing requirements are reflected by parameters for $\overline{\text{UHPI_HSTROBE}}$.
4. The diagram above assumes $\overline{\text{UHPI_HAS}}$ has pulled high.

FIGURE 49. UHPI Write timing ($\overline{\text{HAS}}$ not used, Tied high).




NOTES:

1. For correct operation, strobe the s $\overline{\text{UHPI_HAS}}$ signal only once per $\overline{\text{UHPI_HSTROBE}}$ active cycle.
2. $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$ [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.

FIGURE 50. UHPI Write timing ($\overline{\text{HAS}}$ used).

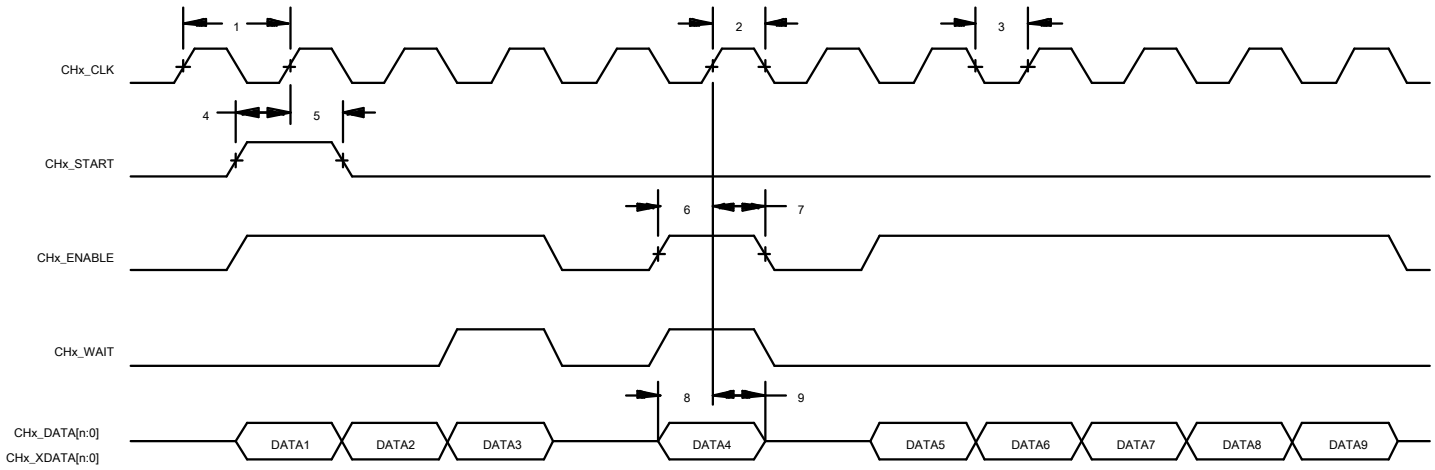



FIGURE 51. µPP Single Data Rate (SDR) receive timing.

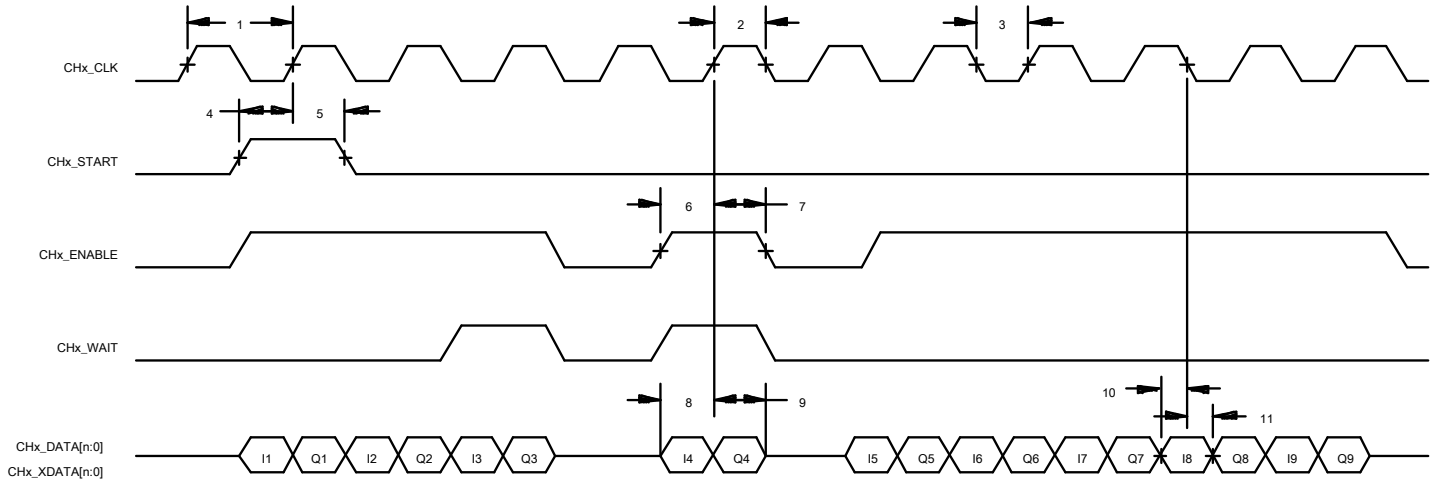



FIGURE 52. µPP Double Data Rate (DDR) receive timing.

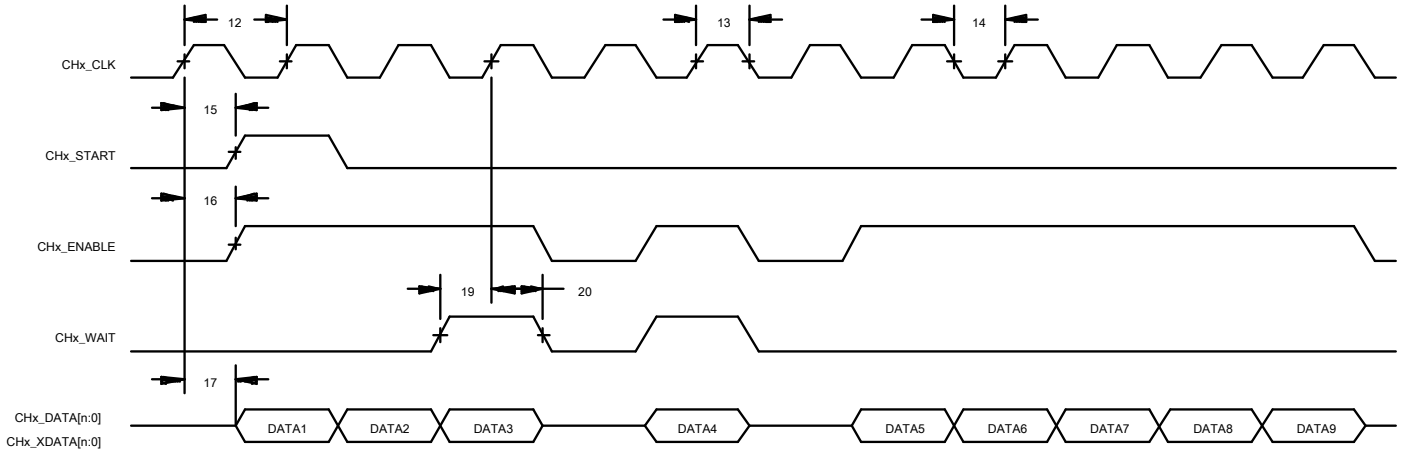



FIGURE 53. µPP Single Data Rate (SDR) transmit timing.

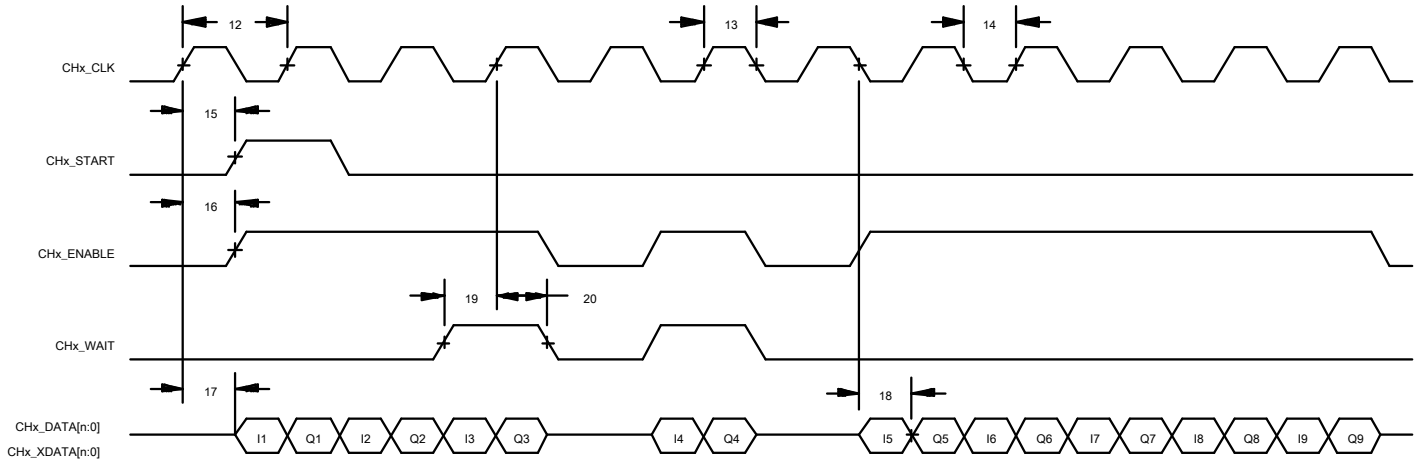



FIGURE 54. µPP Double Data Rate (DDR) transmit timing.

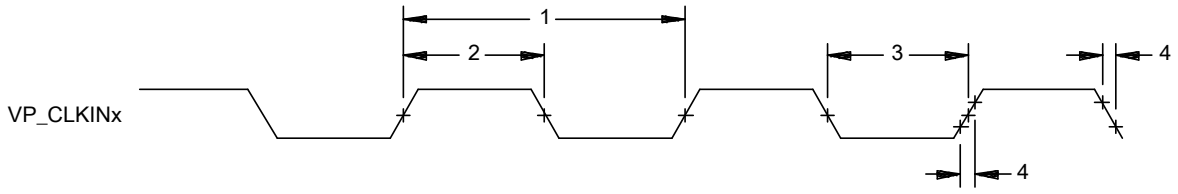



FIGURE 55. Video Port Capture VP_CLKINx timing.

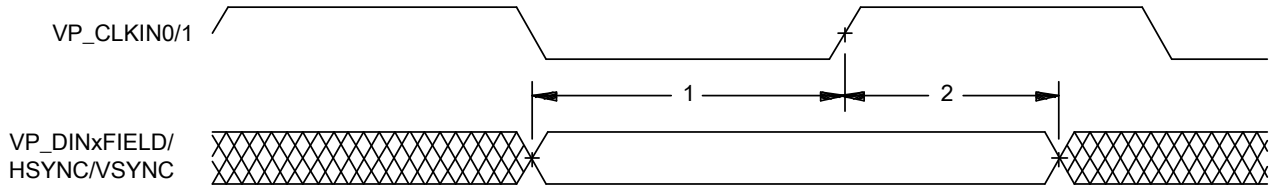



FIGURE 56. VPIF channels 0/1 Video capture data and control input timing.

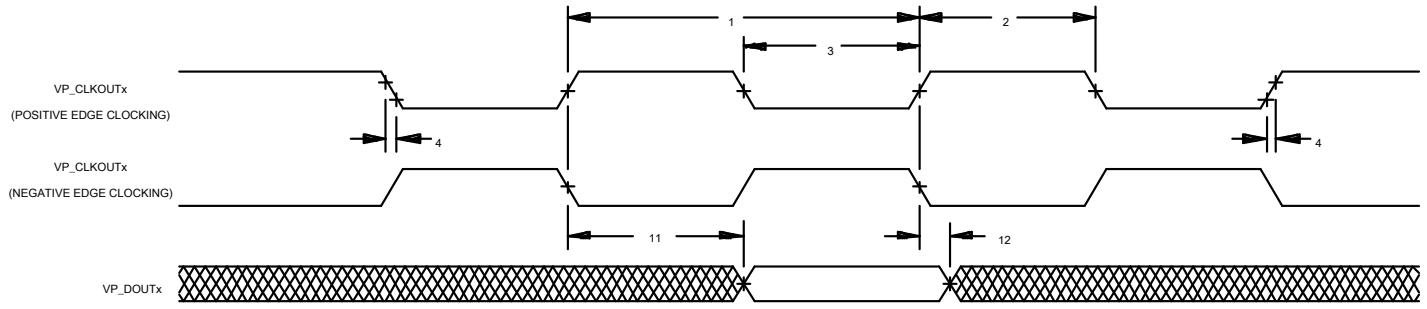



FIGURE 57. VPIF channels 2/3 Video Display Data Output timing with respect to VP_CLKOUT2/3

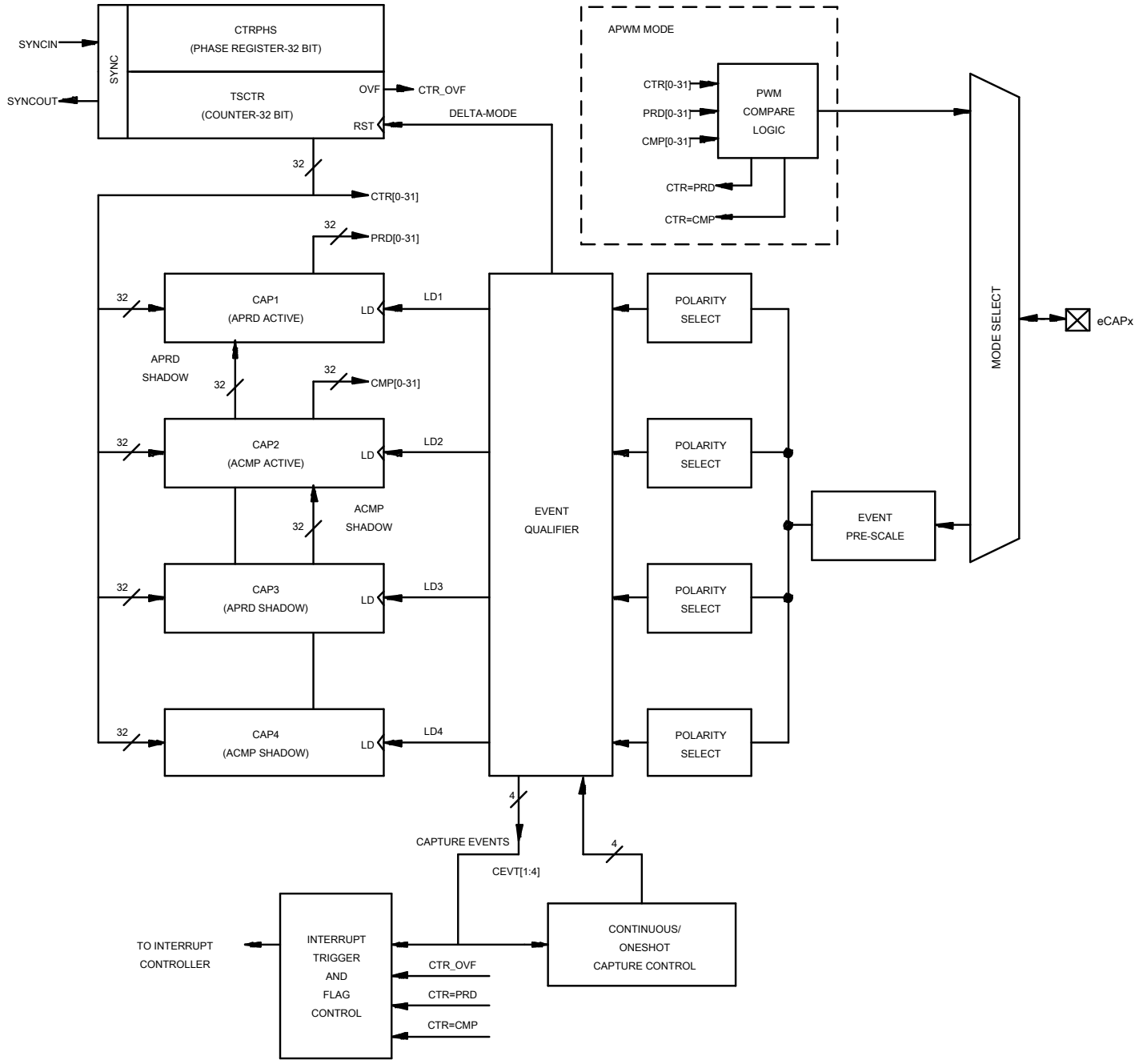
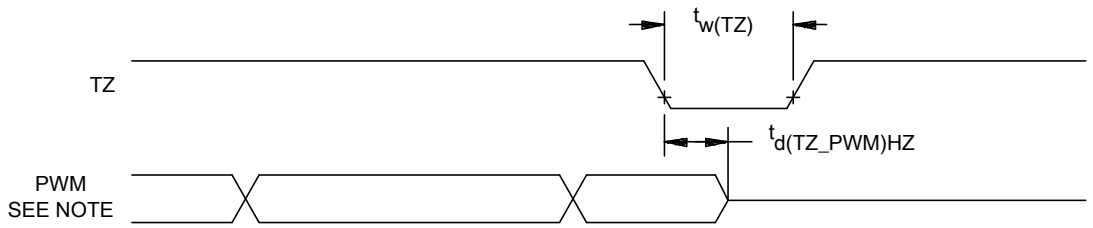



FIGURE 58. eCAP functional block diagram.




NOTE:

1. PWM refers to all the PWM pins ih the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

FIGURE 59. PWM Hi-Z characteristics.

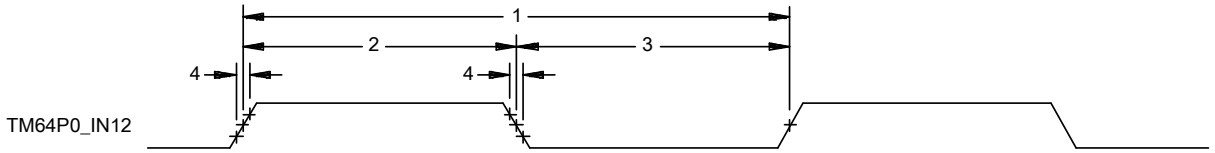



FIGURE 60. Timer timing.

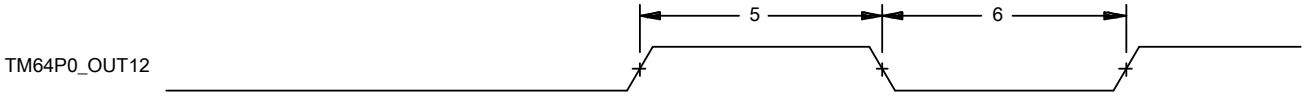



FIGURE 61. Timer timing.

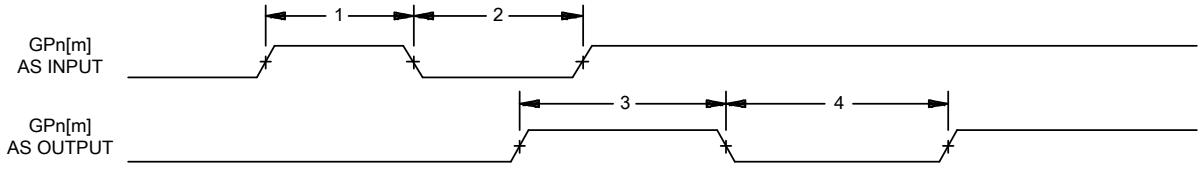



FIGURE 62. GPIO port timing.

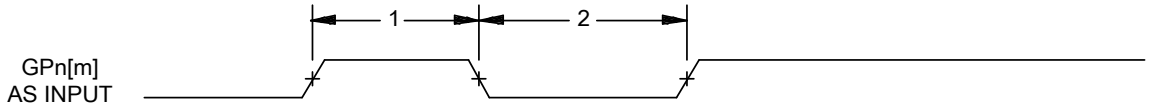



FIGURE 63. GPIO external interrupt timing.

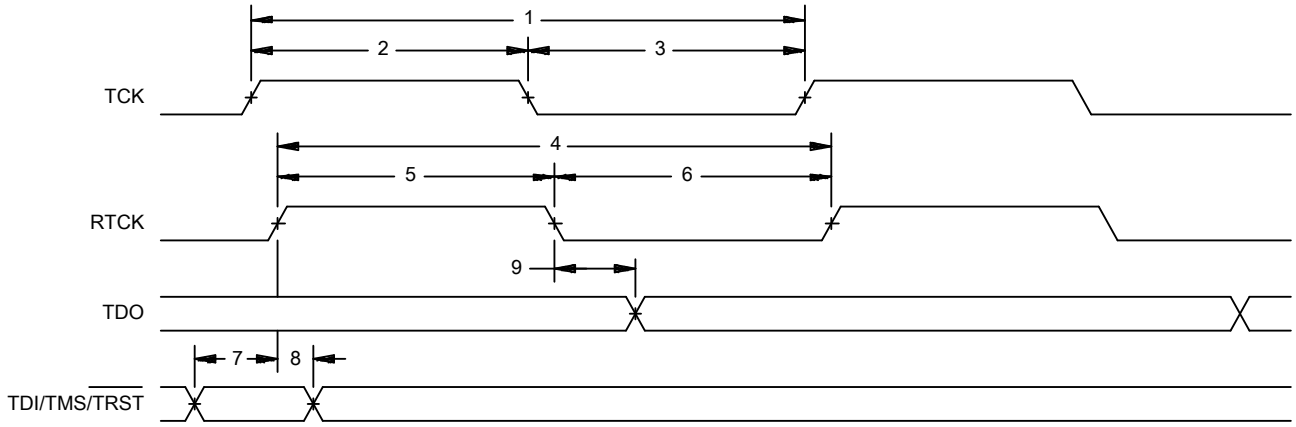



FIGURE 64. JTAG test port timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

| Vendor item drawing administrative control number 1/ | Device manufacturer CAGE code | Vendor part number | Top Side Marking |
|---|---|---|---|
| V62/12605-01XE | 01295 | OMAPL138BGWTMEP | OMAPL138BGWTMEP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

| CAGE code | Source of supply |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |