REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Table I, input offset voltage test, delete 9 mV and substitute 8 mV. Table I, input offset current test, delete 20 nA and substitute 2 nA. Table I, input bias current test, delete 50 nA and substitute 20 nA. Table I, slew rate at unity gain test, delete 5 V/µs and substitute 8 V/µs. - ro	12-12-04	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	19-08-22	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B									
	PAGE			1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 12-01-19	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	TITLE MICROCIRCUIT, LINEAR, LOW NOISE JFET INPUT OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12604**
	REV **B**	**PAGE** 1 **OF** 10

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

AMSC N/A

5962-V067-19

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low noise junction field effect transistor (JFET) input operational amplifier microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12604	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TL072-EP	Low noise JFET input operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage:	
$+V_{CC}$	18 V 2/
$-V_{CC}$	18 V 2/
Differential input voltage (V_{ID})	±30 V 3/
Input voltage (V_I)	±15 V 2/ 4/
Duration of output short circuit	Unlimited 5/
Operating virtual Junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to ambient (θ_{JA})	97.5°C/W 6/ 7/
Thermal resistance, junction to ambient (θ_{JC})	38.3°C/W 7/

1.4 Recommended operating conditions. 8/

Supply voltage range ($\pm V_{CC}$)	±15 V
Operating free-air temperature range (T_A)	-40°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential voltages, are with respect to the midpoint between $+V_{CC}$ and $-V_{CC}$.

3/ Differential voltages are at +IN, with respect to -IN.

4/ The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

5/ The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6/ Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of +150°C can affect reliability.

7/ The package thermal impedance is calculated in accordance with JESD 51-7.

8/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Unity gain amplifier. The unity gain amplifier shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ $\pm V_{CC} = \pm 15$ V, unless otherwise specified	Temperature, T_A 3/	Device type	Limits		Unit
					Min	Max	
Electrical characteristics section							
Input offset voltage	V_{IO}	$V_O = 0$, $R_S = 50\ \Omega$	+25°C	01		6	mV
			-40°C to +125°C			8	
Temperature coefficient of input offset voltage	αV_{IO}	$V_O = 0$, $R_S = 50\ \Omega$	-40°C to +125°C	01	18 typical		µV / °C
Input offset current	I_{IO}	$V_O = 0$	+25°C	01		100	pA
			-40°C to +125°C			2	nA
Input bias current	I_{IB}	$V_O = 0$	+25°C	01		200	pA
			-40°C to +125°C			20	nA
Common mode input voltage range	V_{ICR}		+25°C	01	±11		V
Maximum peak output voltage swing	V_{OM}	$R_L = 10\ k\Omega$	+25°C	01	±12		V
		$R_L \geq 10\ k\Omega$	-40°C to +125°C		±12		
		$R_L \geq 2\ k\Omega$			±10		
Large signal differential voltage amplification	A_{VD}	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	+25°C	01	35		V / mV
			-40°C to +125°C		15		
Unity gain bandwidth	B1		+25°C	01	3 typical		MHz
Input resistance	r_i		+25°C	01	10^{12} typical		Ω
Common mode rejection ratio	CMRR	$V_{IC} = V_{ICR}$min, $V_O = 0$, $R_S = 50\ \Omega$	+25°C	01	80		dB
Supply voltage rejection ratio ($\Delta \pm V_{CC} / \Delta V_{IO}$)	k_{SVR}	$V_{CC} = \pm 9$ V to ± 15 V, $V_O = 0$, $R_S = 50\ \Omega$	+25°C	01	80		dB
Supply current (each amplifier)	I_{CC}	$V_O = 0$, no load	+25°C	01		2.5	mA
Crosstalk attenuation	V_{O1} / V_{O2}	$A_{VD} = 100$	+25°C	01	120 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $\pm V_{CC} = \pm 15$ V	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Operating characteristics section							
Slew rate at unity gain	SR	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, see figure 3	+25°C	01	8		V/μs
Rise time overshoot factor	t_r	V_I = 20 V, R_L = 2 kΩ, C_L = 100 pF, see figure 3	+25°C	01	0.1 typical 20 typical		μs %
Equivalent input noise voltage	Vn	f = 1 kHz, R_S = 20 Ω	+25°C	01	18 typical		$nV/\sqrt{Hz}$
		f = 10 Hz to 10 kHz, R_S = 20 Ω			4 typical		μV
Equivalent input noise current	I_n	f = 1 kHz, R_S = 20 Ω	+25°C	01	0.01 typical		$pA/\sqrt{Hz}$
Total harmonic distortion	THD	$V_I$rms = 6 V, A_{VD} = 1, $R_L \geq 2$ kΩ, $R_S \leq 1$ kΩ, f = 1 kHz	+25°C	01	0.003 typical		%

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Input bias currents of an field effect transistor (FET) input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

3/ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

Case X

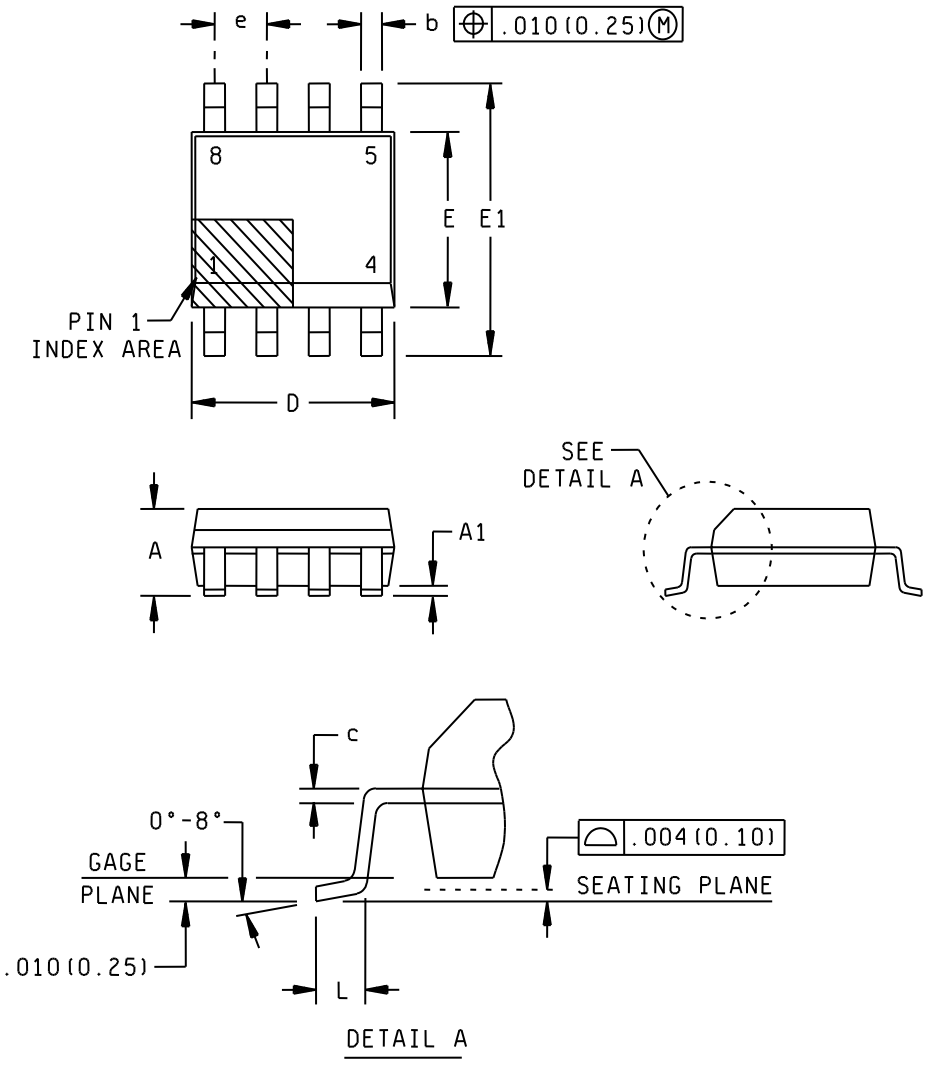

FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) each side.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
4. Falls with JEDEC MS-012 variation AA.

FIGURE 1. Case outline – Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT1
2	-IN1
3	+IN1
4	$-V_{CC}$
5	+IN2
6	-IN2
7	OUT2
8	$+V_{CC}$

FIGURE 2. Terminal connections.

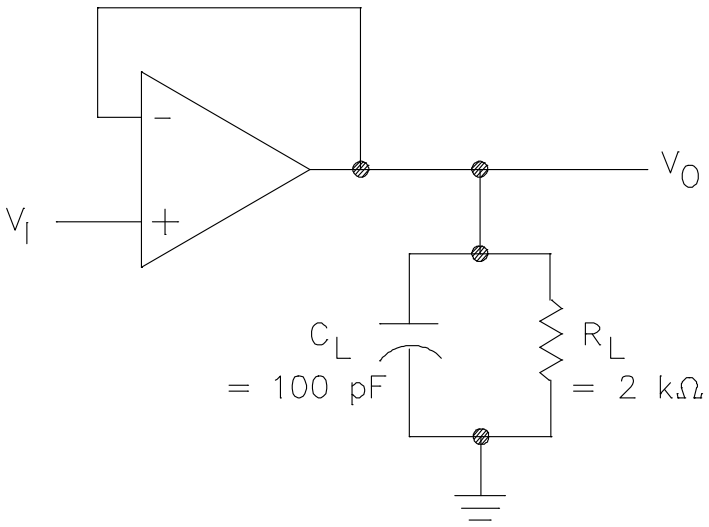

FIGURE 3. Unity gain amplifier.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/12604-01XE	01295	TL072Q	TL072QDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243