REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 13-01-28	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, COMPOLETE DDR, DDR2 AND DDR3 MEMORY POWER SOLUTION SYNCHRONOUS BUCK CONTROLLER, 3 A LDO, BUFFERED REFERENCE, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/12602**
	REV	**PAGE** 1 **OF** 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance complete DDR, DDR2 and DDR3 memory power solution synchronous buck controller, 3-A LDO, buffered reference microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12602	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS51116-EP	Complete DDR, DDR2 and DDR3 memory power solution synchronous buck controller, 3-A LDO, buffered reference

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage range, (V_{IN}):
- VBST ..... -0.3 V to 36.0 V
- VBST wrt LL ..... -0.3 V to 6.0 V
- CS, MODE, S3, S5, VTTSNS, VDDQSNS, V5IN, VLDOIN, VDDQSET ..... -3.0 V to 6.0 V
- PGND, VTTGND ..... -0.3 V to 0.3 V

Output voltage range, (V_{OUT}):
- DVRH ..... -1.0 V to 36.0 V
- LL ..... -1.0 V to 30.0 V
- LL, pulse width < 20 ns ..... -5 V to 30.0 V
- COMP, DRVL, PGOOD, VTT, VTTREF ..... -0.3 V to 6.0 V

Maximum junction temperature, (T_J) ..... 150°C

Storage temperature range (Tstg) ..... -65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

1.4 Thermal characteristics.

Thermal metric 2/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 3/	41.2	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 4/	27.4	
Junction to board thermal resistance, θ_{JB} 5/	23.9	
Junction to top characterization parameter, Ψ_{JT} 6/	1.1	
Junction to board characterization parameter, Ψ_{JB} 7/	23.7	
Junction to case (bottom) thermal resistance, θ_{JCbot} 8/	3.6	

1.5 Recommended operating conditions.

Supply voltage, V5IN ..... 4.75 V to 5.25 V
Voltage range,
VBST, DRVH ..... -0.1 V to 34.0 V
LL ..... -0.6 V to 28.0 V
VLDOIN, VTT, VTTSNS, VDDQSNS ..... -0.1 V to 3.6 V
VTTREF ..... -0.1 V to 1.8 V
PGND, VTTGND ..... -0.1 V to 0.1 V
S3, S5, MODE, VDDQSET, CS, COMP, PGOOD, DRVL ..... -0.1 V to 5.25 V
Operating temperature range, (T_J) ..... -55°C to 125°C

2/ For more information about traditional and new thermal metrics, see manufacturer data.
3/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
4/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
5/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
6/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
7/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
8/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
JESD51-2a	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88 – Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Applications for copies should be addressed to the American National Standards Institute, Semiconductor Equipment and Materials International, 1819 L Street, NW, 6 th floor, Washington, DC 20036 or online at http://www.ansi.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits Min	Limits Typ	Limits Max	Unit
Supply Current						
Supply current 1, V5IN	I_{V5IN1}	No load, $V_{S3} = V_{S5} = 5$ V, COMP connected to capacitor		0.8	2	mA
Supply current 2, V5IN	I_{V5IN2}	No load, $V_{S3} = 0$ V, $V_{S5} = 5$ V COMP connected to capacitor		300	610	µA
Supply current 3, V5IN	I_{V5IN3}	No load, $V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{COMP} = 5$ V		240	508	
Shutdown current, V5IN	$I_{V5INSDN}$	No load, $V_{S3} = V_{S5} = 0$ V		0.1	1.81	
Supply current 1, VLDOIN	$I_{VLDOIN1}$	No load, $V_{S3} = V_{S5} = 5$ V		1	10	
Supply current 2, VLDOIN	$I_{VLDOIN2}$	No load, $V_{S3} = 5$ V, $V_{S5} = 0$ V		0.1	10.5	
Standby current, VLDOIN	$I_{VLDOINSDN}$	No load, $V_{S3} = V_{S5} = 0$ V		0.1	1.5	
VTTREF output						
Output voltage, VTTREF	V_{VTTREF}			$V_{VDDQSNS}/2$		V
Output voltage tolerance	$V_{VTTREFTOL}$	-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS} = 2.5$ V, Tolerance to $V_{VDDQSNS}/2$	-20		20	mV
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS} = 1.8$ V, Tolerance to $V_{VDDQSNS}/2$	-19		19	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS} = 1.5$ V, Tolerance to $V_{VDDQSNS}/2$	-16		16	
		-10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS} = 1.2$ V, Tolerance to $V_{VDDQSNS}/2$	-13		13	
Source current	$V_{VTTTREFSRC}$	$V_{VDDQSNS} = 2.5$ V, $V_{VTTREF} = 0$ V	-19	-40	-83.5	mA
Sink current	$V_{VTTTREFSNK}$	$V_{VDDQSNS} = 2.5$ V, $V_{VTTREF} = 2.5$ V	19	40	83.5	
VDDQ Output						
Output voltage, VDDQ	V_{VDDQ}	$T_A = 25°C$, $V_{VDDQSET} = 0$ V, No load	2.465	2.500	2.535	V
		-55°C ≤ T_A ≤ 125°C, $V_{VDDQSET} = 0$ V, No load	2.43	2.50	2.56	
		$T_A = 25°C$, $V_{VDDQSET} = 5$ V, No load	1.776	1.800	1.830	
		-55°C ≤ T_A ≤ 125°C, $V_{VDDQSET} = 5$ V, No load	1.762	1.800	1.838	
		-55°C ≤ T_A ≤ 125°C, Adjustable mode, No load	0.75		3.0	
VDDQSET regulation voltage	$V_{VDDQSET}$	T_A ≤ 25°C, Adjustable mode	742.5	750	760.5	mV
		-55°C ≤ T_A ≤ 125°C, Adjustable mode	737	750	763	
Input impedance, VDDQSNS	$R_{VDDQSNS}$	$V_{VDDQSET} = 0$ V		215		kΩ
		$V_{VDDQSET} = 5$ V		180		
		Adjustable mode		460		
Input current, VDDQSET	$I_{VDDQSET}$	$V_{VDDQSET} = 0.78$ V, COMP = Open		-0.04		µA
		$V_{VDDQSET} = 0.78$ V, COMP = 5 V		-0.06		
Discharge current, VDDQ	$I_{VDDQDisch}$	$V_{S3} = V_{S5} = 0$ V, $V_{VDDQSNS} = 0.5$ V, $V_{MODE} = 0$ V	10	40		mA
Discharge current, VLDOIN	$I_{VLDOINDisch}$	$V_{S3} = V_{S5} = 0$ V, $V_{VDDQSNS} = 0.5$ V, $V_{MODE} = 0.5$ V		700		mA

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Limits Min		Max	Unit
VTT Output						
Output voltage, VTT	V_{VTTSNS}	$V_{S3} = V_{S5} = 5$ V, $V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V		1.25		V
		$V_{S3} = V_{S5} = 5$ V, $V_{VLDOIN} = V_{VDDQSNS} = 1.8$ V		0.9		
		$V_{S3} = V_{S5} = 5$ V, $V_{VLDOIN} = V_{VDDQSNS} = 1.5$ V		0.75		
VTT output voltage tolerance to VTTREF	$V_{VTTTOL25}$	$V_{VDDQSNS} = V_{VLDOIN} = 2.5$ V, $V_{S3} = V_{S5} = 5$ V, $I_{VTT} = 0$ A	-21		21	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 2.5$ V, $V_{S3} = V_{S5} = 5$ V, $\|I_{VTT}\| < 1$ A	-31		31	
VTT output voltage tolerance to VTTREF	$V_{VTTTOL18}$	$V_{VDDQSNS} = V_{VLDOIN} = 1.8$ V, $V_{S3} = V_{S5} = 5$ V, $I_{VTT} = 0$ A	-21		21	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 1.8$ V, $V_{S3} = V_{S5} = 5$ V, $\|I_{VTT}\| < 1$ A	-31		31	
VTT output voltage tolerance to VTTREF	$V_{VTTTOL15}$	$V_{VDDQSNS} = V_{VLDOIN} = 1.5$ V, $V_{S3} = V_{S5} = 5$ V, $I_{VTT} = 0$ A	-21		21	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 1.5$ V, $V_{S3} = V_{S5} = 5$ V, $\|I_{VTT}\| < 1$ A	-31		31	
VTT output voltage tolerance to VTTREF	$V_{VTTTOL12}$	$V_{VDDQSNS} = V_{VLDOIN} = 1.2$ V, $V_{S3} = V_{S5} = 5$ V, $I_{VTT} = 0$ A	-21		21	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 1.2$ V, $V_{S3} = V_{S5} = 5$ V, $\|I_{VTT}\| < 1$ A	-31		31	
Source current limit, VTT	$I_{VTTTOCLSRC}$	$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $V_{VTT} = V_{VTTSNS} = 1.19$ V, PGOOD = HI	2.7	3.8	6.2	A
		$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $V_{VTT} = 0$ V	1.4	2.2	3.2	
Sink current limit, VTT	$I_{VTTTOCLSNK}$	$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $V_{VTT} = V_{VTTSNS} = 1.31$ V, PGOOD = HI	2.65	3.6	6	
		$V_{VLDOIN} = V_{VDDQSNS} = 2.5$ V, $V_{VTT} = V_{VDDQ}$	1.4	2.2	3	
Leakage current, VTT	I_{VTTLK}	$V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{VTT} = V_{VDDQSNS}/2$	-11		11	µA
Input bias current, VTTSNS	$I_{VTTBIAS}$	$V_{S3} = 5$ V, $V_{VTTSNS} = V_{VDDQSNS}/2$	-1.1		1.1	
Leakage current	$I_{VTTSNSLK}$	$V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{VTT} = V_{VDDQSNS}/2$	-1		1	
Discharge current, VTT	$I_{VTTDisch}$	$V_{S3} = V_{S5} = V_{VDDQSNS} = 0$ V, $V_{VTT} = 0.5$ V	9.5	17		mA
Transconductance amplifier						
Gain	gm		232	300	364	µS
COMP maximum sink current	$I_{COMPSNK}$	$V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{VDDQSET} = 0$ V, $V_{VDDQSNS} = 2.7$ V, $V_{COMP} = 1.28$ V		13		µA
COMP maximum source current	$I_{COMPSRC}$	$V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{VDDQSET} = 0$ V, $V_{VDDQSNS} = 2.3$ V, $V_{COMP} = 1.28$ V		-13		
COMP high clamp voltage	V_{COMPHI}	$V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{VDDQSET} = 0$ V, $V_{VDDQSNS} = 2.3$ V, $V_{CS} = 0$ V	1.3	1.34	1.38	V
COMP low clamp voltage	V_{COMPLO}	$V_{S3} = 0$ V, $V_{S5} = 5$ V, $V_{VDDQSET} = 0$ V, $V_{VDDQSNS} = 2.7$ V, $V_{CS} = 0$ V	1.17	1.21	1.25	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Limits Min	Limits Typ	Limits Max	Unit
Duty control						
Operating on time	T_{ON}	V_{IN} = 12 V, $V_{VDDQSET}$ = 0 V		520		ns
Startup on time	T_{ON0}	V_{IN} = 12 V, $V_{VDDQSET}$ = 0 V		125		
Minimum on time	$T_{ON(min)}$	T_A = 25°C 4/		100		
Minimum off time	$T_{OFF(min)}$	T_A = 25°C 4/		350		
Zero current comparator						
Zero current comparator offset	V_{ZC}		-6	0	6	mV
Output drivers						
DRVH resistance	R_{DRVH}	Source, I_{DRVH} = -100 mA		3	6	Ω
		Sink, I_{DRVH} = 100 mA		0.9	3	
DRVL resistance	R_{DRVL}	Source, I_{DRVH} = -100 mA		3	6	
		Sink, I_{DRVH} = 100 mA		0.9	3	
Dead time	T_D	LL-low to DRVL-on		10		ns
		DRVL-off to DRVH-on		20		
Internal BST diode						
Forward voltage	V_{FBST}	$V_{V5IN-VBST}$, I_F = 10 mA	0.58	0.8	1.1	V
VBST leakage current	I_{VBSTLK}	V_{VBST} = 34 V, V_{LL} = 28 V, V_{VDDQ} = 2.6 V		0.1	1.11	µA
Protections						
Current limit threshold	V_{OCL}	$V_{PGND-CS}$, PGOOD = HI, V_{CS} < 0.5 V	47	60	70	mV
		$V_{PGND-CS}$, PGOOD = LO, V_{CS} < 0.5 V	18	30	40	
Current sense sink current	I_{TRIP}	V_{CS} > 4.5 V, PGOOD = HI	4	10	20	µA
		V_{CS} > 4.5 V, PGOOD = LO	2	5	10	
TRIP current temperature coefficient	TC_{ITRIP}	$R_{DS(on)}$ sense scheme, On the basic of T_A = 25°C 3/		4500		ppm/°C
Over current protection COMP offset	$V_{OCL(off)}$	($V_{V5IN-CS}$ – $V_{PGND-LL}$), $V_{V5IN-CS}$ = 60 mV, V_{CS} > 4.5 V	-7	0	7	mV
Current limit threshold setting range	$V_{R(trip)}$	$V_{V5IN-CS}$	30		150	
Power good comparator						
VDDQ power good threshold	$V_{TVDDQPG}$	PG in from lower	92	95	98	%
		PG in from higher	102	105	108	%
		PG hysteresis		5		%
PGOOD sink current	$I_{PG(max)}$	V_{VTT} = 0 V, V_{PGOOD} = 0.5 V	2.3	7.5		mA
PGOOD delay time	$T_{PG(del)}$	Delay for PG in	78	130	205	µs

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

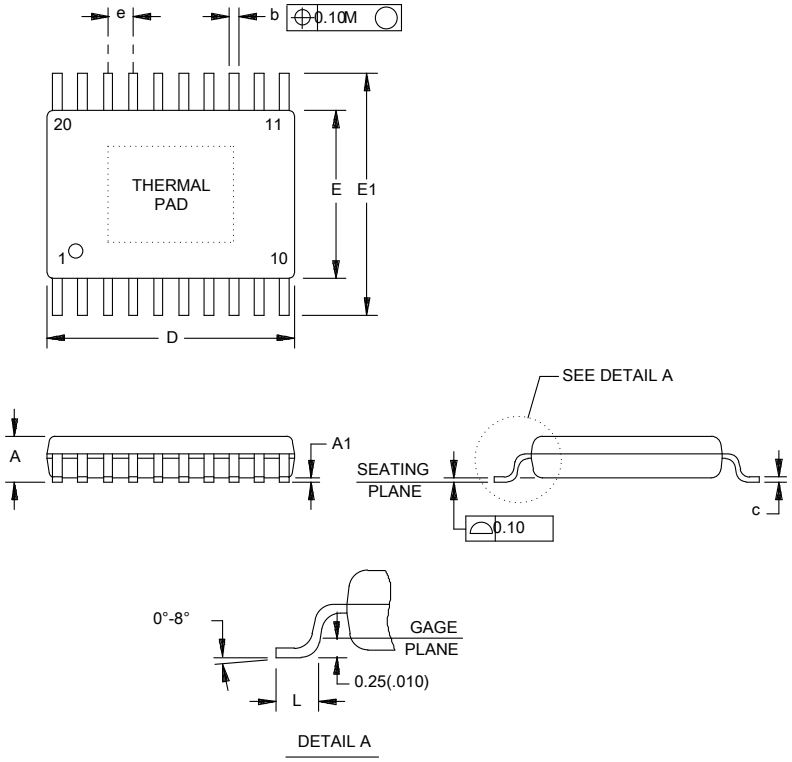
Test	Symbol	Conditions 2/	Limits Min		Limits Max	Unit
Undervoltage Lockout/Logic Threshold						
V5IN UVLO threshold voltage	V_{UVV5IN}	Wake up	3.6	4	4.4	V
		Hysteresis	0.19	0.3	0.41	
MODE threshold	V_{THMODE}	No discharge	4.7			
		Non tracking discharge			0.08	
VDDQSET threshold voltage	$V_{THVDDQSET}$	2.5 V output	0.075	0.150	0.255	
		1.8 V output	3.45	4	4.55	
High level input voltage	V_{IH}	S3, S5	2.2			
Low level input voltage	V_{IL}	S3, S5			0.3	
Hysteresis voltage	V_{IHYST}	S3, S5		0.2		
Logic input leakage current	V_{INLEAK}	S3, S5, MODE	-1		1	µA
Input leakage/bias current	$V_{INVDDQSET}$	VDDQSET	-1		1	
Undervoltage and overvoltage protection						
VDDQ OVP trip threshold voltage	V_{OVP}	OVP detect	109	115	120	%
		Hysteresis		5		%
VDDQ OVP propagation delay	t_{OVPDEL}			1.5		µs
Output UVP trip threshold	V_{UVP}	UVP detect		70		%
		Hysteresis		10		%
Output UVP propagation delay	T_{UVPDEL}			32		cycle
Output UVP enable delay	T_{UVPEN}			1007		
Thermal Shutdown						
Thermal SDN threshold 3/	T_{SDN}	Shutdown temperature		160		°C
		Hysteresis		10		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ T_J = -55°C to 125°C, $T_J = T_A$, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted).

3/ Specified by design. Not production test.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.25 TYP		L	0.50	0.70
D	6.40	6.60			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
4. This package is designed to be soldered to a thermal pad on the board. Refer to manufacturer for information regarding recommended board layout.
5. See the additional figure in the manufacturer Product data sheet for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VLDOIN	20	VBST
2	VTT	19	DRVH
3	VTTGND	18	LL
4	VTTSNS	17	DRVL
5	GND	16	PGND
6	MODE	15	CS
7	VTTREF	14	V5IN
8	COMP	13	PGOOD
9	VDDQSNS	12	S5
10	VDDQSET	11	S3

FIGURE 2. Terminal connections.

Case outline X			
Terminal		I/O	Description
Name	Number		
COMP	8	I/O	Output of the transconductance amplifier for phase compensation. Connect to V5IN to disable gm amplifier and use D-CAP mode.
CS	15	I/O	Current sense comparator input (-) for resistor current sense scheme. Or overcurrent trip voltage setting input for $R_{DS(on)}$ current sense scheme if connected to V5IN through the voltage setting resistor
DRVH	19	O	Switching (top) MOSFET gate drive output.
DRVL	17	O	Rectifying (bottom) MOSFET gate drive output.
GND	5		Signal ground. Connect to minus terminal of the VTT LDO output capacitor.
LL	18	I/O	Switching (top) MOSFET gate driver return. Current sense comparator input (-) for $R_{DS(on)}$ current sense
MODE	6	I	Discharger mode setting pin. See VDDQ and VTT Discharger control in manufacturer data.
PGND	16		Ground for rectifying (bottom) MOSFET gate driver (PWP, RGE). Also current sense comparator input (+) and ground for powergood circuit (PWP).
PGOOD	13	O	Powergood signal open drain output. In HIGH state when VDDQ output voltages is within the target range.
S3	11	I	S3 signal input
S5	12	I	S5 signal input
V5IN	14	I	5 V power supply input for internal circuits (PWP) and MOSFET gate driver (PWP, RGE)
VBST	20	I/O	Switching (top) MOSFET driver bootstrap voltage input.
VDDQSET	10	I	VDDQ output voltage setting pin. See VDDQ output voltage selection in manufacturer data.
VDDQSNS	9	I/O	VDDQ reference input for VTT and VTTREF. Power supply for the VTTREF. Discharger current sinking terminal for VDDQ Non Tracking discharger. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to V5IN or GND.
VLDOIN	1	I	Power supply for the VTT LDO
VTT	2	O	Power output for the VTT LDO
VTTGND	3		Power ground output for the VTT LDO
VTTREF	7	O	VTTREF buffered reference output.
VTTSNS	4	I	Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor.

FIGURE 3. Terminal function.

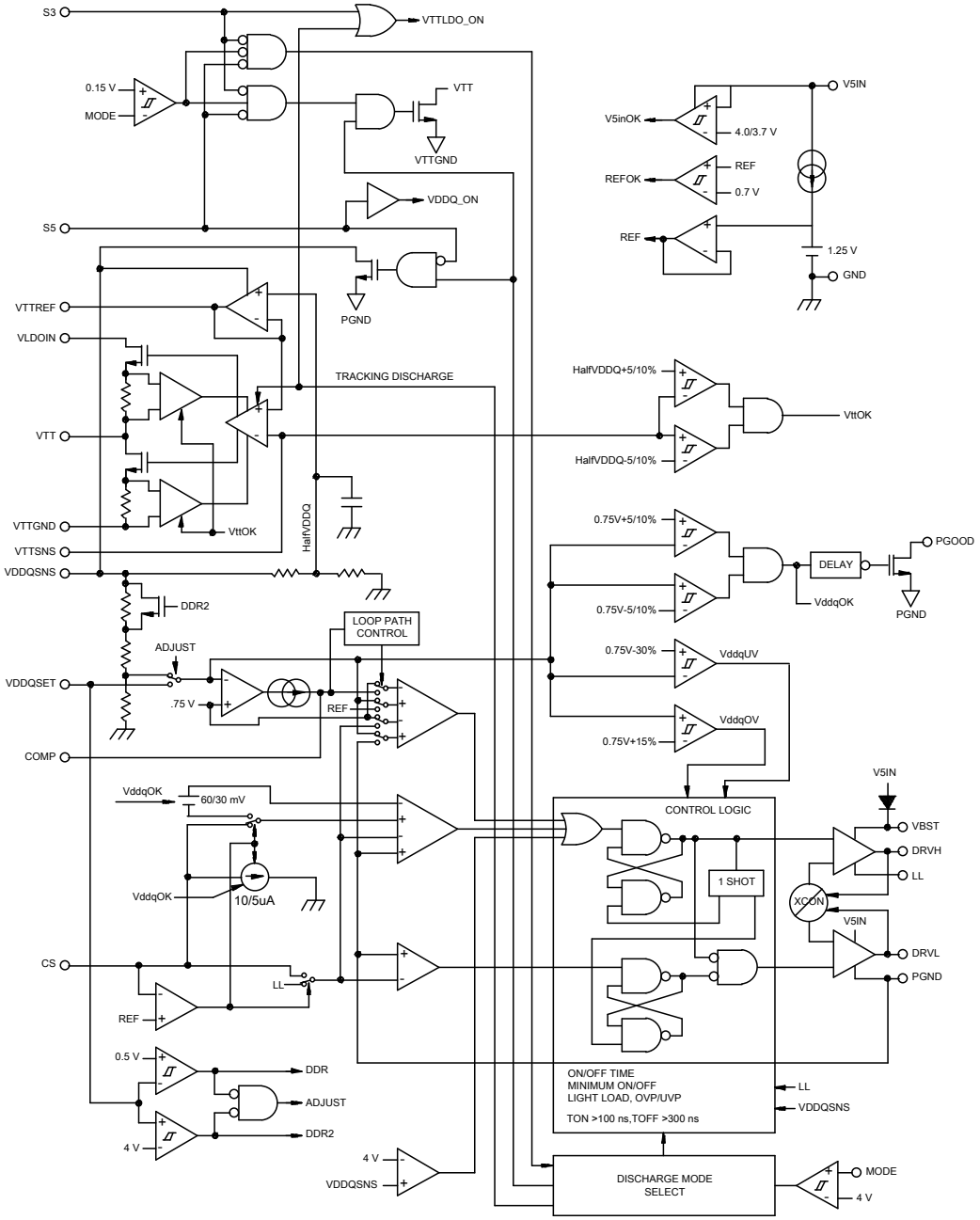


FIGURE 3. Functional block diagram (case X).

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Transport media	Vendor part number
V62/12602-01XE	01295	51116M	Tube	TPS51116MPWPEP
			Tape and real	TPS51116MPWPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493