REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-04-16	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-09-18	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13									

PMIC N/A

Original date of drawing

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12-12-14

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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, ENHANDCED, LOW INPUT VOLTAGE MODE SYNCHRONOUS BUCK CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/12601
REV B		PAGE 1 OF 11

AMSC N/A

5962-V154-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance enhanced, low input voltage mode synchronous buck controller microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12601	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS40021-EP	Enhanced, low input voltage mode synchronous buck controller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage range, (V_{IN}):
- SS/SD, VDD, PVDD, OSNS ..... -0.3 V to 6.0 V
- BOOT2, BOOT1 ..... V_{SW} + 6.0 V
- SW ..... -3.0 V to 10.5 V
- SWT (SW transient < 50 ns) ..... -5.0 V
- FB, ILIM ..... -0.3 V to 6.0 V

Output voltage range, (V_{OUT}): COMP, PWRGD, RT ..... -0.3 V to 6.0 V
Sink current, (I_S): PWDGD ..... 10 mA
Maximum junction temperature, (T_J) ..... 150°C
Storage temperature range (Tstg) ..... -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Thermal resistance

Thermal metric 2/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 3/	38.3	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 4/	28	°C/W
Junction to board thermal resistance, θ_{JB} 5/	9	°C/W
Junction to top characterization parameter, Ψ_{JT} 6/	0.4	°C/W
Junction to board characterization parameter, Ψ_{JB} 7/	8.9	°C/W
Junction to case (bottom) thermal resistance, θ_{JCbot} 8/	2.9	°C/W

1.4 Recommended operating conditions.

Input voltage, (V_{IN}) ..... 2.25 V to 5.5 V
Operating temperature range, (T_J) ..... -55°C to 125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

2/ For more information about traditional and new thermal metrics, see manufacturer data.

3/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-k-board, as specified in JESD51-7, in an environment described in JESD51-2a.

4/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

6/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

7/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

8/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD51-8	–	Junction-to-board thermal resistance Theta-JB or $R\theta_{JB}$

(Copies of these documents are available online at https://www.jedec.org.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88	-	Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available from https://www.ansi.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Internal block diagram. The internal block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Input Supply					
Input voltage range	V_{DD}		2.25	5.50	V
PVDD pin voltage	VP_{VDD}	V_{DD} = 3.3 V		5.20	V
Switching current	I_{DD}	500 KHz, No load on HDRV, LDRV		5.0	mA
Quiescent current		FB = 0.8 V		3.0	mA
Shutdown current		SS/SD = 0 V, Outputs OFF		1.0	mA
Minimum on voltage	V_{UVLO}		1.95	2.15	V
Hysteresis			72	200	mV
Oscillator					
Accuracy	f_{OSC}	2.25 V ≤ V_{DD} ≤ 5.00 V, RT = 69.8 kΩ	405	575	kHz
		2.25 V ≤ V_{DD} ≤ 5.00 V, RT = 34.8 kΩ	740	1100	kHz
Ramp voltage	V_{RAMP}	V_{PEAK} - V_{VAL}	0.80	1.07	V
Ramp valley voltage	V_{VAL}		0.24	0.41	V
PWM					
Maximum duty cycle	d_{MAX}	V_{OSNS} = V_{DD}, R_T = 34.8 kΩ, V_{DD} = 3.3 V, FB = 0 V	85		%
		V_{OSNS} = V_{DD}, R_T = 70 kΩ, V_{DD} = 5.0 V, FB = 0 V	90		%
Minimum duty cycle	d_{MIN}			0 TYP	%
Minimum HDRV on-time 3/	t_{MIN}			250 TYP	ns
Error Amplifier					
Feedback input voltage	V_{FB}	2.25 V ≤ V_{DD} ≤ 5.00 V	0.683	0.701	V
Input bias current	I_{BIAS}			130	nA
High level output voltage	V_{OH}	I_{OH} = 0.5 mA, V_{FB} = GND	2.0		V
Low level output voltage	V_{OL}	I_{OL} = 0.5 mA, V_{FB} = V_{DD}		0.15	V
High level output source current	I_{OH}	V_{FB} = GND	2.7		mA
Low level output sink current	I_{OL}	V_{FB} = V_{DD}	3		mA
Gain bandwidth 4/	G_{BW}			10 TYP	MHz
Open loop gain	A_{OL}		53		dB
Current limit					
Current limit sink current	I_{SINK}	2.25 V ≤ V_{DD} ≤ 5.00 V, R_T = 69.8 kΩ	165	215	µA
Current limit offset voltage	V_{OS}		-20	20	mV
Minimum HDRV on time in overcurrent	t_{ON}	V_{DD} = 3.3 V		300	ns
Switching leading edge blanking pulse time 4/				140 TYP	ns
Soft start cycles	t_{SS}			6 TYP	cycles
Current limit input voltage range	V_{ILIM}		2	V_{DD}	V
Soft start					
Soft start source current	I_{SS}	Outputs = OFF	2.0	5.4	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Shutdown					
Shutdown threshold voltage	V_{SD}		0.2	0.29	V
Device enable threshold voltage	V_{EN}		0.25	0.32	V
Output Driver					
High side driver pull up resistance	R_{HDHI}	$V_{(BOOT1)} – V_{(SW)}$ = 3.3 V, I_{SOURCE} = 100 mA	1.0	5.0	Ω
High side driver pull down resistance	R_{HDLO}	$V_{(BOOT1)} – V_{(SW)}$ = 3.3 V, I_{SINK} = 100 mA	0.7	3.0	Ω
Low side driver pull up resistance	R_{LDHI}	P_{VDD} = 3.3 V, I_{SOURCE} = 100 mA	1.0	5.0	Ω
Low side driver pull down resistance	R_{LDLO}	P_{VDD} = 3.3 V, I_{SINK} = 100 mA	0.41	1.50	Ω
Low side driver rise time	t_{LRISE}	C_{LOAD} = 1 nF		35	ns
Low side driver fall time	t_{LFALL}			25	ns
High side driver rise time	t_{HRISE}			35	ns
High side driver fall time	t_{HFALL}			25	ns
Thermal Shutdown					
Shutdown temperature 4/			165	TYP	°C
Hysteresis 4/			15	TYP	°C
Charge Pump					
$R_{DS(on)}$ VDD to BOOT2	R_{VB2}	V_{DD} = 5.0 V, I_{SOURCE} = 10 mA	2.8	10.4	Ω
$R_{DS(on)}$ BOOT2 to PVDD	R_{B2P}	V_{DD} = 5.0 V, I_{SOURCE} = 10 mA	2.8	8.4	Ω
$R_{DS(on)}$ PVDD to BOOT1	R_{PB1}	V_{DD} = 5.0 V, I_{SOURCE} = 10 mA	2.9	8.9	Ω
Power Good					
Pull down voltage		V_{OSNS} = 0.8 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	50	140	mV
Output sense high to power good low delay time		0.7 V ≤ V_{OSNS} ≤ 0.8 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	6	14	µs
Output sense low to power good low delay time		0.6 V ≤ V_{OSNS} ≤ 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	6	14	µs
Shut down high to power good high delay time		V_{OSNS} = 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V, 0.0 V ≤ $V_{SS/SD}$ ≤ 0.4 V	2	6	µs
Shut down low to power good low delay time			0.5	3.0	µs
Output sense high to nominal to power good high delay time		0.7 V ≤ V_{OSNS} ≤ 0.8 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	140	1000	ns
Output sense high to nominal to power good high delay time		0.6 V ≤ V_{OSNS} ≤ 0.7 V, I_{PWRGD} = 0.5 mA, V_{DD} = 3.3 V	140	1000	ns
Transient comparators					
Overvoltage output threshold voltage	V_{OV}	Reference V_{FB}	23	35	mV
Hysteresis			8	22	mV
Undervoltage output threshold voltage	V_{UV}		-37	-25	mV
Hysteresis			8	22	mV
OSNS minimum disable voltage	V_{DIS}	Referenced to V_{DD}	0.5		V

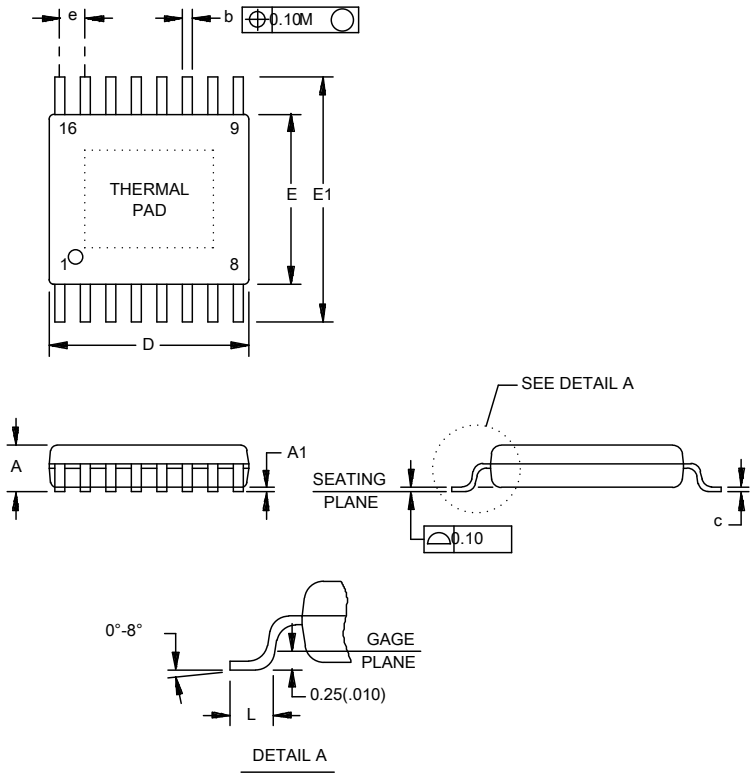
See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
Synchronization					
Synchronization enable low threshold voltage	V_{ENSY}			0.7	V
Synchronization current limit enable threshold voltage	V_{BLNK}	Referenced to VDD	-0.7		V
Minimum synchronization input pulse width	t_{MIN}			50	ns
Predictive Delay					
Sense voltage to modulate delay	V_{SWP}		-200	TYP	mV
Maximum delay modulation	t_{LDHD}	LDRV OFF to HDRV ON	40	90	ns
Counter delay/bit time			2.5	6.2	ns
Maximum delay modulation	t_{HDLD}	HDRV OFF to LDRV ON	80	TYP	ns
Counter delay/bit time			5	TYP	ns
Rectifier Zero current comparator					
Zero current blanking time 4/	t_{ZBLNK}		150	TYP	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ T_J = -55°C to 125°C, $T_J = T_A$, V_{DD} = 5.0 V (unless otherwise noted).
3/ Operation below the minimum on time could result in overlap of the HDRV and LDRV outputs.
4/ Specified by design. Not production tested.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millim eters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.25 TYP		L	0.50	0.70
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
4. This package is designed to be soldered to a thermal pad on the board. Refer to manufacturer for information regarding recommended board layout.
5. See the additional figure in the manufacturer Product data sheet for details regarding the exposed thermal pad features and dimensions.
6. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	ILIM/SYNC	9	PWRGD
2	VDD	10	PGND
3	OSNS	11	LDRV
4	FB	12	PVDD
5	COMP	13	BOOT2
6	SS/SD	14	SW
7	RT	15	HDRV
8	SGND	16	BOOT1

FIGURE 2. Terminal connections.

Terminal name	Terminal number	I/O	Description
BOOT1	16	I	This pin provides a bootstrapped supply for the high side FET driver, enabling the gate of the high side FET to be driven above the input supply rail. Connect a capacitor from this pin to the SW pin.
BOOT2	13	I	This pin provides a secondary bootstrapping necessary for generation of PVDD. Connect a capacitor from this pin to the SW.
COMP	5	O	Output of the error amplifier. refer to Electrical Characteristics table for loading constraints.
FB	4	I	Inverting input of the error amplifier. In normal operation, V_{FB} is equal to the internal reference level of 690 mV.
HDRV	15	O	The gate drive output for the high side N-channel MOSFET switch is bootstrapped to near PVDD for good enhancement of the high side switch. The HDRV switches from BOOT1 to SW.
ILIM/SYNC	1	I	The current limit pin is used to set the current limit threshold. A current sink from this pin to GND sets the threshold voltage for output short circuit current across a resistor connected to VDD. Synchronization is accomplished by pulling IMAX to less than 1 V for a period greater than the minimum pulse width and then releasing. An open collector or drain device should be used. These pulses must be of higher frequency than the free running frequency of the local oscillator.
LDRV	11	O	Gate drive output for the low side synchronous rectifier N-channel MOSFET. LDRV switches from PVDD to PGND.
OSNS	3	O	The output sense pin is connected to a resistor divider from VOUT to GND (identical to the main feedback loop) and is used to sense power good condition and provides reference for the transient comparators
PGND	10	O	Power (high current) ground used by LDRV
PWRGD	9		Power good. This is an open-drain output which connects to the supply via an external resistor.
PVDD	12	O	This pin is the regulated output of the charge-pump and provides the supply voltage for the LDRV driver stage. PVDD also drives the bootstrap circuit which generates the voltage on BOOT1.
RT	7	I	External pin for programming the oscillator frequency. Connected a resistor between this pin and GND.
SGND	8		Signal ground
SS/SD	6	I	The soft-start/shutdown pin provides user programmable soft-start timing and shutdown capability for the controller.

FIGURE 3. Terminal functions

Terminal name	Terminal number	I/O	Description
SW	14	I	This pin, used for overcurrent, zero current, and in the anti-cross conduction sensing is connected to the switched node on the converter. Output short circuit is detected by sensing the voltage at this pin with respect to VDD while the high-side switch is on. Zero current is detected be sensing the pin voltage with respect to ground when the low side rectifier MOSFET is on.
VDD	2	I	Power input for the device. Maximum voltage is 5.5 V. De-coupling of this pin is required.

FIGURE 3. Terminal functions - Continued

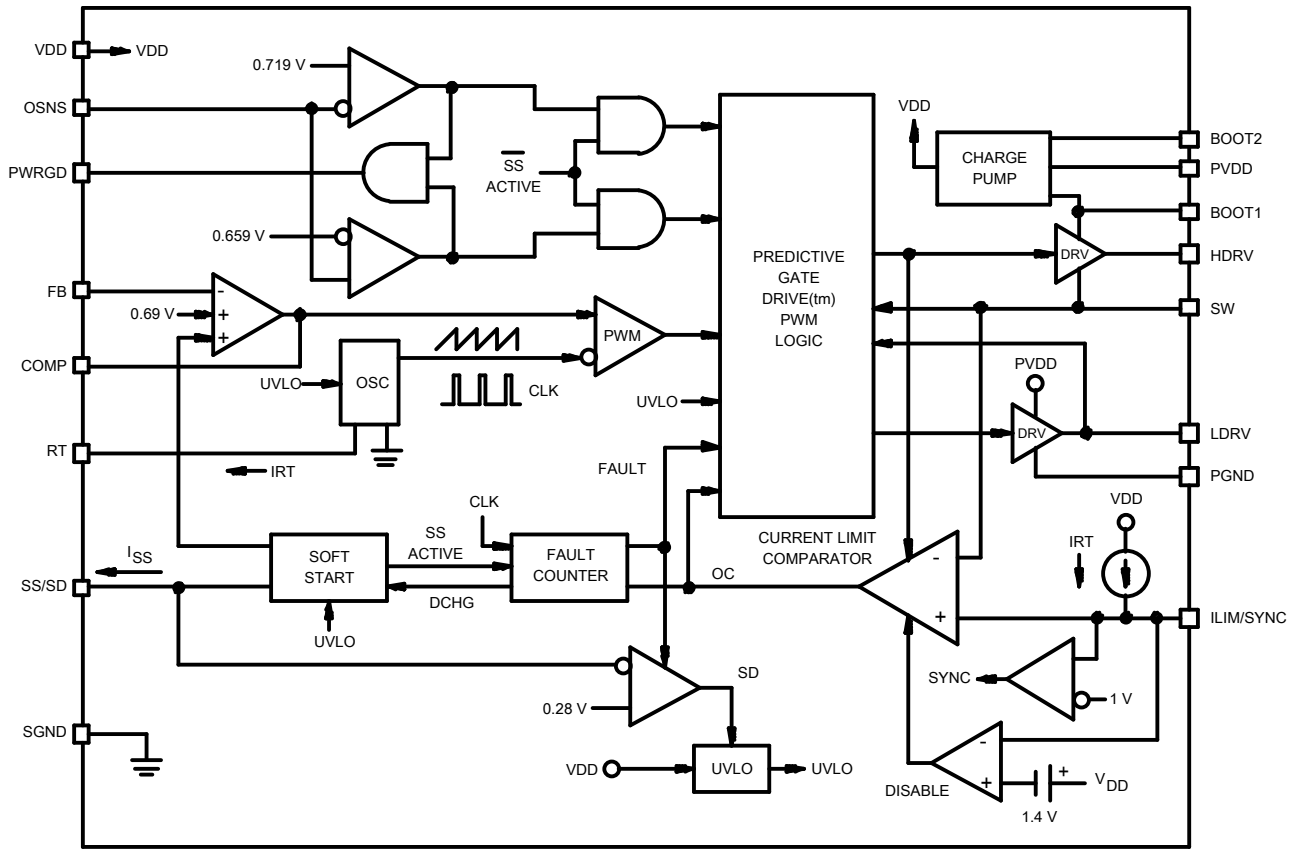


FIGURE 4. Internal block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Transport media	Vendor part number
V62/12601-01XE	01295	40021M	Tape and real	TPS40021MPWPREP
			Tube	TPS40021MPWPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243