REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I, input offset voltage test; with T_A = 25°C delete 9 mV and substitute 6 mV, with -40°C ≤ T_A ≤ 125°C, delete 15 mV and substitute 8 mV. Table I, input offset current test, with -40°C ≤ T_A ≤ 125°C delete 20 nA and substitute 2 nA. Table I, input bias current test, add -40°C ≤ T_A ≤ 125°C, delete 50 nA and substitute 20 nA. Table I, large signal differential voltage amplification test, add -40°C ≤ T_A ≤ 125°C for 5 V/mV min limit. Table I, common mode rejection ratio test, delete 75 dB and substitute 80 dB. Table I, slew rate at unity gain test, delete 5 V/µs and substitute 8 V/µs. - ro	13-01-09	C. SAFFLE
B	Make corrections to pins 2 and 10 as specified in figure 2 Terminal connections. Make change to Top side marking as specified under paragraph 6.3. Update document paragraphs to current requirements. - ro	21-01-26	J. ESCHMEYER
C	Add device type 02. Make changes to paragraph 1.3, Table I and figure 2. - ro	23-06-21	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C											
SHEET	1	2	3	4	5	6	7	8	9	10	11											

PMIC N/A

Original date of drawing
YY-MM-DD
11-11-07

PREPARED BY
Phu H. Nguyen

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, DIGITAL-LINEAR, LOW NOISE JFET INPUT OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/11621
REV C		PAGE 1 OF 11

AMSC N/A

5962-V113-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low noise JFET input operational amplifier microcircuit, with an operating temperature range of -40°C to +125°C for device type 01 and -55°C to +125°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11621	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TL074Q-EP	Low noise JFET input operational amplifier
02	TL074M-EP	Low noise JFET input operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MS-012	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Maximum supply voltage: 2/

V_{CC+}	18 V
V_{CC-}	18 V
Maximum differential input voltage (V_{ID})	±30 V 3/
Maximum input voltage (V_I)	±15 V 2/ 4/
Duration of output short circuit	Unlimited 5/
Thermal resistance, junction to case (θ_{JC})	51.5°C/W 6/ 7/
Thermal resistance, junction to ambient (θ_{JA})	86°C/W 7/
Maximum operating virtual junction temperature (T_J)	150°C
Storage temperature range (T_{stg})	-65°C to 150°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

3/ Differential voltages are at IN+, with respect to IN-.

4/ The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

5/ The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6/ Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

7/ The package thermal impedance is calculated in accordance with JESD 51-7.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Symbol diagram. The symbol diagram shall be as shown in figure 3.

3.5.4 Schematic diagram. The schematic diagram shall be as shown in figure 4.

3.5.5 Unity gain amplifier. The unity gain amplifier shall be as shown in figure 5.

3.5.6 Gain of 10 inverting amplifier. The gain of 10 inverting amplifier shall be as shown in figure 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	T_A 4/	Device type	Limits		Unit
					Min	Max	
Input offset voltage	V_{IO}	V_O = 0, R_S = 50 Ω	25°C	01, 02		6	mV
			-40°C ≤ T_A ≤ 125°C	01		8	
			-55°C ≤ T_A ≤ 125°C	02		8	
Temperature coefficient of input offset voltage	α_{VIO}	V_O = 0, R_S = 50 Ω	-40°C ≤ T_A ≤ 125°C	01	18 typical		µV/°C
			-55°C ≤ T_A ≤ 125°C	02	18 typical		
Input offset current	I_{IO}	V_O = 0	25°C	01, 02		100	pA
			-40°C ≤ T_A ≤ 125°C	01		2	nA
			-55°C ≤ T_A ≤ 125°C	02		2	
Input bias current	I_{IB}	V_O = 0	25°C	01, 02		200	pA
			-40°C ≤ T_A ≤ 125°C	01		20	nA
			-55°C ≤ T_A ≤ 125°C	02		20	
Common mode input voltage range	V_{ICR}		25°C	01, 02	±11		V
Maximum peak output voltage swing	V_{OM}	R_L = 10 kΩ	25°C	01, 02	±12		V
		R_L ≥ 10 kΩ	-40°C ≤ T_A ≤ 125°C	01	±12		
			-55°C ≤ T_A ≤ 125°C	02	±12		
		R_L ≥ 2 kΩ	-40°C ≤ T_A ≤ 125°C	01	±10		
			-55°C ≤ T_A ≤ 125°C	02	±10		
Large signal differential voltage amplification	A_{VD}	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	01, 02	35		V/mV
			-40°C ≤ T_A ≤ 125°C	01	15		
			-55°C ≤ T_A ≤ 125°C	02	15		
Unity gain bandwidth	B_1		25°C	01, 02	3 typical		MHz
Input resistance	r_i		25°C	01, 02	10^{12} typical		Ω
Common mode rejection ratio	CMRR	V_{IC} = V_{ICmin}, V_O = 0, R_S = 50 Ω	25°C	01, 02	80		dB
Supply voltage rejection ratio ($\Delta V_{CC}\pm/\Delta V_{IO}$)	k_{SVR}	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	01, 02	80		dB
Supply current (each amplifier)	I_{CC}	V_O = 0, no load	25°C	01, 02		2.5	mA
Crosstalk attenuation	V_{O1}/V_{O2}	A_{VD} = 100	25°C	01, 02	120 typical		dB

See footnotes at end of the table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/ 3/	T_A 4/	Device type	Limits		Unit
					Min	Max	
Operating characteristics.							
Slew rate at unity gain	SR	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, see figure 1	25°C	01, 02	8		V/µs
Rise time overshoot factor	t_r	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, see figure 1	25°C	01, 02	0.1	typical	µs
					20	typical	%
Equivalent input noise voltage	V_n	f = 1 kHz, R_S = 20 Ω	25°C	01, 02	18	typical	$nV/\sqrt{Hz}$
		f = 10 Hz to 10 kHz, R_S = 20 Ω			4	typical	µV
Equivalent input noise current		R_S = 20 Ω, f = 1 kHz	25°C	01, 02	0.01	typical	$pA/\sqrt{Hz}$
Total harmonic distortion	THD	$V_I$rms = 6 V, A_{VD} = 1, $R_L \geq 2$ kΩ, $R_S \leq 1$ kΩ, f = 1 kHz	25°C	01, 02	0.003	typical	%

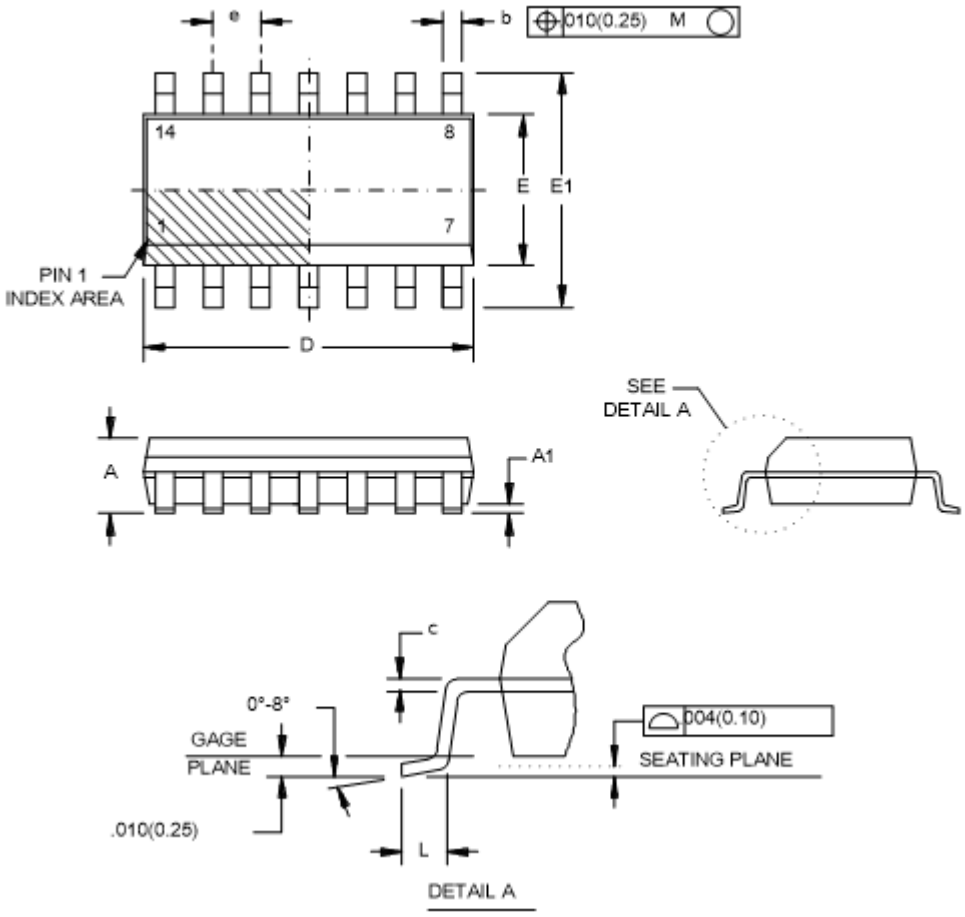
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $V_{CC\pm}$ = ±15 V (unless otherwise noted).

3/ Input bias currents of an FET input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

4/ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

Case X



Dimen sions									
Symbol	Inches		Millimeters		Symbol	Inches		Millim eters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.069		1.75	E	.150	.157	3.80	4.00
A1	.004	.010	0.10	0.25	E1	.228	.244	5.80	6.20
b	.012	.020	0.31	0.51	e	.050 BSC		1.27 BSC	
c	.005	.010	0.13	0.25	L	.016	.050	0.40	1.27
D	.337	.344	8.55	8.75					

NOTES:
1. All linear dimensions are in inches.
2. This drawing is subject to change without notice.
3. Dimension D body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006. inches (0.15 mm) each side.
4. Dimension E body width does not include interlead flash. Interlead flash shall not exceed .017 inch (0.43 mm) each side.
5. Reference JEDEC MS-012 variation AB.

FIGURE 1. Case outline.

Case outline	X		
Device types	01, 02		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1OUT	8	3OUT
2	1IN-	9	3IN-
3	1IN+	10	3IN+
4	V_{CC+}	11	V_{CC-}
5	2IN+	12	4IN+
6	2IN-	13	4IN-
7	2OUT	14	4OUT

FIGURE 2. Terminal connections.

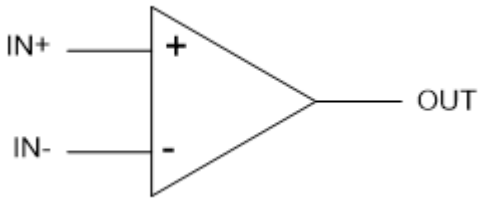


FIGURE 3. Symbol diagram.

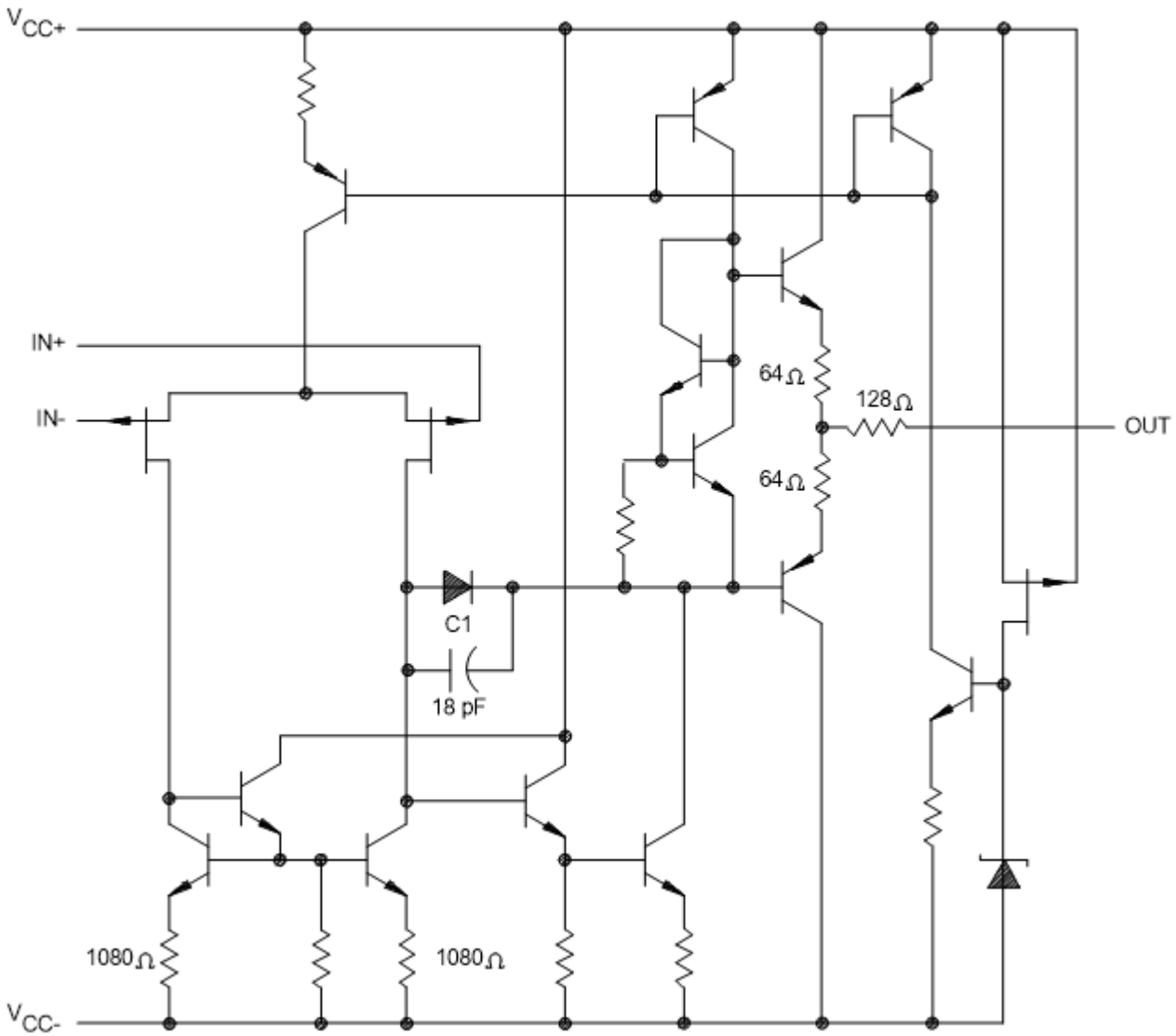


FIGURE 4. Schematic diagram.

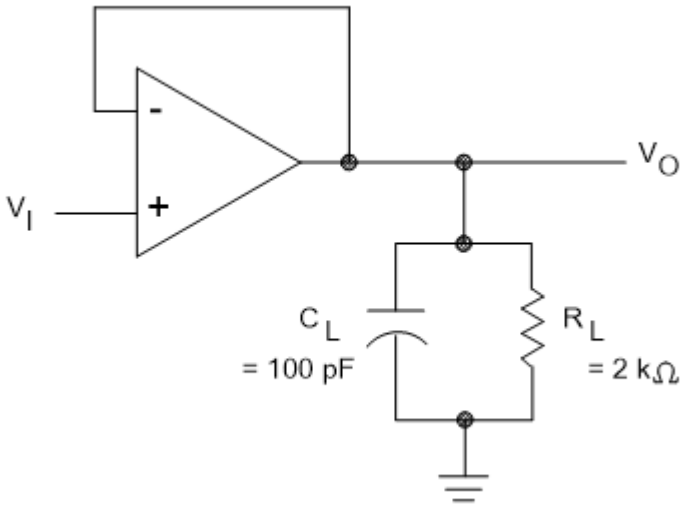


FIGURE 5. Unity gain amplifier.

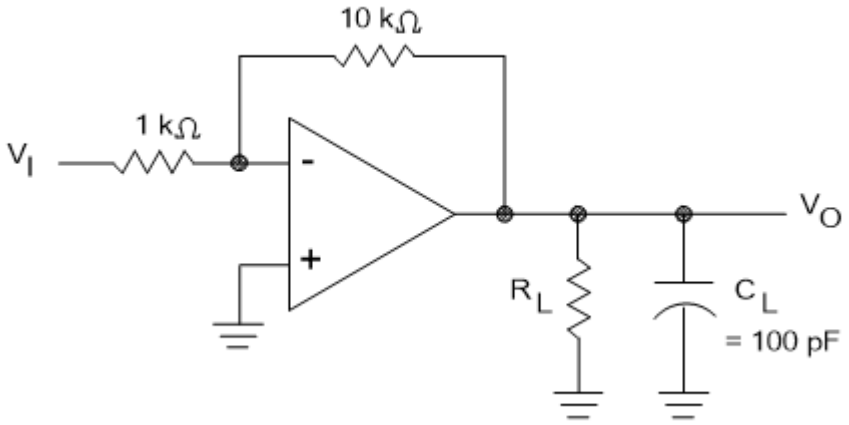


FIGURE 6. Gain of 10 inverting amplifier.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/11621-01XE	01295	TL074Q	TL074QDREP
V62/11621-02XE	01295	TL074M	TL074MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243