

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	17-11-16	Thomas M. Hess
B	Correct number of pin in section 1.2.2. - PHN	18-09-05	Thomas M. Hess
C	Update boilerplate paragraphs to current VID description requirements. - PHN	23-12-12	Muhammad A. Akbar



Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C				
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	<b>PREPARED BY</b> Phu H. Nguyen	<b>DLA LAND AND MARITIME</b> COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/landandmaritime">https://www.dla.mil/landandmaritime</a>
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Original date of drawing YY MM DD  11-10-27	<b>CHECKED BY</b> Phu H. Nguyen		<b>TITLE</b> MICROCIRCUIT, DIGITAL, CURRENT LIMITED POWER DISTRIBUTION SWITCH, MONOLITHIC SILICON	
	<b>APPROVED BY</b> Thomas M. Hess			
	<b>SIZE</b> <b>A</b>	<b>CODE IDENT. NO.</b> <b>16236</b>		<b>DWG NO.</b> <b>V62/11620</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance current limited power distribution switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/11620</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS2041B-EP	Current limited power distribution switch

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	JEDEC MO-178	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage range (IN) ( $V_{I(IN)}$ ) .....	-0.3 V to +6 V	2/
Output voltage range (OUT) ( $V_{O(OUT)}$ ) .....	-0.3 V to +6 V	2/
Input voltage range ( $\overline{EN}$ ) ( $V_{I(\overline{EN})}$ ) .....	-0.3 V to +6 V	
Voltage range ( $\overline{OC}$ ) ( $V_{I(\overline{OC})}$ ) .....	-0.3 V to +6 V	
Continuous output current ( $I_{O(OUT)}$ ) .....	Internally limited	
Continuous total power dissipation .....	See dissipation ratings table.	
Operating virtual junction temperature range ( $T_J$ ) .....	-55°C to 125°C	
Storage temperature range ( $T_{stg}$ ) .....	-65°C to 150°C	
Lead temperature, soldering (1.6 mm (1/16 in) from case for 10 s) .....	260°C	
Electrostatic discharge (ESD) protection:		
Human Body Model (HBM) (H2) .....	2500 V	
Machine Model (MM) (M0) .....	50 V	
Charged Device Model (CDM) (C5) .....	1500 V	
Dissipating ratings table:		

Package	$T_A \leq 25^\circ\text{C}$ Power ratings	Derating factor Above $T_A = 25^\circ\text{C}$	$T_A = 25^\circ\text{C}$ Power rating	$T_A = 85^\circ\text{C}$ Power rating
Case X	285 mW	2.85 mW/°C	155 mW	114 mW

1.4 Recommended operating conditions.

Input voltage (IN) ( $V_{I(IN)}$ ) .....	2.7 V to 5.5 V
Input voltage ( $\overline{EN}$ ) ( $V_{I(\overline{EN})}$ ) .....	0 V to 5.5 V
Continuous output current (OUT) ( $I_{O(OUT)}$ ) .....	0 mA to 500 mA
Operating virtual junction temperature ( $T_J$ ) .....	-55°C to 125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ All voltage are with respect to GND

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### 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

#### 3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections and terminal functions. The terminal connections and terminal functions shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Test circuit and voltage waveforms. The test circuit and voltage waveforms shall be as shown in figure 4.

3.5.5 Turn on delay and rise time with 1  $\mu$ F load. The turn on delay and rise time with 1  $\mu$ F load shall be as shown in figure 5.

3.5.6 Turn off delay and fall time with 1  $\mu$ F load. The turn off delay and fall time with 1  $\mu$ F load shall be as shown in figure 6.

3.5.7 Turn on delay and rise time with 100  $\mu$ F load. The turn on delay and rise time with 100  $\mu$ F load shall be as shown in figure 7.

3.5.8 Turn off delay and fall time with 100  $\mu$ F load. The turn off delay and fall time with 100  $\mu$ F load shall be as shown in figure 8.

3.5.9 Short circuit current, device enables into short. The short circuit current, device enabled into short shall be as shown in figure 9.

3.5.10 Inrush current with different load capacitance. The inrush current with different load capacitance shall be as shown in figure 10.

3.5.11 3  $\Omega$  load connected to enabled device. The 3  $\Omega$  load connected to enabled device shall be as shown in figure 11.

3.5.12 2  $\Omega$  load connected to enabled device. The 2  $\Omega$  load connected to enabled device shall be as shown in figure 12.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	T <sub>J</sub>	Limits		Unit	
				Min	Max		
<b>Power Switch</b>							
Static drain source on state resistance, 5 V or 3.3 V operation	r <sub>DS(on)</sub>	V <sub>I(IN)</sub> = 5 V or 3.3 V, I <sub>o</sub> = 0.5 A	-55°C ≤ T <sub>J</sub> ≤ 125°C		135	mΩ	
Static drain source on state resistance, 2.7 V operation 4/		V <sub>I(IN)</sub> = 2.7 V, I <sub>o</sub> = 0.5 A	-55°C ≤ T <sub>J</sub> ≤ 125°C		150		
Rise time, output 4/	t <sub>r</sub>	V <sub>I(IN)</sub> = 5.5 V	T <sub>J</sub> = 25°C		1.5	ms	
		V <sub>I(IN)</sub> = 2.7 V			1		
Fall time, output 4/	t <sub>f</sub>	V <sub>I(IN)</sub> = 5.5 V			0.05		0.5
		V <sub>I(IN)</sub> = 2.7 V			0.05		0.5
<b>Enable Input (<math>\overline{EN}</math>)</b>							
High level input voltage	V <sub>IH</sub>	2.7 V ≤ V <sub>I(IN)</sub> ≤ 5.5 V		2		V	
Low level input voltage	V <sub>IL</sub>	2.7 V ≤ V <sub>I(IN)</sub> ≤ 5.5 V			0.8	V	
Input current	I <sub>i</sub>	V <sub>I(<math>\overline{EN}</math>)</sub> = 0 V or 5.5 V		-0.5	0.5	μA	
Turn on time 4/	t <sub>on</sub>	C <sub>L</sub> = 100 μF, R <sub>L</sub> = 10 Ω			3	ms	
Turn off time 4/	t <sub>off</sub>	C <sub>L</sub> = 100 μF, R <sub>L</sub> = 10 Ω			10	ms	
<b>Current limit</b>							
Short circuit output current		V <sub>I(IN)</sub> = 5 V, OUT connected to GND, device enable into short circuit	T <sub>J</sub> = 25°C	0.65	1.25	A	
			-55°C ≤ T <sub>J</sub> ≤ 125°C	0.6	1.3		
<b>Supply current</b>							
Supply current, low level output		No load on OUT, V <sub>I(<math>\overline{EN}</math>)</sub> = 5.5 V or V <sub>I(<math>\overline{EN}</math>)</sub> = 0 V	T <sub>J</sub> = 25°C		1	μA	
			-55°C ≤ T <sub>J</sub> ≤ 125°C		5		
Supply current, high level output		No load on OUT, V <sub>I(<math>\overline{EN}</math>)</sub> = 0 V or V <sub>I(<math>\overline{EN}</math>)</sub> = 5.5 V	T <sub>J</sub> = 25°C		60	μA	
			-55°C ≤ T <sub>J</sub> ≤ 125°C		70		
Leakage current		OUT connected to ground, V <sub>I(<math>\overline{EN}</math>)</sub> = 5.5 V or V <sub>I(<math>\overline{EN}</math>)</sub> = 0 V	-55°C ≤ T <sub>J</sub> ≤ 125°C	1 TYP		μA	
Reverse leakage current		V <sub>I(OUT)</sub> = 5.5 V, IN = ground	T <sub>J</sub> = 25°C	0 TYP		μA	
<b>Under voltage lockout</b>							
Low level input voltage, IN				2	2.5	V	
Hysteresis, IN			T <sub>J</sub> = 25°C	75 TYP		mV	
<b>Overcurrent (<math>\overline{OC}</math>)</b>							
Output low voltage, V <sub>OL(OC)</sub>		I <sub>o(OC)</sub> = 5 mA			0.4	V	
Off state current 4/		V <sub>O(OC)</sub> = 5 V or 3.3 V			1	μA	
$\overline{OC}$ deglitch 4/		$\overline{OC}$ assertion or deassertion		4	15	ms	

See footnotes at end of table.

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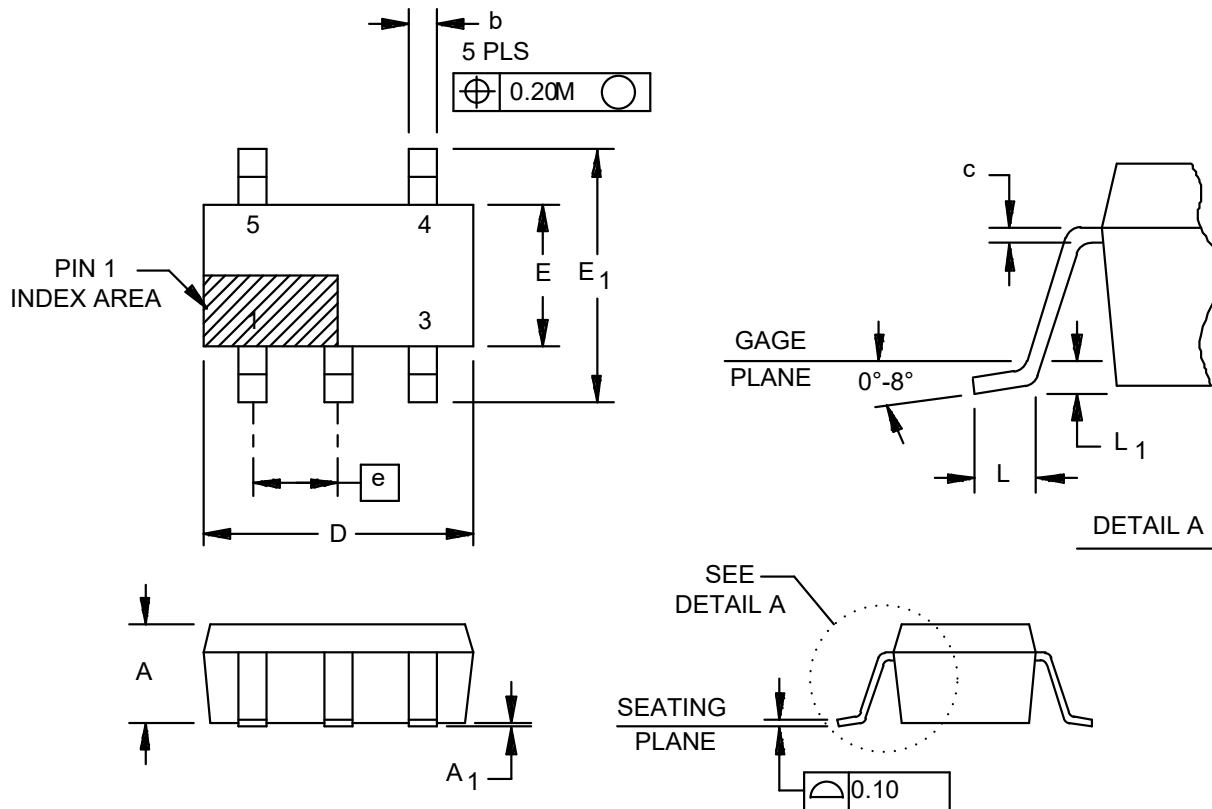
TABLE I. Electrical performance characteristics - Continuous. 1/

Test	Symbol	Conditions <u>2/ 3/</u>	T <sub>J</sub>	Limits		Unit
				Min	Max	
<b>Thermal shutdown</b> <u>5/</u>						
Thermal shutdown threshold <u>4/</u>				135		°C
Recovery from thermal shutdown <u>4/</u>				125		°C
Hysteresis <u>4/</u>				10 TYP		°C

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over recommended operating junction temperature range,  $V_{I(IN)} = 5.5 \text{ V}$ ,  $I_O = 0.5 \text{ A}$ ,  $V_{I(EN)} = 0 \text{ V}$  (unless otherwise noted).
- 3/ Pulse testing techniques maintain junction temperature close to ambient temperature; thermal effects must be accounted for separately.
- 4/ Specified by design.
- 5/ The thermal shutdown only reacts under overcurrent conditions.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.45	E	1.45	1.75
A1	0.00	0.15	E1	2.60	3.00
b	0.30	0.50	e	0.95 BSC	
c	0.08	0.22	L	0.30	0.50
D	2.75	3.05	L1	0.25 TYP	

**NOTES:**

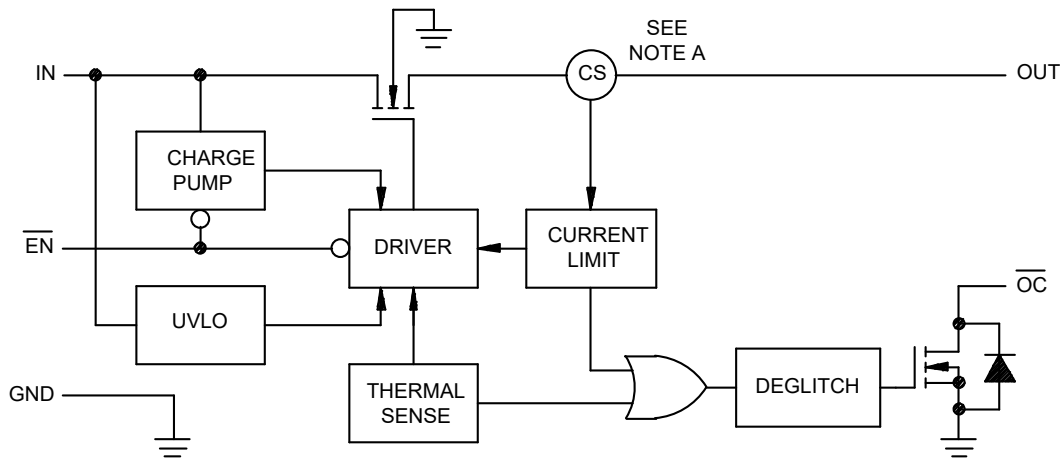
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-178 Variation AA.

FIGURE 1. Case outline.

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Terminal number	Terminal symbol	I/O	Terminal Functions
1	OUT	O	Power switch output
2	GND		Ground
3	$\overline{OC}$	O	Overcurrent, Open drain output, active low
4	$\overline{EN}$	I	Enable input, logic low turns on power switch
5	IN	I	Input voltage

FIGURE 2. Terminal connections and terminal functions.



NOTICE:

A. CS = Current sense.

FIGURE 3. Functional block diagram.

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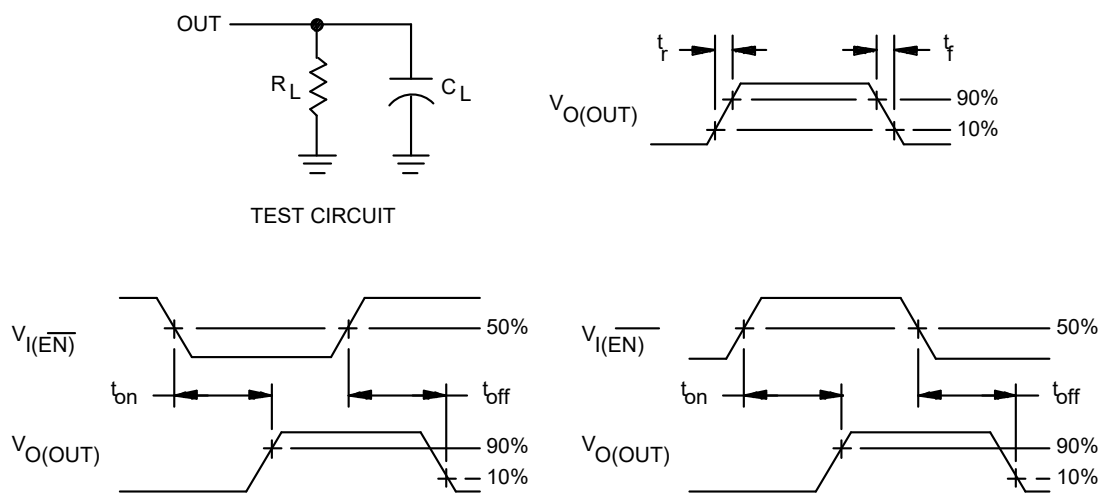


FIGURE 4. Test circuit and voltage waveforms.

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/11620</b></p>
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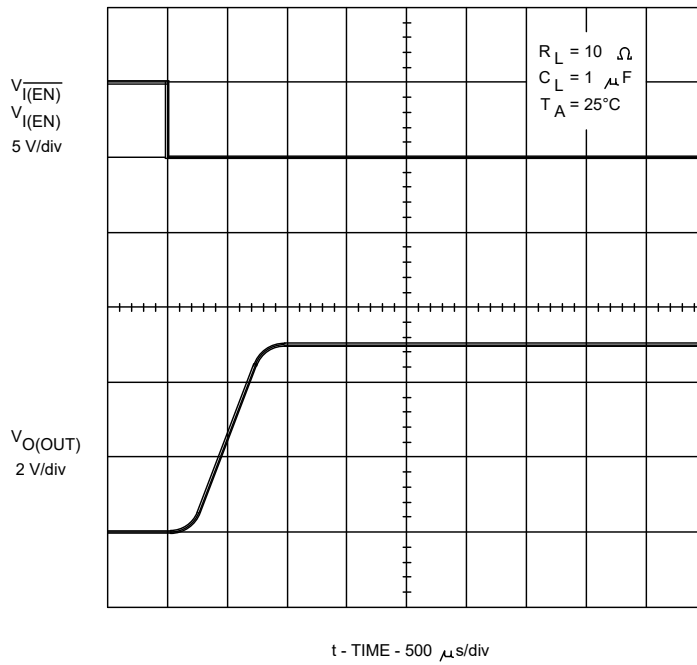


FIGURE 5. Turn-On delay and rise time with 1  $\mu F$  load.

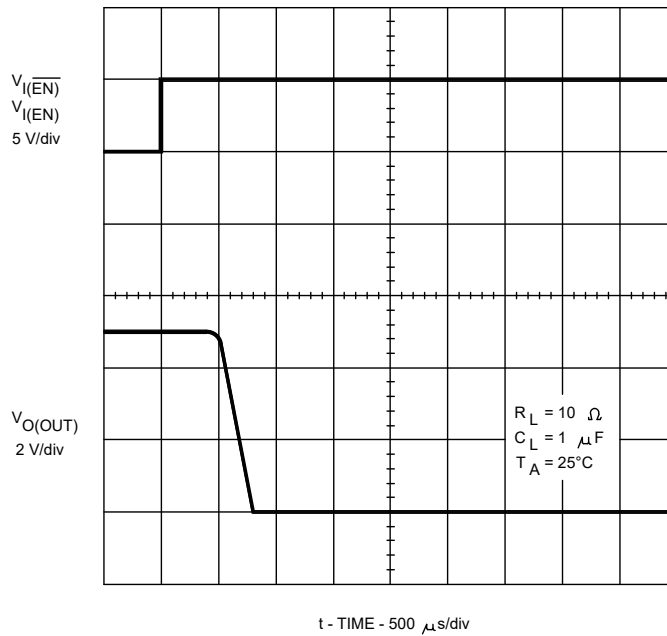


FIGURE 6. Turn-Off delay and fall time with 1  $\mu F$  load.

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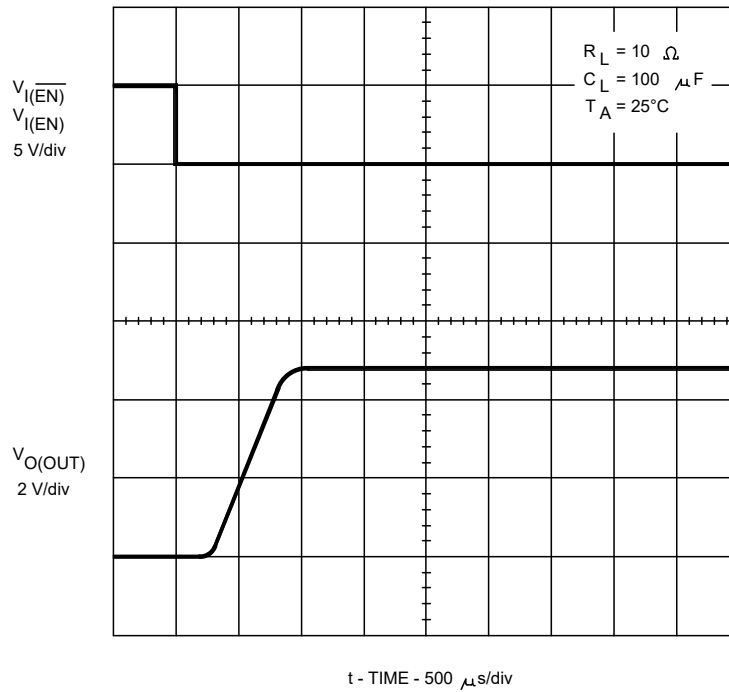


FIGURE 7. Turn-On delay and rise time with 100  $\mu F$  load.

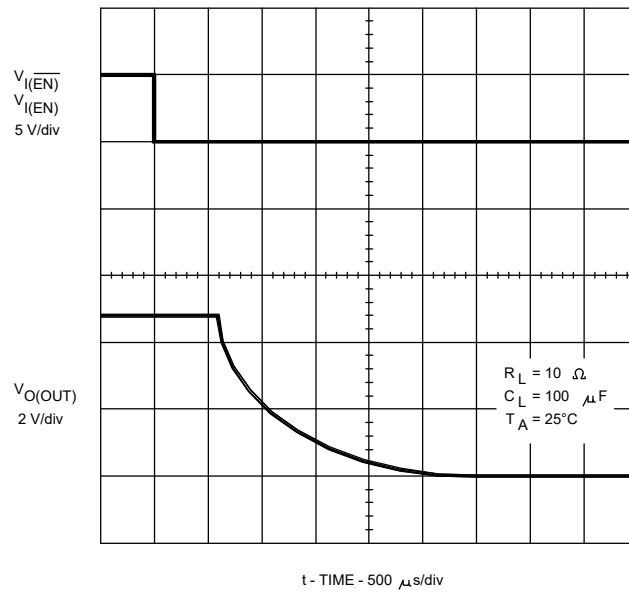


FIGURE 8. Turn-Off delay and fall time with 100  $\mu F$  load.

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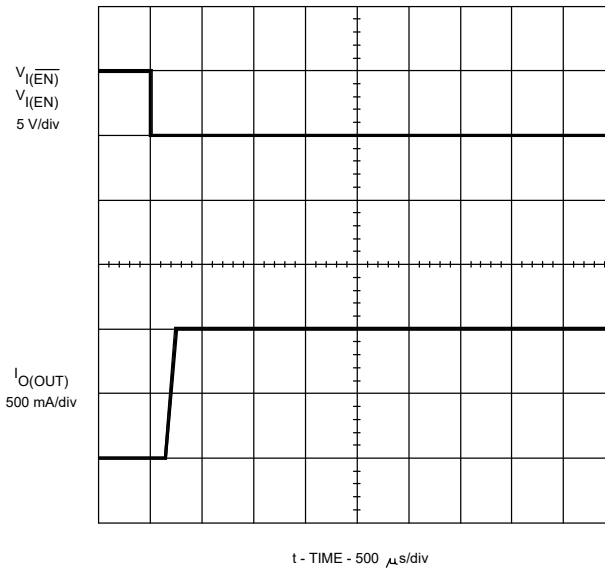


FIGURE 9. Short circuit current, device enabled into short.

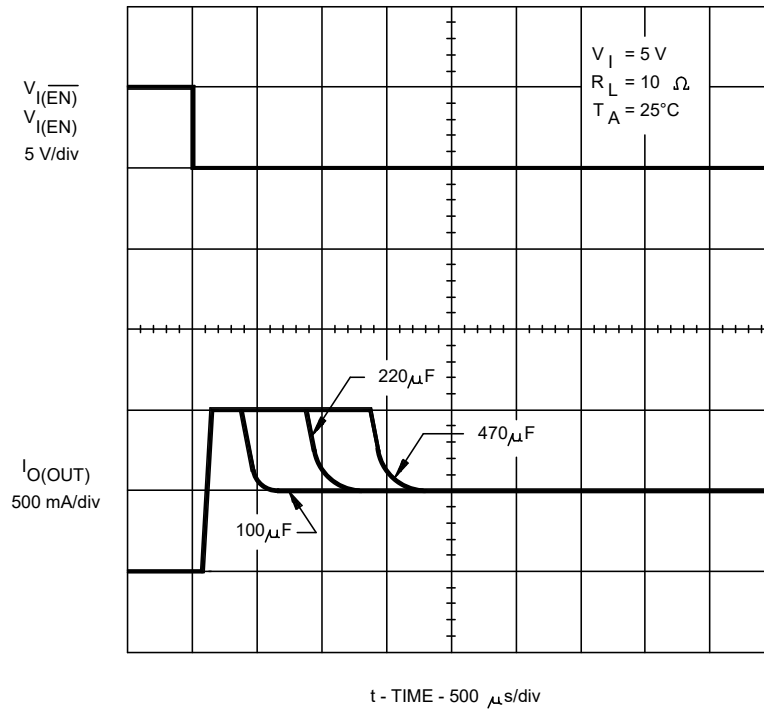


FIGURE 10. Inrush current with different load capacitance.

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/11620</b></p>
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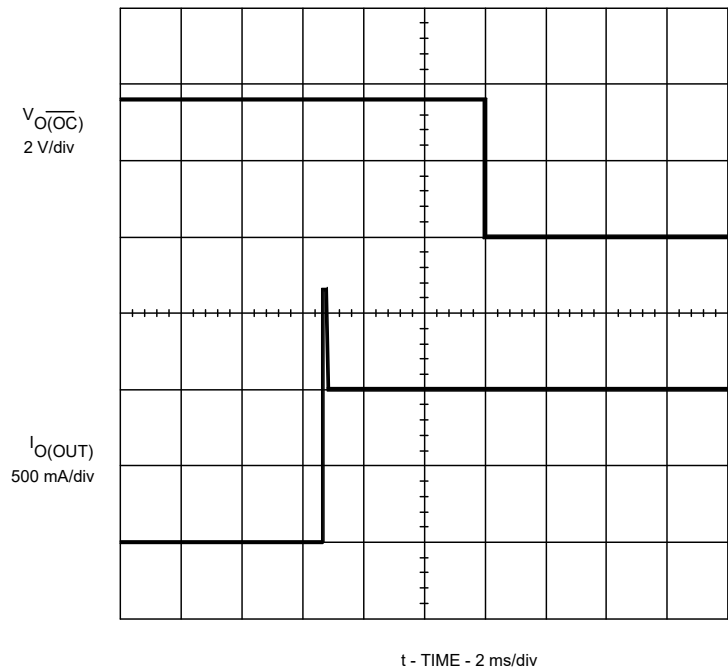


FIGURE 11. 3 Ω Load connected to enable device.

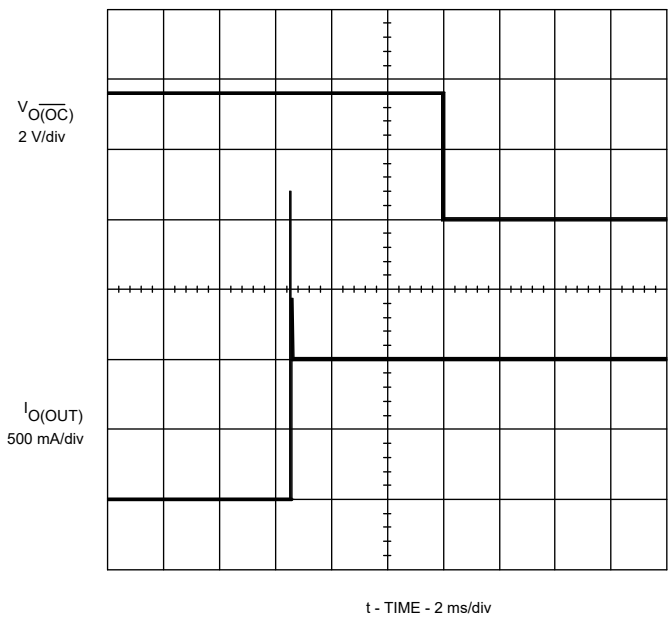


FIGURE 12. 2 Ω Load connected to enable device.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top Side Marking
V62/11620-01XE	01295	TPS2041BMDBVTEP	PXAM

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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