REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraph to current requirements. - ro	17-11-15	Charles F. Saffle

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A							
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dla.mil/landandmaritime**
Original date of drawing YY-MM-DD 11-12-01	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, LINEAR, NEGATIVE VOLTAGE REGULATOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/11619**
	REV **A**	**PAGE** 1 **OF** 12

AMSC N/A

5962-V048-17

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited*.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance negative voltage regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11619	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS7A3001-EP	Negative voltage regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187-AA-T	Plastic small outline with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage :
- IN pin to GND pin ..... -36 V to +0.3 V
- OUT pin to GND pin ..... -33 V to +0.3 V
- OUT pin to IN pin ..... -0.3 V to +36 V
- FB pin to GND pin ..... -2 V to +0.3 V
- FB pin to IN pin ..... -0.3 V to +36 V
- EN pin to IN pin ..... -0.3 V to +36 V
- EN pin to GND pin ..... -36 V to +36 V
- NR/SS pin to IN pin ..... -0.3 V to +36 V
- NR/SS pin to GND pin ..... -2 V to +0.3 V

Peak output current ..... Internally limited

Operating virtual junction temperature (T_J) ..... -55°C to +135°C

Storage temperature range (T_{STG}) ..... -65°C to +150°C

Electrostatic discharge (ESD) rating:
- Human body model (HBM) ..... 1500 V
- Charged device model (CDM) ..... 500 V

1.4 Recommended operating conditions. 2/

Operating junction temperature range (T_J) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	69.3	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	40.3	°C/W
Thermal resistance, junction-to-board	θ_{JB}	39.0	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	2.4	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	38.7	°C/W
Thermal resistance, junction-to-case (bottom)	$\theta_{JC(bottom)}$	17.8	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at https://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Input voltage range	V_{IN}		-55°C to +125°C	01	-36.0	-3.0	V
Internal reference	V_{REF}	VNR/SS = VREF	+25° C	01	-1.22	-1.142	V
					-1.184 typical		
Output voltage 4/ range	V_{OUT}	$\|V_{IN}\| \geq \| V_{OUT(NOM)} \| + 1.0$ V	-55°C to +125°C	01	-35.0	V_{REF}	V
Nominal accuracy	V_{OUT}	$\|V_{IN}\| = \| V_{OUT(NOM)} \| + 0.5$ V	+25° C	01	-1.5	+1.5	%V_{OUT}
Overall accuracy	V_{OUT}	$\| V_{OUT(NOM)} \| + 1.0$ V $\leq \|V_{IN}\| \leq 35$ V, 1 mA $\leq I_{OUT} \leq$ 200 mA	-55°C to +125°C	01	-2.85	+2.85	%V_{OUT}
Line regulation	V_{RLINE}	$\| V_{OUT(NOM)} \| + 1.0$ V $\leq \|V_{IN}\| \leq 35$ V,	+25° C	01	0.14 typical		%V_{OUT}
Load regulation	V_{RLOAD}	1 mA $\leq I_{OUT} \leq$ 200 mA	+25° C	01	0.04 typical		%V_{OUT}
Dropout voltage	$\|V_{DO}\|$	V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 100 mA	-55°C to +125°C	01	216 typical		mV
		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 200 mA				600	
					325 typical		
Current limit	I_{LIM}	V_{OUT} = 90% $V_{OUT(NOM)}$	-55°C to +125°C	01	220	500	mA
					330 typical		
Ground current	I_{GND}	I_{OUT} = 0 mA	-55°C to +125°C	01		100	µA
					55 typical		
		I_{OUT} = 100 mA			950 typical		
Shutdown supply current	$\|I_{SHDN}\|$	V_{EN} = +0.4 V	-55°C to +125°C	01		3.0	µA
					1.0 typical		
		V_{EN} = -0.4 V				3.0	
					1.0 typical		
Feedback 5/ current	I_{FB}		-55°C to +125°C	01		100	nA
					14 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Enable current	$\|I_{EN}\|$	$V_{EN} = \|V_{IN}\| = \| V_{OUT(NOM)} \| + 1.0$ V	-55°C to +125°C	01		1.0	µA
					0.48 typical		
		$V_{IN} = V_{EN} = -35$ V				1.0	
					0.51 typical		
		$V_{IN} = -35$ V, $V_{EN} = +15$ V				1.2	
					0.50 typical		
Positive enable high level voltage	V_{+EN_HI}		-55°C to +125°C	01	+2.0	+15	V
Positive enable low level voltage	V_{+EN_LO}		-55°C to +125°C	01	0	+0.4	V
Negative enable high level voltage	V_{-EN_HI}		-55°C to +125°C	01	V_{IN}	-2.0	V
Negative enable low level voltage	V_{-EN_LO}		-55°C to +125°C	01	-0.4	0	V
Output noise voltage	V_{NOISE}	$V_{IN} = -3$ V, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT} = 10$ µF, $C_{NR/SS} = 10$ nF, BW = 10 Hz to 100 kHz	-55°C to +125°C	01	15.1 typical		µVRMS
		$V_{IN} = -6.2$ V, $V_{OUT(NOM)} = -5$ V, $C_{OUT} = 10$ µF, $C_{NR/SS} = C_{BYP} = 10$ nF, 6/ BW = 10 Hz to 100 kHz			17.5 typical		
Power supply rejection ratio	PSRR	$V_{IN} = -6.2$ V, $V_{OUT(NOM)} = -5$ V, $C_{OUT} = 10$ µF, $C_{NR/SS} = C_{BYP} = 10$ nF, 6/ f = 120 Hz	-55°C to +125°C	01	72 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Thermal shutdown temperature	T_{SD}	Shutdown, temperature increasing	-55°C to +125°C	01	+170 typical		°C
		Reset, temperature decreasing			+150 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ At operating conditions, $V_{IN} \leq 0$ V, $V_{OUT(NOM)} \leq V_{REF} \leq 0$ V. At regulation, $V_{IN} \leq V_{OUT(NOM)} - |V_{DO}|$.
$I_{OUT} > 0$ flows from OUT to IN.

3/ Unless otherwise specified, at T_J = -55°C to +125°C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$ V or $|V_{IN}| = 3.0$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 μF, C_{OUT} = 2.2 μF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT.

4/ To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 μA is required.

5/ $I_{FB} > 0$ flows into the device.

6/ C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

Case X

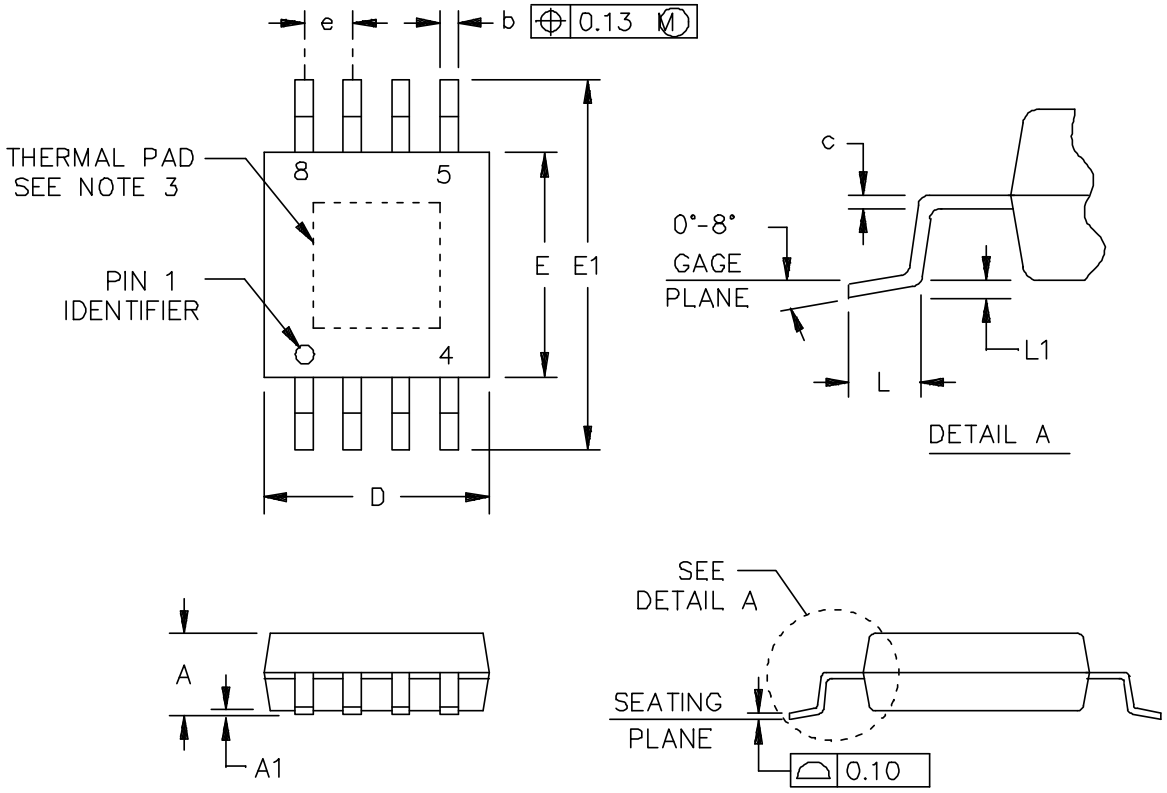

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/11619
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.043	---	1.10
A1	0.001	0.005	0.05	0.15
b	0.009	0.014	0.25	0.38
c	0.005	0.009	0.13	0.23
D	0.114	0.122	2.90	3.10
e	0.025 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
E1	0.187	0.198	4.75	5.05
L	0.015	0.027	0.40	0.70
L1	0.009 BSC		0.25 BSC	

NOTES:
1. Controlling dimensions are millimeters, inch dimensions are given for reference only.
2. Body dimensions do not include mold and flash or protrusion.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout.
4. See additional figure in the manufacturer's datasheet for details regarding the exposed thermal pad features and dimension.
5. Falls within reference to JEDEC MO-187-AA-T.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUT	Regulator output. A capacitor ≥ 2.2 μF must be tied from this pin to ground to assure stability.
2	FB	This pin is the input to the control loop error amplifier. It is used to set the output voltage of the device.
3	NC	Not internally connected. This pin must either be left open or tied to GND.
4	GND	Ground.
5	EN	This pin turns the regulator on or off. If $V_{EN} \geq V_{+EN\_HI}$ or $V_{EN} \leq V_{-EN\_HI}$, the regulator is enabled. If $V_{+EN\_LO} \geq V_{EN} \geq V_{-EN\_LO}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $\lvert V_{EN} \rvert \leq \lvert V_{IN} \rvert$.
6	NR/SS	Noise reduction pin. Connecting an external capacitor to this pin bypass noise generated by the internal bandgap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft start function.
7	DNC	Do not connect. Do not route this pin to any electrical net, not even ground or IN.
8	IN	Input supply.
Thermal pad		Must either be left open or tied to GND. Solder to printed circuit board (PCB) plane to enhanced thermal performance.

FIGURE 2. Terminal connections.

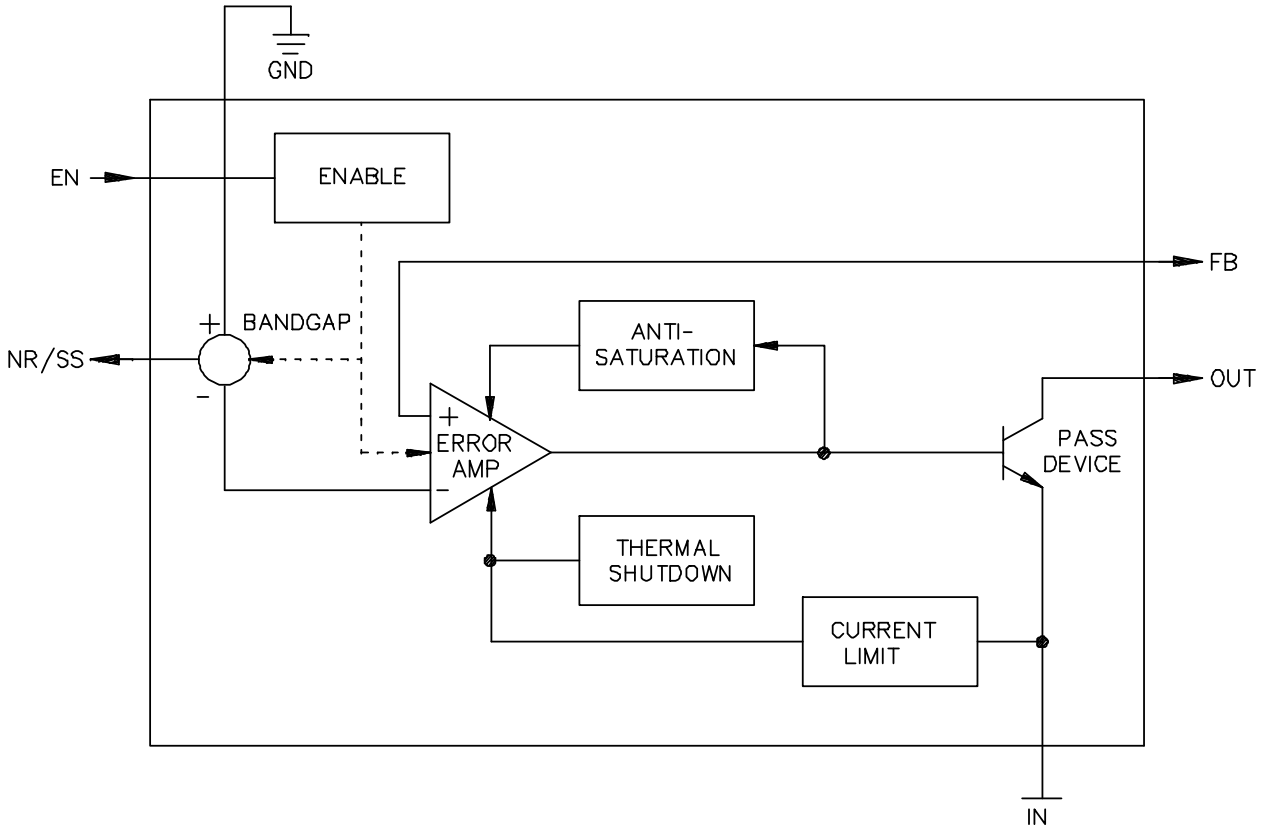

FIGURE 3. Logic diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/11619-01XE	01295	Tape and reel, 250 units	PXCM	TPS7A3001MDGNTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243