

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make change to the top side marking from DADI to TMP4 as specified under paragraph 6.3. Update document paragraphs to current requirements. - ro	17-08-02	C. SAFFLE
B	Make changes and additions to thermal data as specified in paragraph 1.3. Delete the min limits to all Temperature error section tests as specified in Table I. Under Figure 2 description column, delete Table III and replace with Table II. - ro	21-09-28	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="https://www.dla.mil/LandandMaritime">https://www.dla.mil/LandandMaritime</a>
Original date of drawing YY-MM-DD  11-10-04	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, TEMPERATURE SENSOR, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE <b>A</b>	CODE IDENT. NO. <b>16236</b>
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance temperature sensor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/11618</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TMP422	Dual channel temperature sensor

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	M0-178-BA	Plastic small outline surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (Vs) .....	+7 V
Input voltage (VIN):	
DX1, DX2, DX3, and DX4 pins .....	-0.5 V to Vs + 0.5 V
SDA and SCL pins .....	-0.5 to 7 V
Input current .....	10 mA
Power dissipation (PD) .....	230 mW
Junction temperature range (TJ) .....	+150°C
Storage temperature range (TSTG) .....	-65°C to +150°C
Electrostatic discharge (ESD) rating:	
Human body model (HBM) .....	3000 V
Charged device model (CDM) .....	1000 V
Machine Model (MM) .....	200 V
Thermal resistance, junction to case ( $\theta_{JC}$ ) .....	86°C/W typical
Thermal resistance, junction to ambient ( $\theta_{JA}$ ) .....	120.4°C/W typical
Thermal resistance, junction to bottom ( $\theta_{JB}$ ) .....	38.5°C/W typical
Characterization parameter, junction to top ( $\psi_{JT}$ ) .....	25.1°C/W typical
Characterization parameter, junction to board ( $\psi_{JB}$ ) .....	38.4°C/W typical

1.4 Recommended operating conditions. 2/

Supply voltage range (Vs) .....	2.7 V to 5.5 V
Operating free-air temperature range (TA) .....	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions Vs = 2.7 V to 5.5 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Temperature error							
Local temperature sensor	TELOCAL		-55°C to +125°C	01		±2.5	°C
Remote <sup>2/</sup> temperature sensor	TEREMOTE	TA = -55°C to +125°C, TD = -55°C to +125°C, VS = 3.3 V	-55°C to +125°C	01		±3	°C
		TA = -55°C to +125°C, TD = -55°C to +125°C				±5	
Remote temperature sensor versus supply (local/remote)		Vs = 2.7 V to 5.5 V	-55°C to +125°C	01		±0.72	°C/V
Temperature measurement							
Conversion time (per channel)			-55°C to +125°C	01	100	130	ms
Resolution, local temperature sensor (programmable)			-55°C to +125°C	01	12 typical		Bits
Resolution, remote temperature sensor			-55°C to +125°C	01	12 typical		Bits
Remote sensor source currents, high		Series resistance 3 kΩ maximum	-55°C to +125°C	01	120 typical		μA
Remote sensor source currents, medium high			-55°C to +125°C	01	60 typical		μA
Remote sensor source currents, medium low			-55°C to +125°C	01	12 typical		μA
Remote sensor source currents, low			-55°C to +125°C	01	6 typical		μA
Remote transistor ideality factor	η	Optimized ideality factor	-55°C to +125°C	01	1.008 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VS = 2.7 V to 5.5 V unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
System management bus (SMBus) interface							
Logic input high voltage (SCL, SDA)	VIH		-55°C to +125°C	01	2.1		V
Logic input low voltage (SCL, SDA)	VIL		-55°C to +125°C	01		0.8	V
Hysteresis			-55°C to +125°C	01	500 typical		mV
SMBus output low sink current			-55°C to +125°C	01	6		mA
SDA output low voltage	VOL	IOUT = 6 mA	-55°C to +125°C	01		0.4	V
Logic input current		0 ≤ VIN ≤ 6 V	-55°C to +125°C	01	-1	+1	µA
SMBus input capacitance (SCL, SDA)			-55°C to +125°C	01	3 typical		pF
SMBus clock frequency			-55°C to +125°C	01		3.4	MHz
SMBus timeout			-55°C to +125°C	01	25	35	ms
SCL falling edge to SDA valid time			-55°C to +125°C	01		1	µs
Digital inputs							
Input capacitance	CIN		-55°C to +125°C	01	3 typical		pF
Input logic levels, input high voltage	VIH		-55°C to +125°C	01	0.7 * (+VS)	(+VS) +0.5	V
Input logic levels, input low voltage	VIL		-55°C to +125°C	01	-0.5	0.3 * (+VS)	V
Leakage input current	IIN	0 ≤ VIN ≤ VS	-55°C to +125°C	01		1	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V <sub>S</sub> = 2.7 V to 5.5 V unless otherwise specified	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Power supply							
Specified voltage range	V <sub>S</sub>		-55°C to +125°C	01	2.7	5.5	V
Quiescent current	I <sub>Q</sub>	0.0625 conversions per second	-55°C to +125°C	01		38	μA
		Eight conversions per second				525	
		Serial bus inactive, shutdown mode				10	
		Serial bus active, f <sub>S</sub> = 400 kHz, shutdown mode			90 typical		
		Serial bus active, f <sub>S</sub> = 3.4 MHz, shutdown mode			350 typical		
Undervoltage lockout	UVLO		-55°C to +125°C	01	2.3	2.6	V
Power on reset threshold	POR		-55°C to +125°C	01		2.3	V

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Tested with less than 5 Ω effective series resistance and 100 pF differential input capacitance.

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Case X

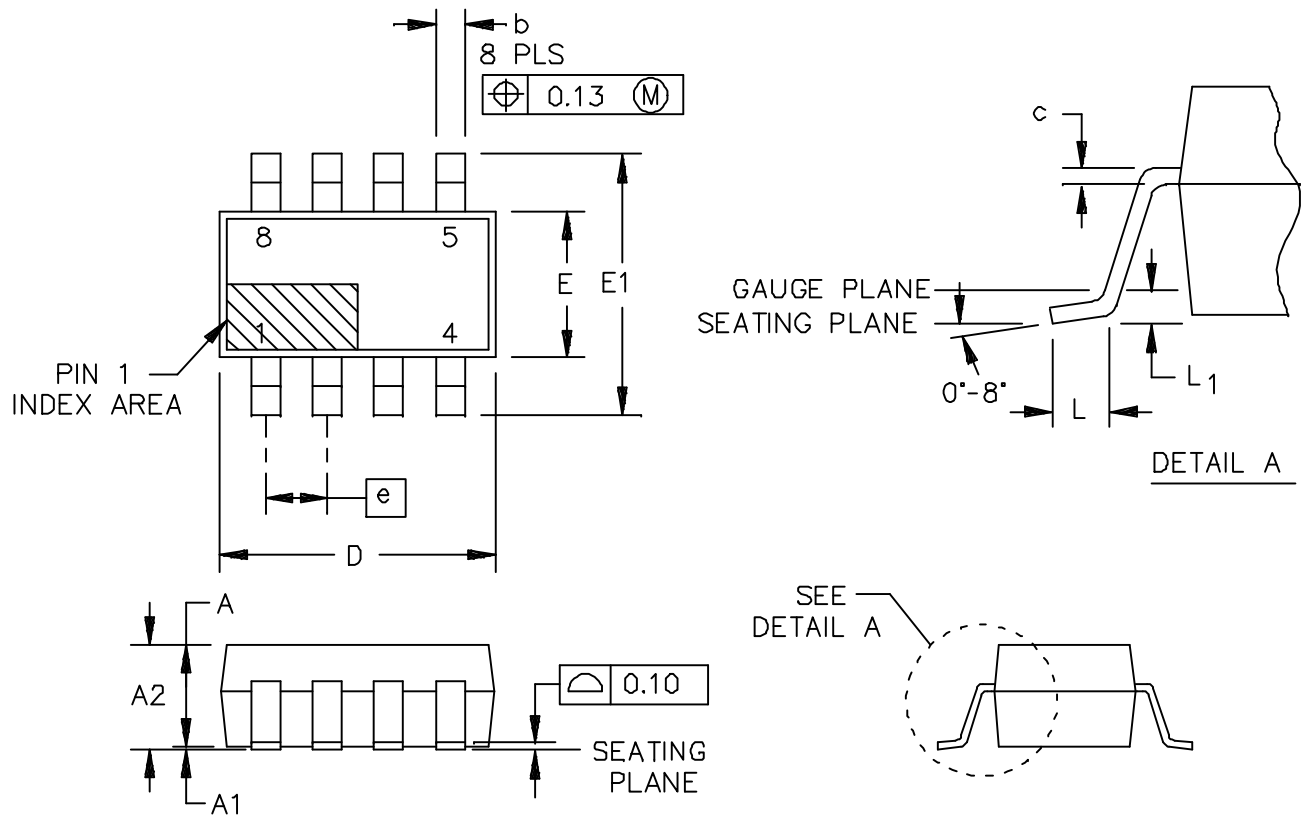


FIGURE 1. Case outline.

<p><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/11618</b></p>
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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.035	0.051	0.90	1.30
A1	0.00	0.005	0.00	0.15
A2	0.035	0.057	0.90	1.45
b	0.008	0.014	0.22	0.38
c	0.003	0.008	0.08	0.22
D	0.110	0.118	2.80	3.00
e	0.025 BSC		0.65 BSC	
E	0.057	0.068	1.45	1.75
E1	0.102	0.118	2.60	3.00
L	0.011	0.023	0.30	0.60
L1	0.009 BSC		0.25 BSC	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Package outline exclusive of metal burr and dambar protrusion/intrusion.
3. Package outline inclusive of soldering plating.
4. A visual index feature must be located within the pin 1 index area.
5. Body length does not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 mm ( 0.009 inch ) per side.
6. Falls within reference to JEDEC MO-178-BA.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	DX1	Channel 1 remote temperature sensor connection pin. Also sets the device address. See Table II.
2	DX2	Channel 1 remote temperature sensor connection pin. Also sets the device address. See Table II.
3	DX3	Channel 2 remote temperature sensor connection pin. Also sets the device address. See Table II.
4	DX4	Channel 2 remote temperature sensor connection pin. Also sets the device address. See Table II.
5	GND	Ground.
6	SDA	Serial data line for SMBus, open drain; requires pull up resistors +VS.
7	SCL	Serial clock line for SMBus, open drain; requires pull up resistor to +VS.
8	+VS	Positive supply voltage (2.7 V to 5.5 V).

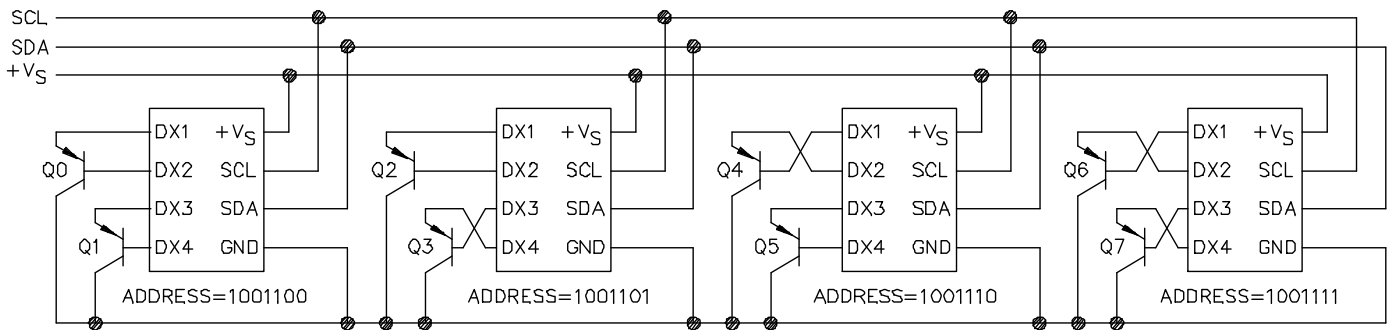
FIGURE 2. Terminal connections.

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TABLE II. Slave address options.

Two wire slave address	DX1	DX2	DX3	DX4
1001 100	DXP1	DXN1	DXP2	DXN2
1001 101	DXP1	DXN1	DXN2	DXP2
1001 110	DXN1	DXP1	DXP2	DXN2
1001 111	DXN1	DXP1	DXN2	DXP2

This device supports four slave addresses. The slave device address is set by the connections between the external transistors and the device according to figure 3 and Table II. If one of the channels is unused, the respective DXP (positive emitter base junction voltage) connection should be connected to GND, and the DXN (negative emitter base junction voltage) connection should be left unconnected. The polarity of the transistor for external channel 2 (DX3 and DX4 pins) sets the least significant bit of the slave address. The polarity of the transistor for external channel 1 (DX1 and DX2 pins) sets the next least significant bit of the slave address.



The device checks the polarity of the external transistor at power on, or after software reset, by forcing current to DX1 pin while connecting DX2 pin to approximately 0.6 V.

If the voltage on DX1 pin does not pull up to near the +Vs of the device, DX1 pin functions as DXP for channel 1, and the second LSB of the slave address is "0".

If the voltage on DX1 pin does pull up to near +Vs, the device forces current to DX2 while connecting DX1 pin to 0.6 V.

If the voltage on DX2 pin does not pull up to near +Vs, the device uses DX2 pin for DXP of channel 1, and sets the second LSB of the slave address to "1".

If both pins are shorted to GND or if both pins are open, the device uses DX1 pin as DXP and sets the address bit to "0". This process is then repeated for channel 2 (DX3 and DX4 pins).

If the device is to be used with transistors that are located on another integrated circuit (IC) (such as central processing unit (CPU), digital signal processor (DSP), or graphics processor), it is recommended to use DX1 pin or DX3 pin as DXP to ensure correct address detection.

If the other IC has a lower supply voltage or is not powered when the device tries to detect the slave address, a protection diode may turn on during the detection process and the device may incorrectly choose the DXP pin and corresponding slave address. Using DX1 pin and/or DX3 pin for transistors that are on other ICs ensures correct operation independent of supply sequencing or levels.

FIGURE 3. Connections for device address setup.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number <u>2/ 3/</u>
V62/11618-01XE	01295	TMP4	TMP422AMDCNTEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ For the most current package and ordering information, contact the manufacturer.
- 3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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