REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE	40	41	42	43	44	45	46															
REV																						
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY MM DD 12-03-22	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, FLOATNG POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/11617**
	REV	**PAGE** 1 **OF** 46

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance floating point digital signal processor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SM320C6727B-EP	Floating point digital signal processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	256	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range, CV_{DD}, $OSCV_{DD}$ ..... -0.3 V to 1.8 V 3/
Supply voltage range, DV_{DD}, PLLHV ..... -0.3 V to 4.0 V
Input voltage range:
All pins except OSCIN ..... -0.3 V to DV_{DD} + 0.5 V
OSCIN pin ..... -3.0 V to CV_{DD} + 0.5 V
Output voltage range:
All pins except OSCOUT ..... -0.3 V to DV_{DD} + 0.5 V
OSCOUT pin ..... -3.0 V to CV_{DD} + 0.5 V
Clamp current ..... ±20 mA
Operating case temperature range, (T_C) ..... -55°C to 125°C
Storage temperature range (Tstg) ..... -65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values are with referenced to VSS unless otherwise specified.
3/ If $OSCV_{DD}$ and $OSCV_{SS}$ pins are used as filter pins for reduced oscillator jitter, they should not be connected to CV_{DD} and V_{SS} externally.

1.3 Recommended operating conditions. 4/

Core supply voltage, (CV_{DD}) ..... 1.14 V to 1.32 V
I/O supply voltage, (DV_{DD}):..... 3.13 V to 3.47 V
Operating free air temperature, (T_C) ..... -55°C to 125°C
Allowed PLL operating conditions

	Parameter	Default Value	Allowed Setting or Range	
			Min	Max
1	PLLRST = 1 assertion time during initialization	N/A	125 ns	
2	Lock time before setting PLLEN = 1. After changing D0, PLLM, or input clock	N/A	187.5 µs	
3	PLL input frequency (PLLREF after D0) 5/		12 MHz	50 MHz
4	PLL multiplier values (PLLM)	x13	x4	x25
5	PLL output frequency (PLLOUT before dividers D1, D2, D3) 6/	N/A	140 MHz	600 MHz
6	SYSCLK1 frequency (set by PPLM and dividers D0, D1)	PLLOUT/1		divide frequency specification
7	SYSCLK2 frequency (set by PPLM and dividers D0, D2)	PLLOUT/2	/2, /3, or /4 of SYSCLK1	
8	SYSCLK3 frequency (set by PPLM and dividers D0, D3)	PLLOUT/3		EMIF frequency specification

Thermal characteristics for case X

No.		Symbol	°C/W	Air Flow (m/s)
Two Signal, Two Plane, 101.5 x 114.5 x 1.6 mm, 2 oz Cu. 7/				
1	Thermal resistance junction to ambient	$R\theta_{JA}$	25	0
2	Thermal resistance junction to board	$R\theta_{JB}$	14.5	0
3	Thermal resistance junction to top of case	$R\theta_{JC}$	10	0
4	Thermal metric junction to board	ψ_{JB}	14	0
5	Thermal metric junction to top of case	ψ_{JT}	0.39	0

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ Some values for the D0 divider produce results outside of this range and should not be selected.
6/ In general, selecting the PLL output clock rate closest to the maximum frequency will decrease clock jitter.
7/ EIA/JESD51-9 PCB

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD51-9 – Test Board for Area Array Surface Mount Packages.

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Test and timing diagram. The test and timing diagram shall be as shown in figures 4 to 37.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
High level output voltage	V_{OH}	I_O = -100 µA	DV_{DD} – 0.2		V
Low level output voltage	V_{OL}	I_O = -100 µA		0.2	V
High level output current	I_{OH}	V_O = 0.8 DV_{DD}		-8	mA
Low level output current	I_{OL}	V_O = 0.22 DV_{DD}		8	mA
High level input current	V_{IH}		2	DV_{DD}	V
Low level input current	V_{IL}		0	0.8	V
Input hysteresis	V_{HYS}		0.13 $DV_{DD\ TYP}$		V
Input current and off state output current	I_I, I_{OZ}	Pins without pullup or pulldown		±10	µA
		Pins with internal pullup	-50	-170	
		Pins with internal pulldown	50	170	
Input transition time	t_{tr}			25	ns
Input capacitance	C_I			7	pF
Output capacitance	C_O			7	pF
CV_{DD} Supply 3/	I_{DD2V}	Capacitance = 7 pF, CV_{DD} = 1.2 V 658 CPU clock = 250 MHz	555 TYP		mA
DV_{DD} Supply 3/	I_{DD3V}	DVDD = 3.3 V, 32 bit EMIF speed = 100 MHz	58 TYP		mA

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
	EMIF ELECTRICAL DATA/TIMING (See Figure 7 – 13)					
EMIF SDRAM interface timing requirements						
19	Input setup time, read data valid on D[31:0] before EM_CLK rising	$t_{su(EM_DV-EM_CLKH)}$		3		ns
20	Input hold time, read data valid on D[31:0] after EM_CLK rising	$t_{h(EM_CLKHJ-EM_DIV)}$		1.9		
EMIF SDRAM interface switching characteristics						
1	Cycle time, EMIF clock EM_CLK	$t_{c(EM_CLK)}$		10		ns
2	Pulse width, EMIF clock EM_CLK high or low	$t_{w(EM_CLK)}$		3		
3	Delay time, EM_CLK rising to $\overline{EM_CS[0]}$ valid	$t_{d(EM_CLKH-EM_CSV)S}$			7.7	
4	Output hold time, EM_CLK rising to $\overline{EM_CS[0]}$ invalid	$t_{oh(EMCLKH-EM_CSIV)S}$		1.15		
5	Delay time, EM_CLK rising to EM_$\overline{WE}$_DQM[3:0] valid	$t_{d(EM_CLKH-EM_WE-DQMV)S}$			7.7	
6	Output hold time, EM_CLK rising to EM_$\overline{WE}$_DQM[3:0] invalid	$t_{oh(EM_CLKH-EM_WE-DQMiV)S}$		1.15		
7	Delay time, EM_CLK rising to EM_A[12:0] and EM_BA[1:0] valid	$t_{d(EM_CLKH-EM_AV)S}$			7.7	
8	Output hold time, EM_CLK rising to EM_A[12:0] and EM_BA[1:0] invalid	$t_{oh(EMCLKH-EM_AIV)S}$		1.15		
9	Delay time, EM_CLK rising to EM_D[31:0] valid	$t_{d(EM_CLKH-EM_DV)S}$			7.7	
10	Output hold time, EM_CLK rising to EM_D[31:0] invalid	$t_{oh(EMCLKH-EM_DIV)S}$		1.15		
11	Delay time, EM_CLK rising to $\overline{EM_RAS}$ valid	$t_{d(EM_CLKH-EM_RASV)S}$			7.7	
12	Output hold time, EM_CLK rising to $\overline{EM_RAS}$ invalid	$t_{oh(EMCLKH-EM_RASIV)S}$		1.15		
13	Delay time, EM_CLK rising to $\overline{EM_CAS}$ valid	$t_{d(EM_CLKH-EM_CASV)S}$			7.7	
14	Output hold time, EM_CLK rising to $\overline{EM_CAS}$ invalid	$t_{oh(EMCLKH-EM_CASIV)S}$		1.15		
15	Delay time, EM_CLK rising to $\overline{EM_WE}$ valid	$t_{d(EM_CLKH-EM_WEV)S}$			7.7	
16	Output hold time, EM_CLK rising to $\overline{EM_WE}$ invalid	$t_{oh(EMCLKH-EM_WEIV)S}$		1.15		
17	Delay time, EM_CLK rising to EM_D[31:0] 3-stated	$t_{d(EM_CLKH-EM_DHZ)S}$			7.7	
18	Output hold time, EM_CLK rising to EM_D[31:0] driving	$t_{oh(EMCLKH-EM_DLZ)S}$		1.15		
EMIF asynchronous interface timing requirements 4/ 5/						
28	Input setup time, read data valid on EM_D[31:0] before EM_CLK rising	$t_{su(EM_DV-EM_CLKH)A}$		5		ns
29	Input hold time, read data valid on EM_D[31:0] after EM_CLK rising	$t_{h(EM_CLK-EM_DIV)A}$		2		
30	Setup time, EM_WAIT valid before EM_CLK rising edge	$t_{su(EM_CLK-EM_WAITV)A}$		5		
31	Hold time, EM_WAIT valid after EM_CLK rising edge	$t_{h(EM_CLK-EM_WAITIV)A}$		0		
33	Pulse width of EM_WAIT assertion and deassertion	$t_{w(EM_WAIT)A}$		2E+5		
34	Delay from EM_WAIT sampled deasserted on EM_CLK rising to beginning of HOLD phase	$t_{d(EM_WAITD-HOLD)A}$			4E 6/	
35	Setup before end of STROBE phase (if no extended wait state are inserted) by which EM_WAIT must be sampled asserted on EM_CLK rising in order to add extended wait states. 7/	$t_{su(EM_WAITA-HOLD)A}$		4E 6/		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
	EMIF ELECTRICAL DATA/TIMING – Continued. (See Figure 7 – 13)					
	EMIF asynchronous interface switching characteristics 5/					
1	Cycle time, EMIF clock EM_CLK	$t_{c(EM_CLK)}$		10		ns
2	Pulse width, high or low, EMIF clock EM_CLK	$t_{w(EM_CLK)}$		3		
17	Delay time, EM_CLK rising to EM_D[31:0] 3-stated	$t_{dis(EM_CLKH\text{-}EM_DHZ)S}$			7.7	
18	Output hold time, EM_CLK rising to EM_D[31:0] driving	$t_{ena(EM_CLKH\text{-}EM_DLZ)S}$		1.15		
21	Delay time, from EM_CLK rising edge to $\overline{EM_CS[2]}$	$t_{d(EM_CLK\text{-}EM_CS2V)A}$		0	8	
22	Delay time, EM_CLK rising to EM_$\overline{WE}$_DQM[3:0] valid	$t_{d(EM_CLK\text{-}EM_WE_DQMV)A}$		0	8	
23	Delay time, EM_CLK rising to EM_A[12:0] and EM_BA[1:0] valid	$t_{d(EM_CLK\text{-}EM_AV)A}$		0	8	
24	Delay time, EM_CLK rising to EM_D[31:0] valid	$t_{d(EM_CLK\text{-}EM_DV)A}$		0	8	
25	Delay time, EM_CLK rising to $\overline{EM_OE}$ valid	$t_{d(EM_CLK\text{-}EM_OEV)A}$		0	8	
26	Delay time, EM_CLK rising to EM_R$\overline{W}$ valid	$t_{d(EM_CLK\text{-}EM_RW)A}$		0	8	
27	Delay time, EM_CLK rising to EM_D[31:0] 3-stated	$t_{d(EM_CLK\text{-}EM_DDIS)A}$		0	8	
32	Delay time, EM_CLK rising to $\overline{EM_WE}$ valid	$t_{d(EM_CLK\text{-}EM_WE)A}$		0	8	
	UHPI ELECTRICAL DATA/TIMING (See Figure 14 – 21)					
	UHPI read and write timing requirements 8/ 9/					
9	Setup time, $\overline{UHPI_HAS}$ low before DS falling edge	$t_{su(HASL_DSL)}$		5		ns
10	Hold time, $\overline{UHPI_HAS}$ low after DS falling edge	$t_{h(DSL_HASL)}$		2		
11	Setup time, HAD valid before $\overline{UHPI_HAS}$ falling edge	$t_{su(HAD_HASL)}$		5		
12	Hold time, HAD valid after $\overline{UHPI_HAS}$ falling edge	$t_{h(HASL_HAD)}$		5		
13	Pulse duration, DS low	$t_{w(DSL)}$		15		
14	Pulse duration, DS high	$t_{w(DSH)}$		2P		
15	Setup time, HAD valid before DS falling edge	$t_{su(HAD\text{-}DSL)}$		5		
16	Hold time, HAD valid after DS falling edge	$t_{h(DSL\text{-}HAD)}$		5		
17	Setup time, HD valid before DS rising edge	$t_{su(HD\text{-}DSH)}$		5		
18	Hold time, HD valid after DS rising edge	$t_{h(DSH\text{-}HD)}$		0		
37	Setup time, $\overline{UHPI_HCS}$ low before DS falling edge	$t_{su(HCSL\text{-}DSL)}$		0		
38	Hold time, DS low after $\overline{UHPI_HCS}$ rising edge	$t_{h(HRDYH\text{-}DSL)}$		1		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
UHPI ELECTRICAL DATA/TIMING – Continued. (See Figure 14 – 21)						
UHPI read and write switching characteristics 9/ 10/						
1	Delay time, DS low to HD valid	$t_{d(DSL-HDV)}$	Case 1. HPIC or HPIA read	1	15	ns
			Case 2. HPID read with no auto increment		9*2H+20 11/	
			Case 3. HPID read with auto increment and read FIFO initially empty		9*2H+20 11/	
			Case 4. HPID read with auto increment and data previously prefetched into the read FIFO	1	15	
2	Disable time, HD high impedance from DS high	$t_{dis(DSH-HDV)}$		1	4	
3	Enable time, HD driven from DS low	$t_{en(DSL-HDD)}$		3	15	
4	Delay time, DS low to $\overline{\text{UHPI_HRDY}}$ high	$t_{d(DSL-HRDYH)}$			12	
5	Delay time, DS high to $\overline{\text{UHPI_HRDY}}$ high	$t_{d(DSH-HRDYH)}$			12	
6	Delay time, DS low to $\overline{\text{UHPI_HRDY}}$ low	$t_{d(DSL-HRDYL)}$	Case 1. HPID read with no auto increment		10*2H+20 11/	
			Case 2. HPID read with auto increment and read FIFO initially empty		10*2H+20 11/	
7	Delay time, HD valid to $\overline{\text{UHPI_HRDY}}$ low	$t_{d(HDV-HRDYL)}$		0		
34	Delay time, DS high to $\overline{\text{UHPI_HRDY}}$ low	$t_{d(DSH-HRDYL)}$	Case 1. HPIA write		5*2H+20 11/	
			Case 2. HPID read with auto increment and read FIFO initially empty		5*2H+20 11/	
35	Delay time, DS low to $\overline{\text{UHPI_HRDY}}$ low for HPIA write and FIFO not empty	$t_{d(DSL-HRDYL)}$			40*2H+20 11/	
36	Delay time, $\overline{\text{UHPI_HAS}}$ low to $\overline{\text{UHPI_HRDY}}$ high	$t_{d(HASL-HRDYH)}$			12	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits		Unit
				Min	Max	
	McASP ELECTRICAL DATA/TIMING (See figure 22 – 24)					
McASP timing requirements 12/ 8/						
1	Cycle time, AHCLKR external, AHCLKR input	$t_{c(AHCKRX)}$		20		ns
	Cycle time, AHCLKX external, AHCLKX input			20		
2	Pulse duration, AHCLKR external, AHCLKR input	$t_{w(AHCKRX)}$		7.5		
	Pulse duration, AHCLKX external, AHCLKX input			7.5		
3	Cycle time, ACLKR external, ACLKR input	$t_{c(ACKRX)}$		greater of 2P or 20		
	Cycle time, ACLKX external, ACLKX input			greater of 2P or 20		
4	Pulse duration, ACLKR external, ACLKR input	$t_{w(ACKRX)}$		10		
	Pulse duration, ACLKX external, ACLKX input			10		
5	Setup time, AFSR input to ACLKR internal	$t_{su(AFRXC-ACKRX)}$		8		
	Setup time, AFSX input to ACLKX internal			8		
	Setup time, AFSR input to ACLKR external input			3		
	Setup time, AFSX input to ACLKX external input			3		
	Setup time, AFSR input to ACLKR external output			3		
	Setup time, AFSX input to ACLKX external output			3		
6	Hold time, AFSR input after ACLKR internal	$t_{h(ACKRX-AFRX)}$		0		
	Hold time, AFSX input after ACLKX internal			0		
	Hold time, AFSR input after ACLKR external input			3		
	Hold time, AFSX input after ACLKX external input			3		
	Hold time, AFSR input after ACLKR external output			3		
	Hold time, AFSX input after ACLKX external output			3		
7	Setup time, AXRn input to ACLKR	$t_{su(AXR-ACKRX)}$		8		
	Setup time, AXRn input to ACLKR			3		
	Setup time, AXRn input to ACLKR			3		
8	Hold time, AXRn input after ACLKR	$t_{h(ACKRX-AXR)}$		3		
	Hold time, AXRn input after ACLKR			3		
	Hold time, AXRn input after ACLKR			3		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
	McASP ELECTRICAL DATA/TIMING – Continued (See figure 22 – 24)					
	McASP switching characteristics 12/					
9	Cycle time, AHCLKR internal, AHCLKR output	$t_{c(AHCKRX)}$		20		ns
	Cycle time, AHCLKR external, AHCLKR output			20		
	Cycle time, AHCLKX internal, AHCLKX output			20		
	Cycle time, AHCLKX external, AHCLKX output			20		
10	Pulse duration, AHCLKR internal, AHCLKR output	$t_{w(AHCKRX)}$		(AHR/2)-2.5 13/		
	Pulse duration, AHCLKR external, AHCLKR output			(AHR/2)-2.5 13/		
	Pulse duration, AHCLKX internal, AHCLKX output			(AHX/2)-2.5 14/		
	Pulse duration, AHCLKX external, AHCLKX output			(AHX/2)-2.5 14/		
11	Cycle time, ACLKR internal, ACLKR output	$t_{c(ACKRX)}$		greater of 2P or 20 ns 8/		
	Cycle time, ACLKR external, ACLKR output			greater of 2P or 20 ns 8/		
	Cycle time, ACLKX internal, ACLKX output			greater of 2P or 20 ns 8/		
	Cycle time, ACLKX external, ACLKX output			greater of 2P or 20 ns 8/		
12	Pulse duration, ACLKR internal, ACLKR output	$t_{w(ACKRX)}$		(AR/2) – 2.5 15/		
	Pulse duration, ACLKR external, ACLKR output			(AR/2) – 2.5 15/		
	Pulse duration, ACLKX internal, ACLKX output			(AX/2) – 2.5 16/		
	Pulse duration, ACLKX external, ACLKX output			(AX/2) – 2.5 16/		
13	Delay time, ACLKR internal, AFSR output	$t_{d(ACKRX-FRX)}$			5	
	Delay time, ACLKX internal, AFSX output				5	
	Delay time, ACLKR external input, AFSR output				10	
	Delay time, ACLKX external input, AFSX output				10	
	Delay time, ACLKR external output, AFSR output				10	
	Delay time, ACLKX external output, AFSX output				10	
	Delay time, ACLKR internal, AFSR output			-2		
	Delay time, ACLKX internal, AFSX output			-2		
	Delay time, ACLKR external input, AFSR output			0		
	Delay time, ACLKX external input, AFSX output			0		
	Delay time, ACLKR external output, AFSR output			0		
	Delay time, ACLKX external output, AFSX output			0		
14	Delay time, ACLKX internal, AXRn output	$t_{d(ACLKX-AXRV)}$		-1	5	
	Delay time, ACLKX external input, AXRn output			0	10	
	Delay time, ACLKX external output, AXRn output			0	10	
15	Delay time, ACLKX internal, AXRn output	$t_{dis(ACKX-AXRHZ)}$		-3	10	
	Delay time, ACLKX external input, AXRn output			-3	10	
	Delay time, ACLKX external output, AXRn output			-3	10	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
SPI ELECTRICAL DATA/TIMING (See figure 25 – 30)						
General timing requirements for SPIx Master Modes 8/						
1	Cycle time, SPIx_CLK, All master modes	$t_{c(SPC)M}$		greater of 8P or 100 ns	256P	ns
2	Pulse width high, SPIx_CLK, All master modes	$t_{w(SPCH)M}$		greater of 4P or 45 ns		
3	Pulse width low, SPIx_CLK, All master modes	$t_{w(SPCL)M}$		greater of 4P or 45 ns		
4	Dealy, initial data bit valid on SPIx_SIMO to initial edge on SPIx_CLK 17/	$t_{d(SIMO-SPC)M}$	Polarity = 0, Phase = 0, to SPIx_CLK rising	4P		
			Polarity = 0, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + 4P		
			Polarity = 1, Phase = 0, to SPIx_CLK falliing	4P		
			Polarity = 1, Phase = 1, to SPIx_CLK falliing	$0.5t_{c(SPC)M}$ + 4P		
5	Dealy, subsequent bits valid on SPIx_SIMO after transmit edge of SPIx_CLK	$t_{d(SPC-SIMO)M}$	Polarity = 0, Phase = 0, from SPIx_CLK rising		15	
			Polarity = 0, Phase = 1, from SPIx_CLK falling		15	
			Polarity = 1, Phase = 0, from SPIx_CLK falling		15	
			Polarity = 1, Phase = 1, from SPIx_CLK rising		15	
6	Output hold time, SPIx_SIMO valid after receive edge of SPIxCLK, except for final bit 18/	$t_{oh(SPC_SIMO)M}$	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)M}$ - 10		
			Polarity = 0, Phase = 1, from SPIx_CLK rising	$0.5t_{c(SPC)M}$ - 10		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)M}$ - 10		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	$0.5t_{c(SPC)M}$ - 10		
7	Input setup time, SPIx_SOMI valid before edge of SPIx_CLK	$t_{su(SOMI_SPC)M}$	Polarity = 0, Phase = 0, to SPIx_CLK falling	0.5P + 15		
			Polarity = 0, Phase = 1, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	0.5P + 15		
8	Input hold time, SPIx_SOMI valid after receive edge of SPIx_CLK	$t_{ih(SPC_SOMI)M}$	Polarity = 0, Phase = 0, from SPIx_CLK falling	0.5P + 5		
			Polarity = 0, Phase = 1, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	0.5P + 5		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
SPI ELECTRICAL DATA/TIMING – Continued (See figure 25 – 30)						
General timing requirements for SPIx Slave Modes 8/						
9	Cycle time, SPIx_CLK, All slave modes	$t_{c(SPC)M}$		greater of 8P or 100 ns	256P	ns
10	Pulse width high, SPIx_CLK, All slave modes	$t_{w(SPCH)M}$		greater of 4P or 45 ns		
11	Pulse width low, SPIx_CLK, All slave modes	$t_{w(SPCL)M}$		greater of 4P or 45 ns		
12	Setup time, transmit data writtern to SPI and output onto SPIx_SOMI pin before initial clock edge from master 19/ 20/	$t_{su(SOMI-SPC)S}$	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P		
			Polarity = 0, Phase = 1, to SPIx_CLK rising	2P		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	2P		
13	Dealy, subsequent bits valid on SPIx_SOMI after transmit edge of SPIx_CLK	$t_{d(SPC-SIMO)S}$	Polarity = 0, Phase = 0, from SPIx_CLK rising		2P+15	
			Polarity = 0, Phase = 1, from SPIx_CLK falling		2P+15	
			Polarity = 1, Phase = 0, from SPIx_CLK falling		2P+15	
			Polarity = 1, Phase = 1, from SPIx_CLK rising		2P+15	
14	Output hold time, SPIx_SOMI valid after receive edge of SPIxCLK, except for final bit 21/	$t_{oh(SPC_SIMO)S}$	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)S}$ - 10		
			Polarity = 0, Phase = 1, from SPIx_CLK rising	$0.5t_{c(SPC)S}$ - 10		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)S}$ - 10		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	$0.5t_{c(SPC)S}$ - 10		
15	Input setup time, SPIx_SIMO valid before receive edge of SPIx_CLK	$t_{su(SIMO_SPC)S}$	Polarity = 0, Phase = 0, to SPIx_CLK falling	0.5P + 15		
			Polarity = 0, Phase = 1, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	0.5P + 15		
16	Input hold time, SPIx_SIMO valid after receive edge of SPIx_CLK	$t_{ih(SPC_SIMO)S}$	Polarity = 0, Phase = 0, from SPIx_CLK falling	0.5P + 5		
			Polarity = 0, Phase = 1, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	0.5P + 5		
Additional 22/ SPI master timings, 4-Pin Enable option 8/ 23/						
19	Delay from slave assertion of $\overline{SPIx_ENA}$ active to first SPIx_CLK from master 24/	$t_{d(ENA_SPC)M}$	Polarity = 0, Phase = 0, to SPIx_CLK rising		3P + 15	ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising		$0.5t_{c(SPC)M}$ + 3P + 15	
			Polarity = 1, Phase = 0, to SPIx_CLK falling		3P + 15	
			Polarity = 1, Phase = 1, to SPIx_CLK falling		$0.5t_{c(SPC)M}$ + 3P + 15	
18	Max delay for slave deassert $\overline{SPIx_ENA}$ after final SPIx_CLK edge to ensure master does not begin the next transfer 25/		Polarity = 0, Phase = 0, to SPIx_CLK falling		$0.5t_{c(SPC)M}$	
			Polarity = 0, Phase = 1, to SPIx_CLK falling		0	
			Polarity = 1, Phase = 0, to SPIx_CLK rising		$0.5t_{c(SPC)M}$	
			Polarity = 1, Phase = 1, to SPIx_CLK rising		0	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
SPI ELECTRICAL DATA/TIMING – Continued (See figure 25 – 30)						
Additional 22/ SPI master timings, 4-Pin Enable option 8/ 23/						
19	Delay from $\overline{\text{SPIx_SCS}}$ active to first SPIx_CLK 26/ 27/	$t_{d(SCS_SPC)M}$	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P-10		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + 2P-10		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P-10		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + 2P-10		
20	Delay from final SPIx_CLK edge to master deasserting $\overline{\text{SPIx_SCS}}$ 28/ 29/	$t_{d(SPC_SCS)M}$	Polarity = 0, Phase = 0, to SPIx_CLK falling	$0.5t_{c(SPC)M}$		
			Polarity = 0, Phase = 1, to SPIx_CLK falling	0		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	$0.5t_{c(SPC)M}$		
			Polarity = 1, Phase = 1, to SPIx_CLK rising	0		
Additional 22/ SPI master timings, 5-Pin option 8/ 23/						
18	Max delay for slave to deassert $\overline{\text{SPIx_ENA}}$ after final SPIx_CLK edge to ensure master does not begin the net transfer 30/		Polarity = 0, Phase = 0, to SPIx_CLK falling		$0.5t_{c(SPC)M}$	ns
			Polarity = 0, Phase = 1, to SPIx_CLK falling		0	
			Polarity = 1, Phase = 0, to SPIx_CLK rising		$0.5t_{c(SPC)M}$	
			Polarity = 1, Phase = 1, to SPIx_CLK rising		0	
20	Delay from final SPIx_CLK edge to master deasserting $\overline{\text{SPIx_SCS}}$ 29/ 31/		Polarity = 0, Phase = 0, to SPIx_CLK falling	$0.5t_{c(SPC)M}$		
			Polarity = 0, Phase = 1, to SPIx_CLK falling	0		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	$0.5t_{c(SPC)M}$		
			Polarity = 1, Phase = 1, to SPIx_CLK rising	0		
21	Max delay for slave SPI to drive $\overline{\text{SPIx_ENA}}$ valid after master asserts $\overline{\text{SPIx_SCS}}$ to delay the master from beginning the next transfer	$t_{d(SCSL_ENAL)M}$			0.5 P	
22	Delay from $\overline{\text{SPIx_SCS}}$ active to first SPIx_CLK 26/ 27/ 32/	$t_{d(SCS_SPC)M}$	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P-10		
			Polarity = 0, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + 2P-10		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P-10		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + 2P-10		
23	Delay from assertion of $\overline{\text{SPIx_ENA}}$ low to first SPIx_CLK edge 33/	$t_{d(ENA_SPC)M}$	Polarity = 0, Phase = 0, to SPIx_CLK rising		3P + 15	
			Polarity = 0, Phase = 1, to SPIx_CLK rising		$0.5t_{c(SPC)M}$ + 3P + 15	
			Polarity = 1, Phase = 0, to SPIx_CLK falling		3P + 15	
			Polarity = 1, Phase = 1, to SPIx_CLK falling		$0.5t_{c(SPC)M}$ + 3P + 15	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
SPI ELECTRICAL DATA/TIMING – Continued (See figure 25 – 30)						
Additional 34/ SPI slave timings, 4-Pin Enable option 8/ 35/						
24	Delay from final SPIx_CJK edge to slave $\overline{\text{SPIx_ENA}}$	$t_{d(SPC_ENAH)S}$	Polarity = 0, Phase = 0, to SPIx_CLK falling	P-10	3P + 15	ns
			Polarity = 0, Phase = 1, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + P-10	$0.5t_{c(SPC)M}$ +3P+15	
			Polarity = 1, Phase = 0, to SPIx_CLK rising	P-10	3P + 15	
			Polarity = 1, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + P-10	$0.5t_{c(SPC)M}$ + 3P+15	
Additional 34/ SPI slave timings, 4-Pin chip select option 8/ 35/						
25	Required delay from $\overline{\text{SPIx_SCS}}$ asserted at slave to first SPIx_CLK edge at slave			P		ns
26	Required delay from final SPIx_CLK edge before $\overline{\text{SPIx_SCS}}$ is deasserted	$t_{d(SPC_SCSH)S}$	Polarity = 0, Phase = 0, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + P-10		
			Polarity = 0, Phase = 1, to SPIx_CLK falling	P-10		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + P-10		
			Polarity = 1, Phase = 1, to SPIx_CLK rising	P-10		
27	Delay from master asserting $\overline{\text{SPIx_SCS}}$ to slave driving SPIx_SOMI valid	$t_{ena(SCSL_SOMI)S}$			P + 15	
28	Delay from master deasserting $\overline{\text{SPIx_SCS}}$ to slave 3-stating SPIx_SOMI	$t_{dis(SCSH_SOMI)S}$			P + 15	
Additional 34/ SPI slave timings, 5-Pin option 8/ 35/						
25	Required delay from $\overline{\text{SPIx_SCS}}$ asserted at slave to first SPIx_CLK edge at slave	$t_{d(SPC_SCSH)S}$		P		ns
26	Required delay from final SPIx_CLK edge before $\overline{\text{SPIx_SCS}}$ is deasserted	$t_{d(SPC_SCSH)S}$	Polarity = 0, Phase = 0, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + P-10		
			Polarity = 0, Phase = 1, to SPIx_CLK falling	P-10		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + P-10		
			Polarity = 1, Phase = 1, to SPIx_CLK rising	P-10		
27	Delay from master asserting $\overline{\text{SPIx_SCS}}$ to slave driving SPIx_SOMI valid	$t_{ena(SCSL_SOMI)S}$			P + 10	
28	Delay from master deasserting $\overline{\text{SPIx_SCS}}$ to slave 3-stating SPIx_SOMI	$t_{dis(SCSH_SOMI)S}$			P + 10	
29	Delay from master asserting $\overline{\text{SPIx_SCS}}$ to slave driving $\overline{\text{SPIx_ENA}}$ valid				15	
30	Delay from final clock receive edge on SPIx_CLK to slave 3-tarting or driving high $\overline{\text{SPIx_ENA}}$ 36/		Polarity = 0, Phase = 0, to SPIx_CLK falling		2P + 15	
			Polarity = 0, Phase = 1, to SPIx_CLK falling		2P + 15	
			Polarity = 1, Phase = 0, to SPIx_CLK rising		2P + 15	
			Polarity = 1, Phase = 1, to SPIx_CLK rising		2P + 15	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits		Unit
				Min	Max	
	I2C ELECTRICAL DATA/TIMING (See Figure 31-33)					
I2C input timing requirements						
1	Cycle time, I2Cx_SCL	$t_{c(SCL)}$	Standard Mode	10		µs
			Fast Mode	2.5		
2	Setup time, I2Cx_SCL high before I2Cx_SDA low	$t_{su(SCLH_SDAL)}$	Standard Mode	4.7		
			Fast Mode	0.6		
3	Hold time, I2Cx_SCL low after I2Cx_SDA low	$t_{h(SCLL_SDAL)}$	Standard Mode	4		
			Fast Mode	0,6		
4	Pulse duration, I2Cx_SCL low	$t_{w(SCLL)}$	Standard Mode	4.7		
			Fast Mode	1.3		
5	Pulse duration, I2Cx_SCL high	$t_{w(SCLH)}$	Standard Mode	4		
			Fast Mode	0.6		
6	Setup time, I2Cx_SDA before I2Cx_SCL high	$t_{su(SDA_SCLH)}$	Standard Mode	250		
			Fast Mode	100		
7	Hold time, I2Cx_SDA after I2Cx_SCL low	$t_{h(SDA_SCLL)}$	Standard Mode	0		
			Fast Mode	0	0.9	
8	Pulse duration, I2Cx_SDA high	$t_{w(SDAH)}$	Standard Mode	4.7		
			Fast Mode	1.3		
9	Rise time, I2Cx_SDA	$t_{r(SDA)}$	Standard Mode		1000	ns
			Fast Mode	$20+0.1C_b$	300	
10	Rise time, I2Cx_SCL	$t_{r(SCL)}$	Standard Mode		1000	
			Fast Mode	$20+0.1C_b$	300	
11	Fall time, I2Cx_SDA	$t_{f(SDA)}$	Standard Mode		1000	
			Fast Mode	$20+0.1C_b$	300	
12	Fall time, I2Cx_SCL	$t_{f(SCL)}$	Standard Mode		1000	
			Fast Mode	$20+0.1C_b$	300	
13	Setup time, I2Cx_SCL high before I2Cx_SDA high	$t_{su(SCLH_SDAH)}$	Standard Mode	4		µs
			Fast Mode	0.6		
14	Pulse duration, spike (must be suppressed)	$t_{w(SP)}$	Standard Mode	N/A		ns
			Fast Mode	0	50	
15	Capacitive load for each bus line	C_b	Standard Mode		400	pF
			Fast Mode		400	

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Conditions 2/	Limits Min	Limits Max	Unit
	I2C ELECTRICAL DATA/TIMING – Continued (See Figure 31-33)					
I2C switching characteristics 37/						
16	Cycle time, I2Cx_SCL	$t_{c(SCL)}$	Standard Mode	10		µs
			Fast Mode	2.5		
17	Setup time, I2Cx_SCL high before I2Cx_SDA low	$t_{su(SCLH_SDAL)}$	Standard Mode	4.7		
			Fast Mode	0.6		
18	Hold time, I2Cx_SCL low after I2Cx_SDA low	$t_{h(SDAL_SCLL)}$	Standard Mode	4		
			Fast Mode	0,6		
19	Pulse duration, I2Cx_SCL low	$t_{w(SCLL)}$	Standard Mode	4.7		
			Fast Mode	1.3		
20	Pulse duration, I2Cx_SCL high	$t_{w(SCLH)}$	Standard Mode	4		
			Fast Mode	0.6		
21	Setup time, I2Cx_SDA valid before I2Cx_SCL high	$t_{su(SDAV_SCLH)}$	Standard Mode	250		
			Fast Mode	100		
22	Hold time, I2Cx_SDA valid after I2Cx_SCL low	$t_{h(SCLL_SDAV)}$	Standard Mode	0		
			Fast Mode	0	0.9	
23	Pulse duration, I2Cx_SDA high	$t_{w(SDAH)}$	Standard Mode	4.7		
			Fast Mode	1.3		
28	Setup time, I2Cx_SCL high before I2Cx_SDA high	$t_{su(SCLH_SDAH)}$	Standard Mode	4		
			Fast Mode	0.6		
29	capacitive load on each bus line from this device	C_b	Standard Mode		10	pF
			Fast Mode		10	
	CLOCK ELECTRICAL DATA/TIMING (See figure 34-37)					
CLKIN timing requirements						
1	Oscillator frequency range (OSCIN/OSCOUT)	f_{OSC}		12		MHz
2	Cycle time, external clock driven on CLKIN	$t_{c(CLKIN)}$		20		ns
3	Pulse width, CLKIN high	$t_{w(CLKINH)}$		$0.4t_{c(CLKIN)}$		
4	Pulse width, CLKIN low	$t_{w(CLKINL)}$		$0.4t_{c(CLKIN)}$		
5	Transition time, CLKIN	$t_{t(CLKIN)}$			5	
6	Frequency range of PLL input	f_{PLL}		12	50	MHz

See footnote at end of table.

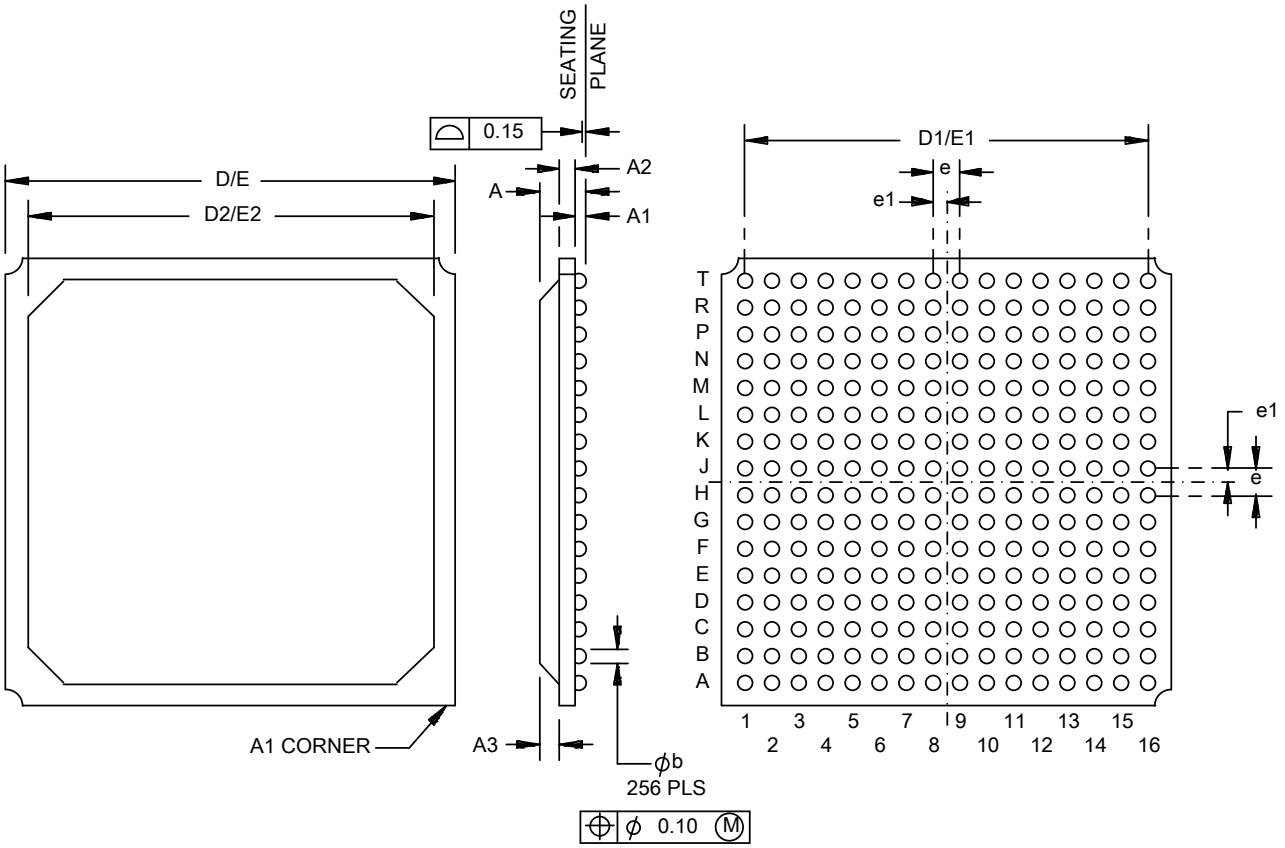
TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over operating case temperature range (unless otherwise noted).
3/ Assumes the following conditions : 25°C case temperature; 60% CPU utilization; EMIF at 50% utilization (100 MHz), 50% writes, (32 bits), 50% bit switching; two 10 MHz SPI at 100% utilization, 50% bit switching.
The actual current draw is highly application dependent. For more details on core and I/O activity, refer to manufacturer data.
4/ E = SYSCLK3 (EM_CLK) period.
5/ Thes parameters apply to memories selected by $\overline{\text{EM_CS[2]}}$ in beth normal and NAND modes.
6/ Thes parameters specify the number of EM_CLK cycles of latency between EM_WAIT being sampled at the device pin and the EMIF entering the HOLD phase. However, the asynchronous setup (parameter 30) and hold time (parameter 31) around each EM_CLK edge must also be met in order to ensure the EM_WAIT signal is correct sampled.
7/ In Figure 13, it appears that there are more than 4 EM_CLK cycles encompassed by parameter 35. However, EM_CLK cycles that are part of the extended wait period should not be counted; the 4 EM_CLK requirements is to the start of where the HOLD phase would begin if there were no extended wait cycles.
8/ P = SYSCLK2 period.
9/ DS refers to $\overline{\text{HSTROBE}}$. HD refers to UHPI_HD[31:0]. HDS refers to $\overline{\text{UHPI_HDS[1]}}$ or , $\overline{\text{UHPI_HDS[2]}}$. HAD refers to UHPI_HCNTL[0], UHPI_HCNTL[1], UHPI_HHWIL, and UHPI_HR$\overline{\text{W}}$.
10/ H = 0.5 * SYSCLK2 period.
11/ Max delay is a best case, assuming no delays due to resource conflicts between UHPI and dMAX or CPU. $\overline{\text{UHPI_HRDY}}$ should always to be used to indicate when an access is complete instead of relying on these parameters.
12/ ACLKX internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR internal – ACLKRCTL.CLKXM = 1, PDIR.ACLKR = 1
ACLKR external input – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
13/ AHR – Cycle time, AHCLKR.
14/ AHX – Cycle time, AHCLKX.
15/ AR – ACLKR period.
16/ AX – ACLKX period.
17/ First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPIx_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPIx_SOMI.
18/ The final data bit will be held on the SPIx_SIMO pin until the SPIDAT0 or SPIDAT1 register is writtern with new data.
19/ First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPIx_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPIx_SIMO.
20/ Measured from termination of the write of new data to the SPI module, as evidenced by new output data appearing on the SPIx_SOMI pin. In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be writtern to the SPI module by either the DSP CPU or the dMAX.
21/ The final data bit will be held on the SPIx_SOMI pin until the SPIDAT0 or SPIDAT1 register is writtern with new data.
22/ These parameters are in addition to the general timing for SPI master modes on sheet 10.
23/ Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
24/ In the case where the master SPI is ready with new data before $\overline{\text{SPIx_ENA}}$ assertion.
25/ In the case where the master SPI is ready with new data before $\overline{\text{SPIx_ENA}}$ deassertion.
26/ In the case where the master SPI is ready with new data before $\overline{\text{SPIx_SCS}}$ assertion.
27/ This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
28/ Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case $\overline{\text{SPIx_SCS}}$ will remain asserted.
29/ This delay can be increased under software control by the register bit field SPIDELAY.T2CTDELAY[4:0].
30/ In the case where the master SPI is ready with new data before $\overline{\text{SPIx_ENA}}$ deassertion.

TABLE I. Electrical performance characteristics – Continued. 1/

31/ Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case $\overline{\text{SPIx_SCS}}$ will remain asserted.
32/ If $\overline{\text{SPIx_ENA}}$ is asserted immediately such that the transmission in not delayed by $\overline{\text{SPIx_ENA}}$.
33/ If $\overline{\text{SPIx_ENA}}$ was initially deasserted high and SPIx_CLK is delayed.
34/ These parameters are in addition to the general timing for SPI slave modes on sheet 11.
35/ Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
36/ $\overline{\text{SPIx_ENA}}$ isdriven low after the transmission completes if the SPINT0.ENABLE_HIGHZ bits is programmed to 0. Otherwise it is 3-stated. If 3-stated, an external pulluo resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.
37/ I2C must be configured correctly to meet the timings in this table.

Case X



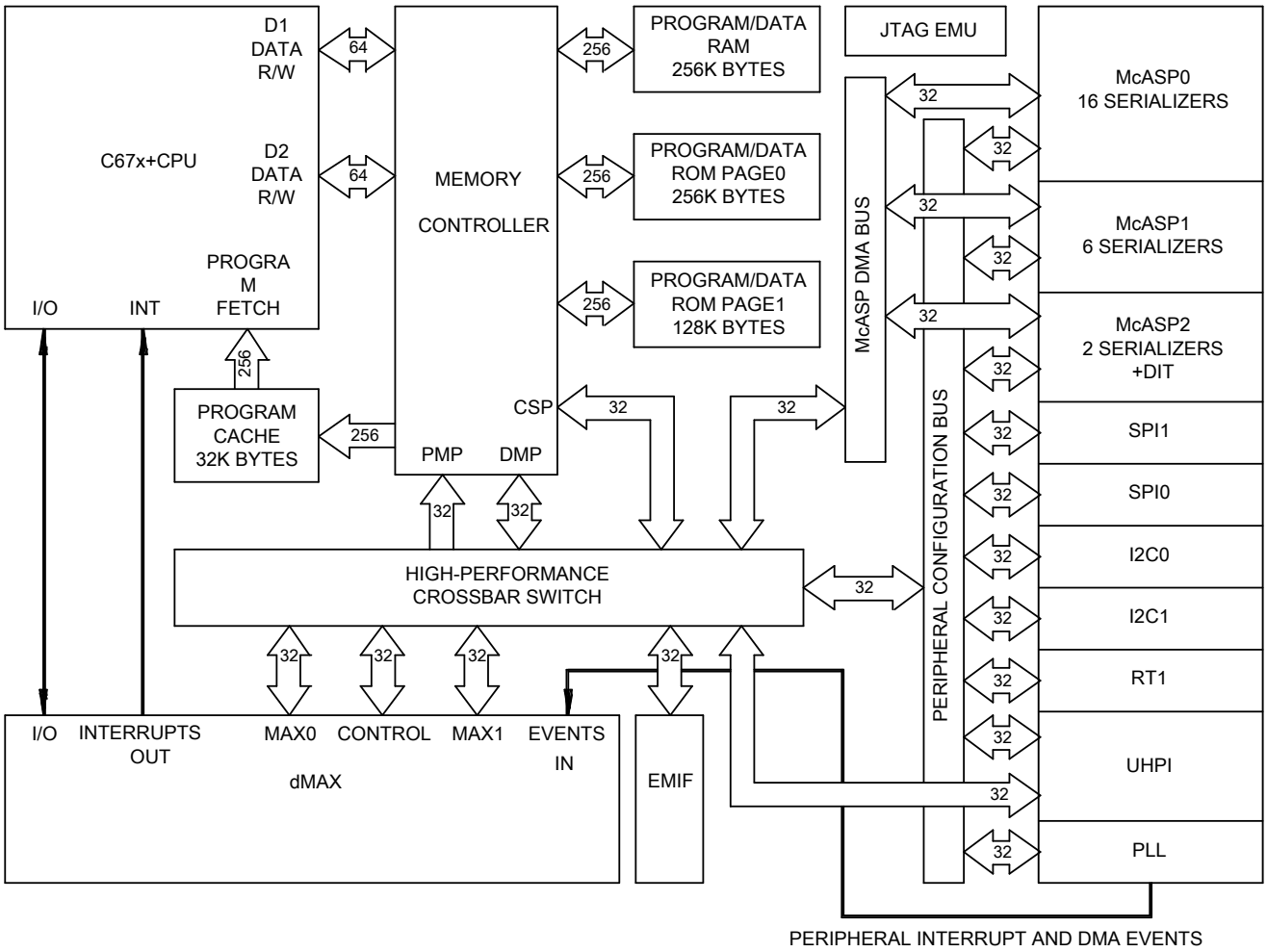
Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		2.02	D1/E1	15.00 TYP	
A1	0.30	0.50	D2/E2	14.95	15.70
A2	0.55	0.67	e	1.00 TYP	
A3	0.75	0.85	e1	0.50 TYP	
D/E	16.80	17.20			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Thermally enhanced plastic package.

FIGURE 1. Case outline.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T	V_{SS}	DV_{DD}	$\overline{EM_WE}$	EM_D[7]	EM_D[5]	EM_D[3]	V_{SS}	EM_D[0]	EM_D[14]	V_{SS}	EM_D[11]	EM_D[9]	EM_$\overline{WE}$_DQM[1]	EM_CKE	DV_{DD}	V_{SS}
R	DV_{DD}	EM_D[23] /UHPI_HA[7]	$\overline{EM_CAS}$	EM_$\overline{WE}$_DQM[0]	EM_D[6]	EM_D[4]	EM_D[2]	EM_D[1]	EM_D[15]	EM_D[13]	EM_D[12]	EM_D[10]	EM_D[8]	EM_CLK	EM_$\overline{WE}$_DQM[3]	DV_{DD}
P	TCK	UHPI_HD[24]	EM_D[21] /UHPI_HA[5]	EM_D[20] /UHPI_HA[4]	EM_D[19] /UHPI_HA[3]	EM_D[17] /UHPI_HA[1]	EM_D[31] /UHPI_HA[15]	DV_{DD}	EM_D[28] /UHPI_HA[12]	EM_D[26] /UHPI_HA[10]	EM_D[24] /UHPI_HA[8]	EM_A[12]	EM_$\overline{WE}$_DQM[2]	UHPI_HD[7]	EM_A[11]	EM_A[9]
N	$\overline{EMU[1]}$	UHPI_HD[25]	UHPI_HD[26]	EM_D[22] /UHPI_HA[6]	DV_{DD}	EM_D[18] /UHPI_HA[2]	EM_D[16] /UHPI_HA[0]	EM_D[30] /UHPI_HA[14]	EM_D[29] /UHPI_HA[13]	EM_D[27] /UHPI_HA[11]	EM_D[25] /UHPI_HA[9]	DV_{DD}	UHPI_HD[5]	UHPI_HD[6]	EM_A[8]	EM_A[7]
M	$\overline{EMU[0]}$	TDO	UHPI_HD[27]	DV_{DD}	V_{SS}	CV_{DD}	CV_{DD}	CV_{DD}	CV_{DD}	CV_{DD}	CV_{DD}	V_{SS}	DV_{DD}	UHPI_HD[2]	EM_A[6]	EM_A[5]
L	TDI	UHPI_HD[30]	UHPI_HD[28]	UHPI_HD[29]	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	UHPI_HD[3]	UHPI_HD[4]	EM_A[4]	EM_A[3]
K	V_{SS}	PLLHV	TMS	$\overline{TRST}$	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CV_{DD}	UHPI_HD[0]	UHPI_HD[1]	EM_A[2]	V_{SS}
J	$OSCV_{SS}$	OSCIN	OSCOUT	$OSCV_{DD}$	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CV_{DD}	UHPI_HD[15]	DV_{DD}	EM_A[1]	EM_A[0]
H	UHPI_HD[16] /HHWIL	CLKIN	V_{SS}	UHPI_HD[31]	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CV_{DD}	UHPI_HD[14]	UHPI_HD[13]	EM_A[10]	EM_BA[1]
G	V_{SS}	$\overline{RESET}$	UHPI_HD[17]	UHPI_HD[18]	CV_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CV_{DD}	UHPI_HD[12]	UHPI_HD[11]	EM_BA[0]	V_{SS}
F	AFSR1	AFSX1	UHPI_HD[19]	UHPI_HD[20]	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	UHPI_HD[10]	UHPI_HD[9]	$\overline{EM_CS[0]}$	$\overline{EM_RAS}$
E	ACLKR1	ACLKX1	UHPI_HD[21]	DV_{DD}	V_{SS}	CV_{DD}	CV_{DD}	CV_{DD}	CV_{DD}	CV_{DD}	CV_{DD}	V_{SS}	DV_{DD}	UHPI_HD[8]	$\overline{EM_CS[2]}$	EM_$\overline{RW}$
D	AHCLKX1	AMUTE1	UHPI_HD[22]	DV_{DD}	DV_{DD}	$\overline{UHPI_HRDY}$	$\overline{UHPI_HDS[1]}$	UHPI_$\overline{HRW}$	UHPI_HCNTL[0]	AMUTE2/$\overline{HINT}$	ACLKX2	DV_{DD}	DV_{DD}	EM_WAIT	$\overline{EM_OE}$	$\overline{SPI0_ENA}$ /I2C1_SDA
C	AMUTE0	AHCLKX0 /AHCLKX2	UHPI_HD[23]	$\overline{UHPI_HBE[2]}$	$\overline{UHPI_HBE[1]}$	$\overline{UHPI_HBE[0]}$	$\overline{UHPI_HDS[2]}$	$\overline{UHPI_HCS}$	$\overline{UHPI_HAS}$	UHPI_HCNTL[1]	AFSX2	AFSR2	ACLKR2	AHCLKR2	$\overline{SPI0_SCS}$ /I2C1_SCL	SPI0_CLK /I2C0_SCL
B	DV_{DD}	$\overline{UHPI_HBE[3]}$	AHCLKR0 /AHCLKR1	AFSR0	AXR0[15] /AXR2[0]	AXR0[13] /AXR1[0]	AXR0[12] /AXR1[1]	AXR0[10] /AXR1[3]	AXR0[8] /AXR1[5] /SPI1_SOMI	AXR0[7] /SPI1_CLK	AXR0[5] /$\overline{SPI1_SCS}$	AXR0[3]	AXR0[1]	SPI0_SOMI /I2C0_SDA	SPI0_SIMO	DV_{DD}
A	V_{SS}	DV_{DD}	AFSX0	ACLKX0	ACLKR0	AXR0[14] /AXR2[1]	V_{SS}	AXR0[11] /AXR1[2]	AXR0[9] /AXR1[4] /SPI1_SIMO	V_{SS}	AXR0[6] /$\overline{SPI1_ENA}$	AXR0[4]	AXR0[2]	AXR0[0]	DV_{DD}	V_{SS}

FIGURE 2. Terminal connections.



NOTES:
1. UHPI is available only on this device. McASP2 is not available on this device.

FIGURE 3. Functional block diagram.

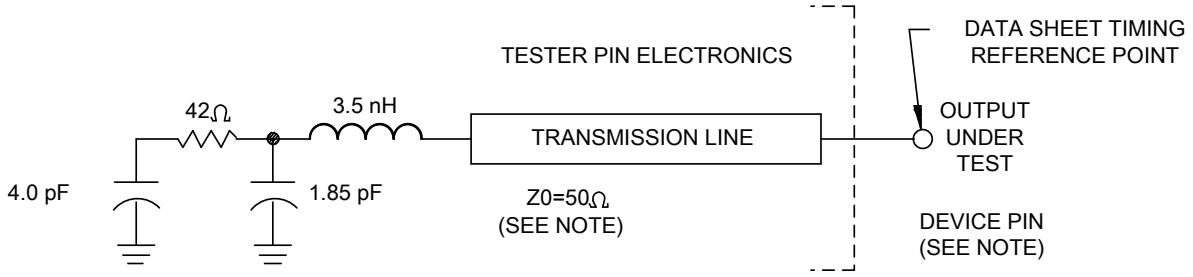
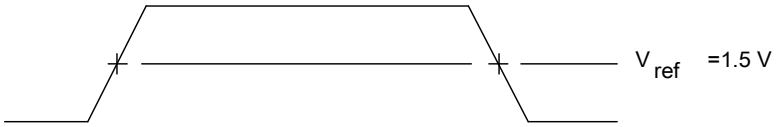
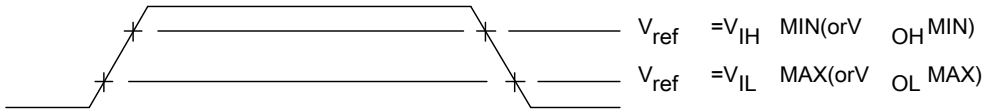


FIGURE 4. Test load circuit for AC timing measurements.

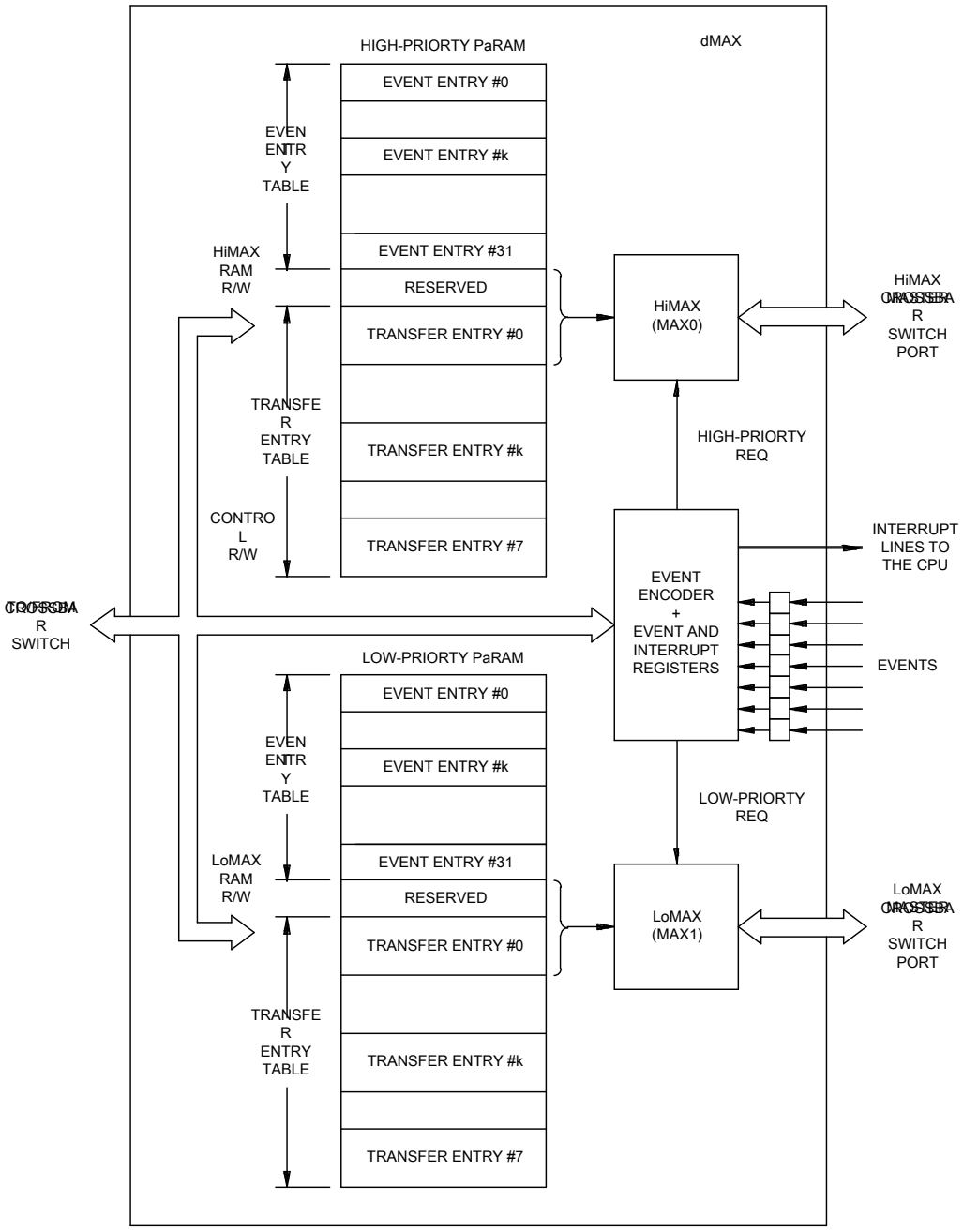


INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASURMENTS



RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

FIGURE 5. Signal transitions levels.



dMAX CONTROLLER BLOCK DIAGRAM

FIGURE 6. dMAX controller block diagram.

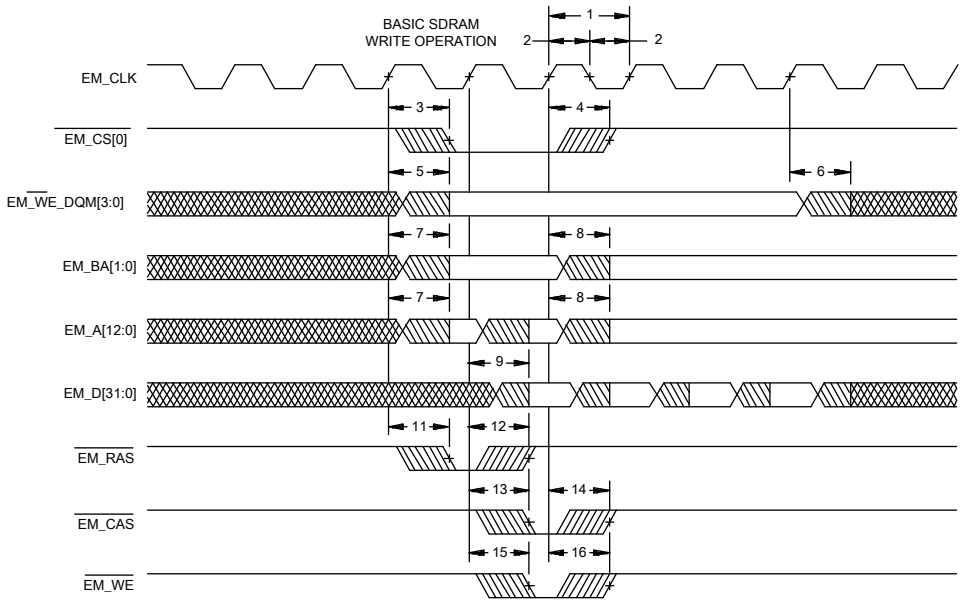


FIGURE 7. Basic SDRAM write operation.

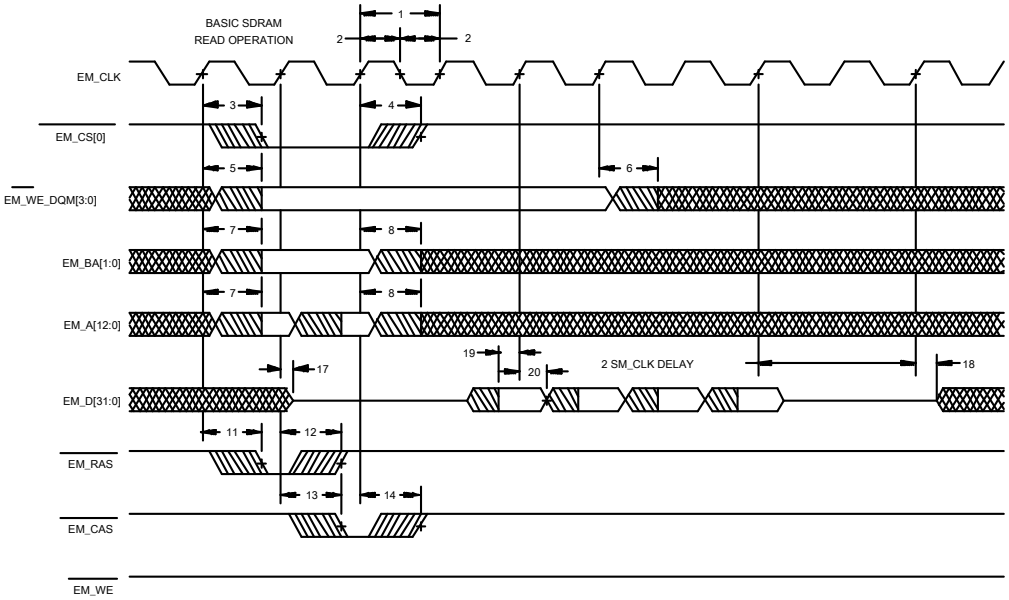


FIGURE 8. Basic SDRAM read operation.

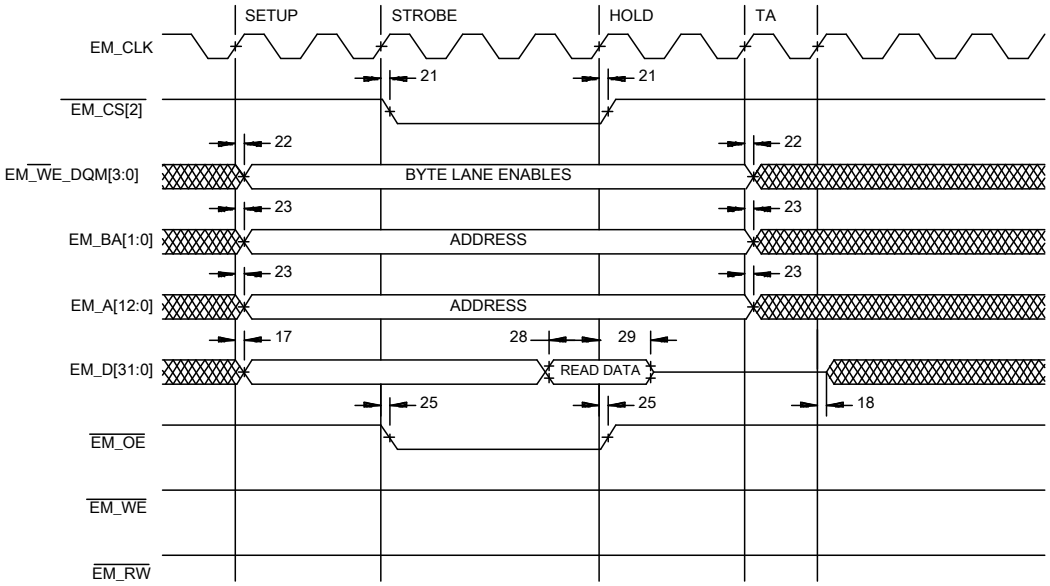


FIGURE 9. Asynchronous read WE strobe mode

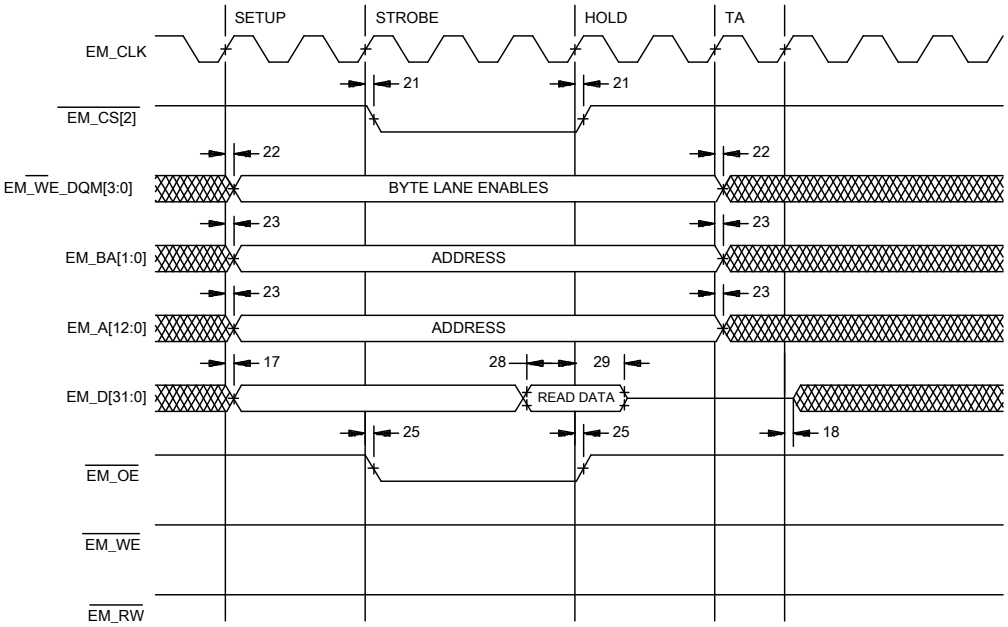


FIGURE 10. Asynchronous read select strobe mode

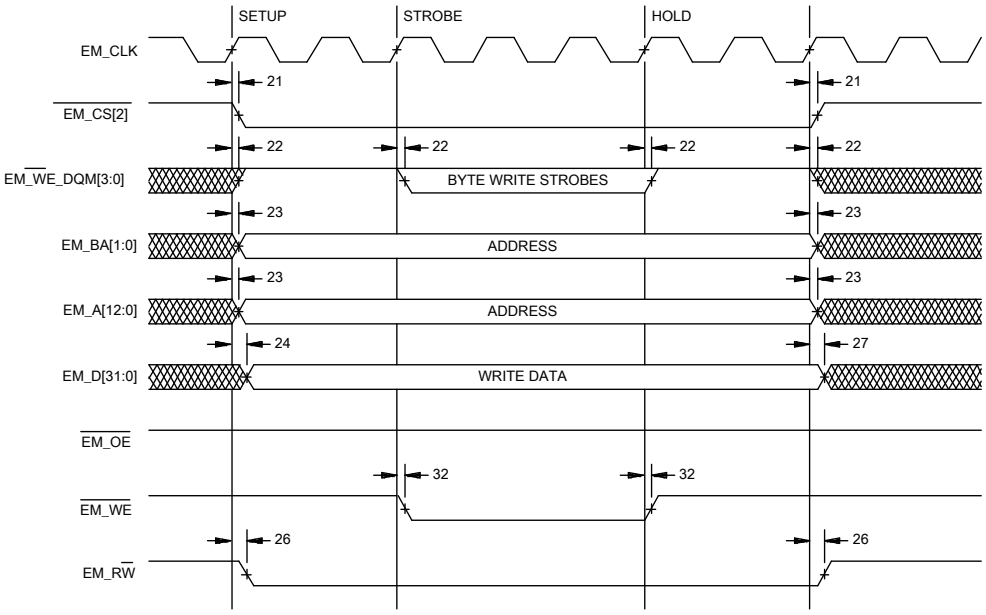


FIGURE 11. Asynchronous write WE strobe mode.

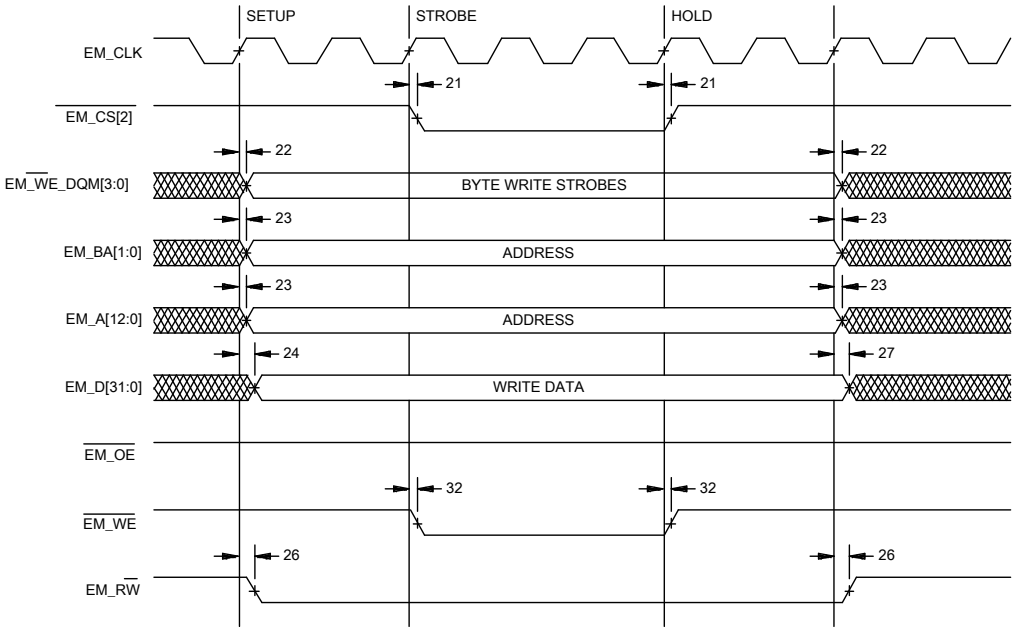


FIGURE 12. Asynchronous write select strobe mode.

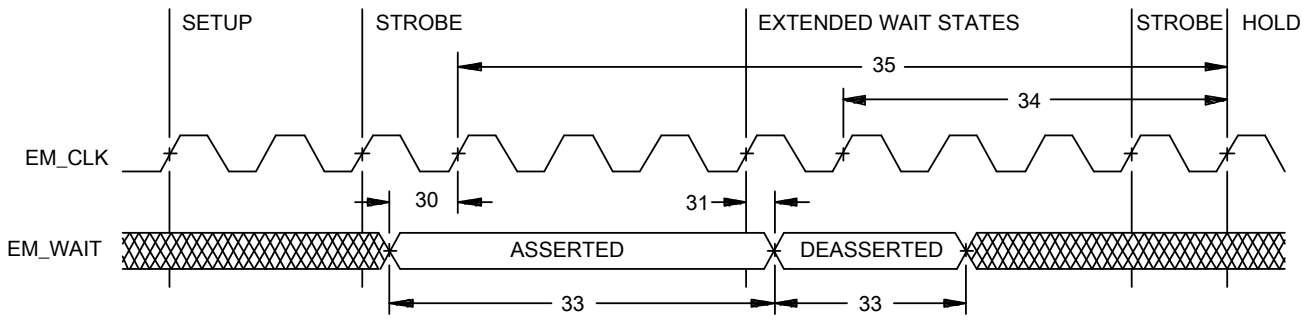


FIGURE 13. EM_WAIT timing requirements.

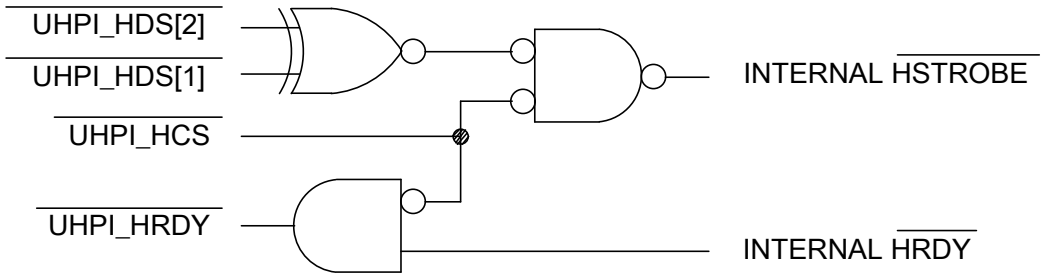
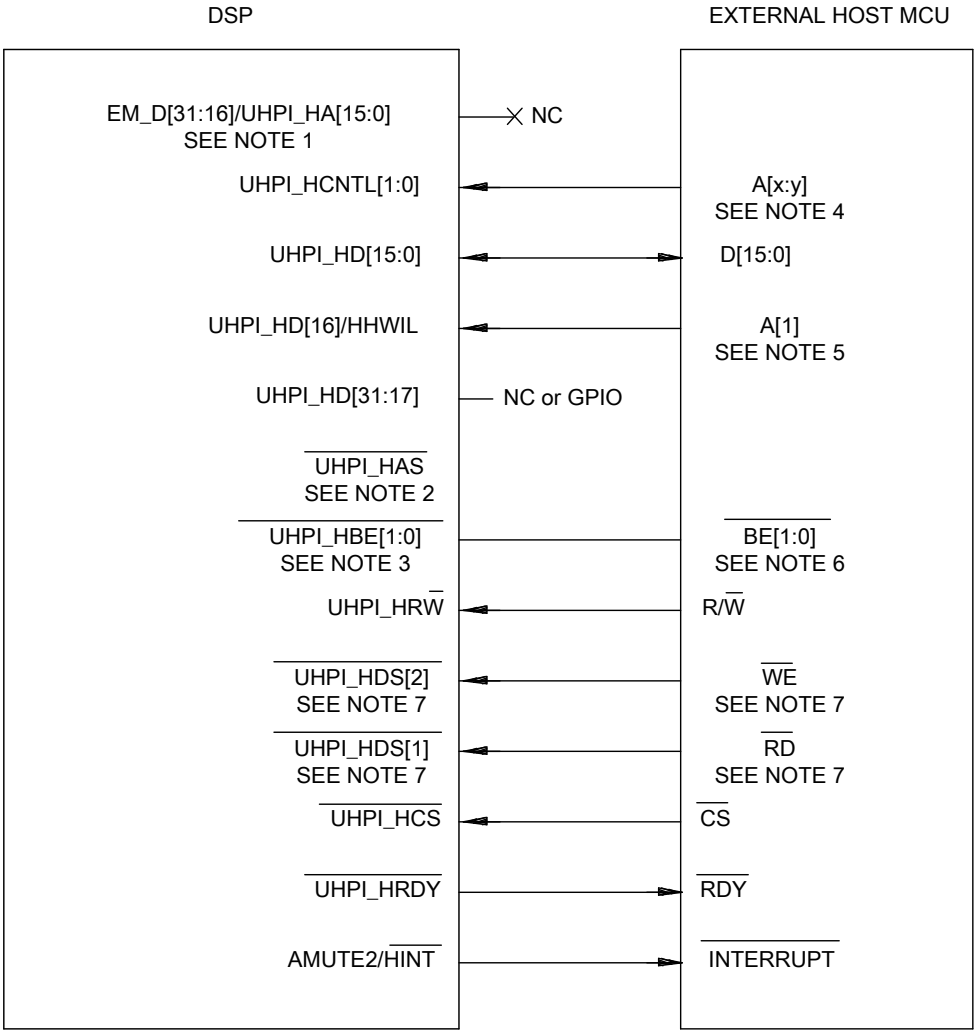


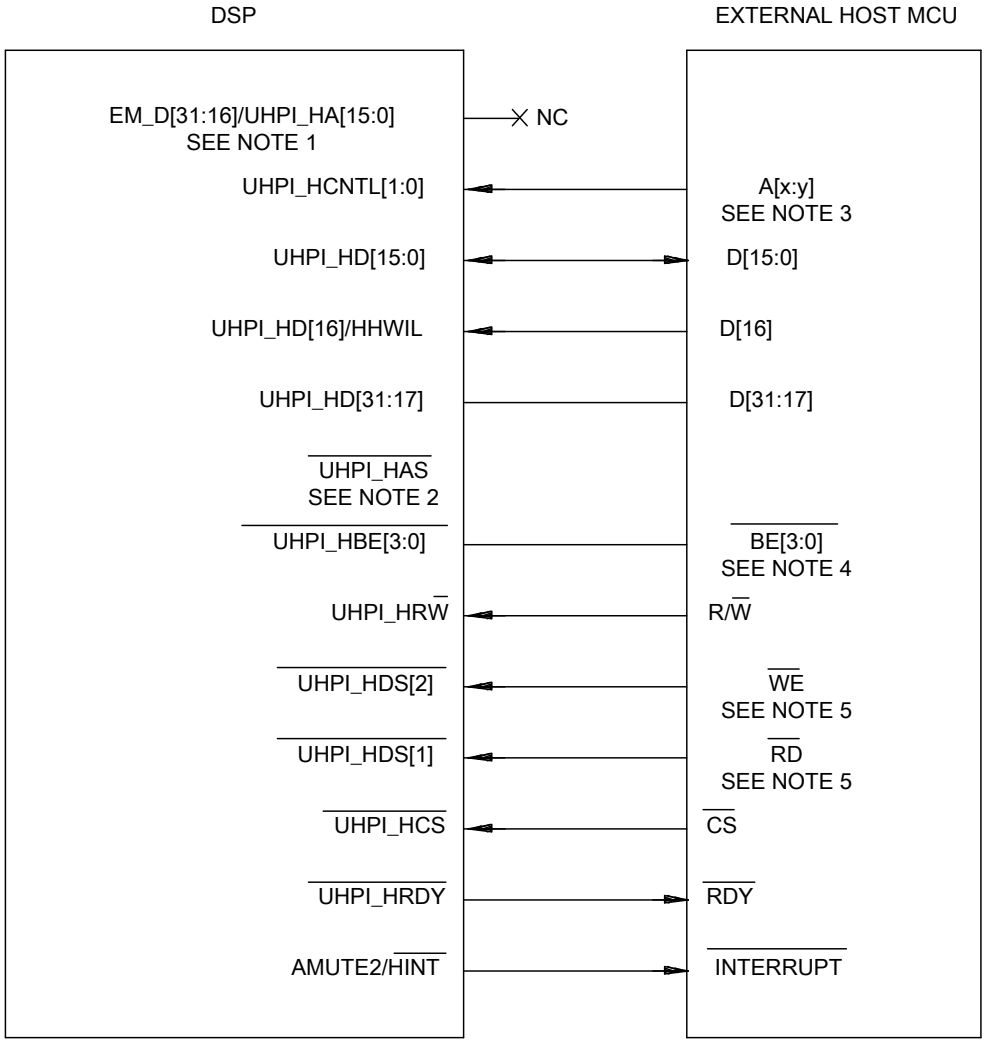
FIGURE 14. UHPI strobe and ready interaction.



NOTES:

1. May be used as EM_D[31:16]
2. Optional for hosts supporting multiplexed address and data. Pull up if not used. Low when address is on data bus.
3. DSP byte enables $\overline{\text{UHPI_HBE[3:2]}}$ and not required in this mode.
4. Two host address lines or host GPIO is address lines are not available.
5. A[1], assuming this address increments from 0 to 1 between two successive 16 bit accesses.
6. Byte enables (active during reads and writes). Some processors support a byte-enable mode on their write-enable pins.
7. Only required if needed for strobe timing. Not required if $\overline{\text{CS}}$ meets strobe timing requirements. Tie $\overline{\text{UHPI_HDS[2]}}$ and $\overline{\text{UHPI_HDS[1]}}$ opposite. For more information see Figure 14.

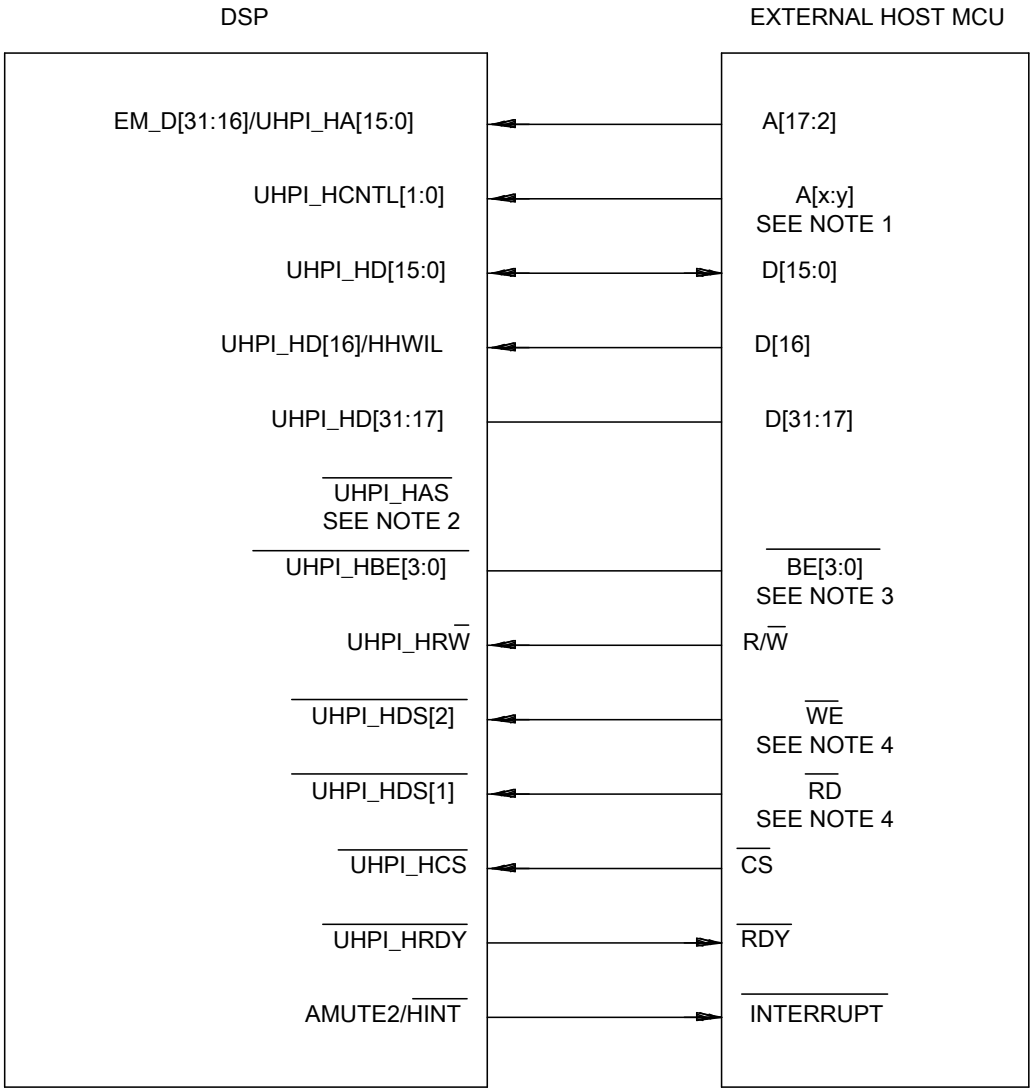
FIGURE 15. UHPI multiplexed host address/Data Half-Word mode.



NOTES:

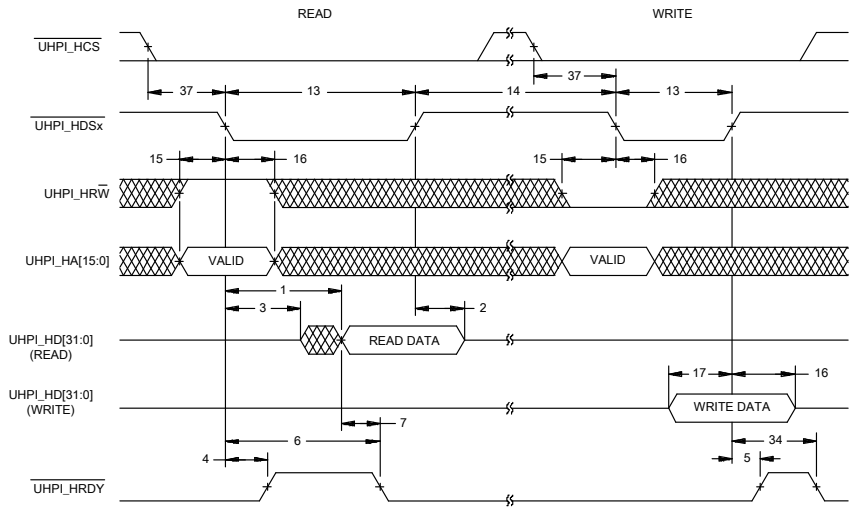
1. May be used as EM_D[31:16]
2. Optional for hosts supporting multiplexed address and data. Pull up if not used. Low when address is on data bus.
3. Two host address lines or host GPIO is address lines are not available.
4. Byte enables (active during reads and writes). Some processors support a byte-enable mode on their write-enable pins.
5. Only required if needed for strobe timing. Not required if $\overline{CS}$ meets strobe timing requirements.

FIGURE 16. UHPI multiplexed host address/Data FullWord mode



NOTES:
1. Two host address lines or host GPIO is address lines are not available.
2. Not used in this mode.
3. Byte enables (active during reads and writes). Some processors support a byte-enable mode on their write-enable pins.
4. Only required if needed for strobe timing. Not required if $\overline{CS}$ meets strobe timing requirements.

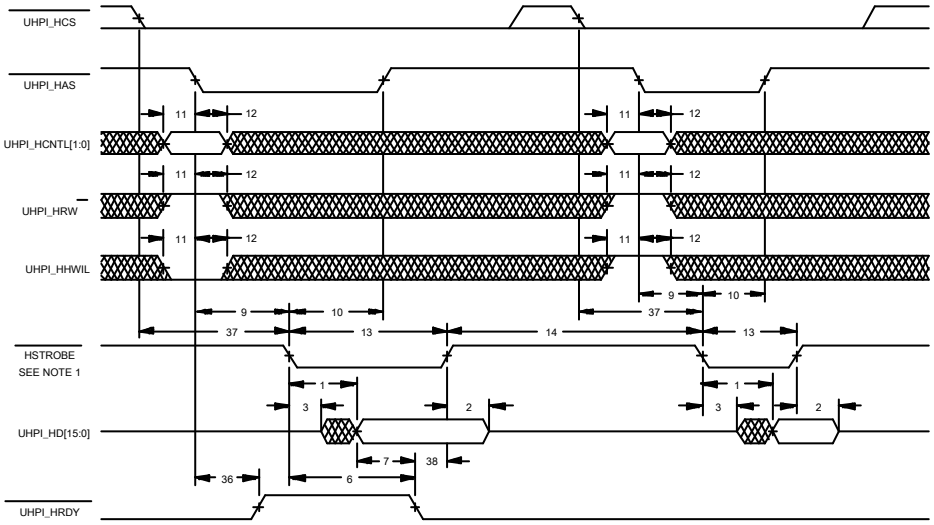
FIGURE 17. UHPI Non-multiplexed host address/Data FullWord mode



NOTES:

1. Depending on the type of write or read operation (HDIP or HPIC), transactions on $\overline{\text{UHPI_HRDY}}$ may or may not occur.

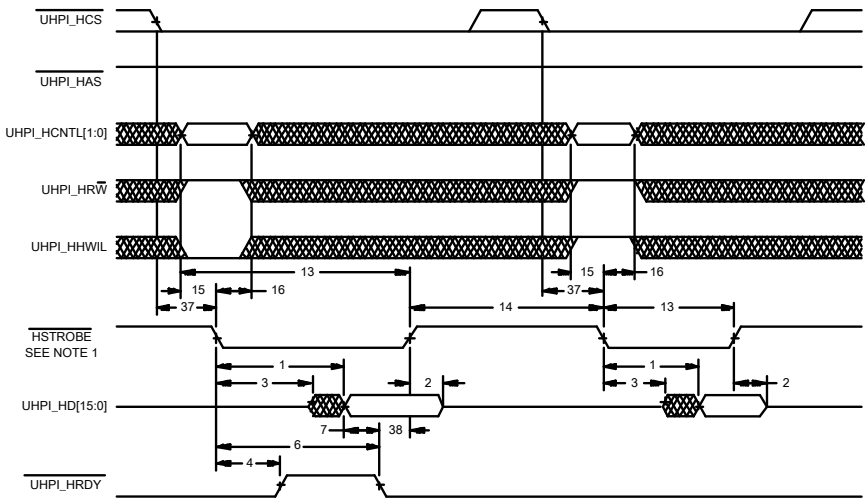
FIGURE 18. Non-Multiplexed Read/Write timings.



NOTES:

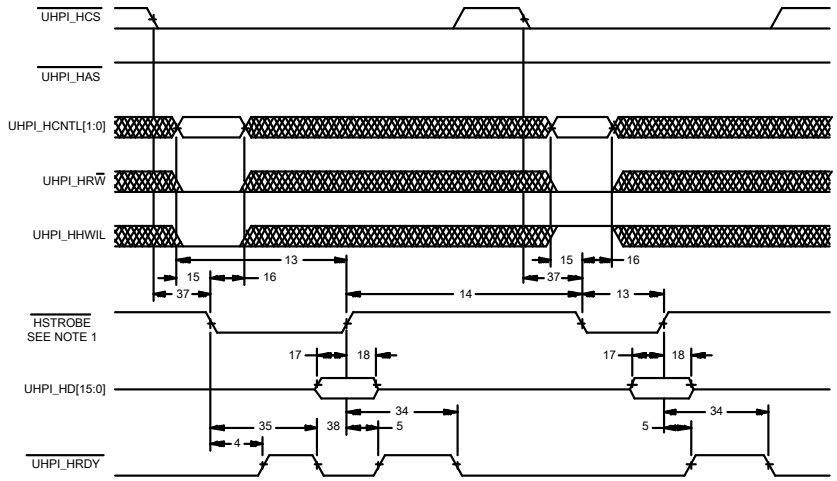
1. See Figure 14.
2. Depending on the type of write or read operation (HDIP without auto-incrementing, HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transactions on $\overline{\text{UHPI_HRDY}}$ may or may not occur.

FIGURE 19. Multiplexed Read timings using $\overline{\text{UHPI_HAS}}$.



NOTES:
1. See Figure 14.
2. Depending on the type of write or read operation (HDIP without auto-incrementing, HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transactions on $\overline{\text{UHPI_HRDY}}$ may or may not occur.

FIGURE 20. Multiplexed Read timings with $\overline{\text{UHPI_HAS}}$ held high.



NOTES:
1. See Figure 14.
2. Depending on the type of write or read operation (HDIP without auto-incrementing, HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transactions on $\overline{\text{UHPI_HRDY}}$ may or may not occur.

FIGURE 21. Multiplexed Write timings with $\overline{\text{UHPI_HAS}}$ held high.

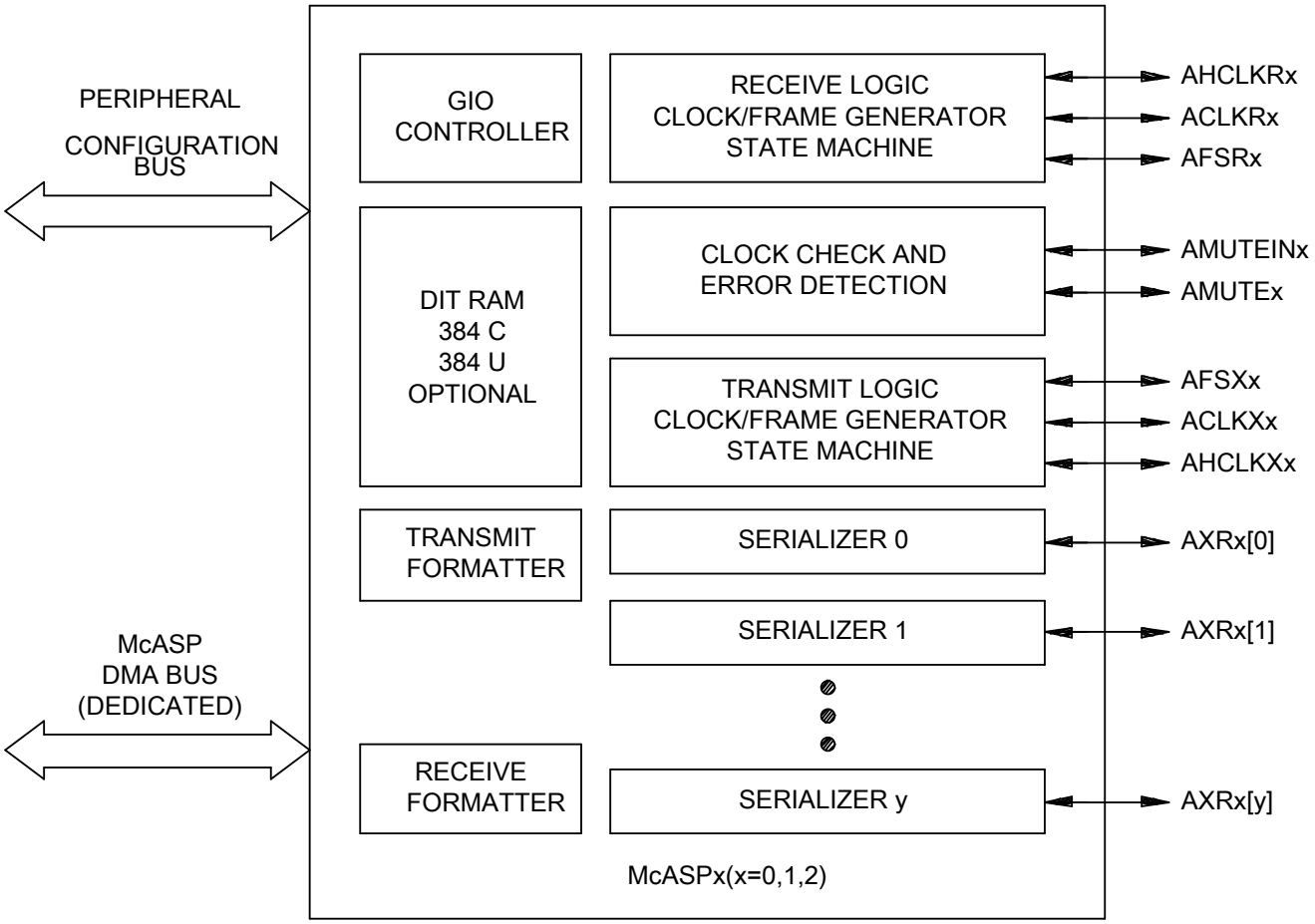
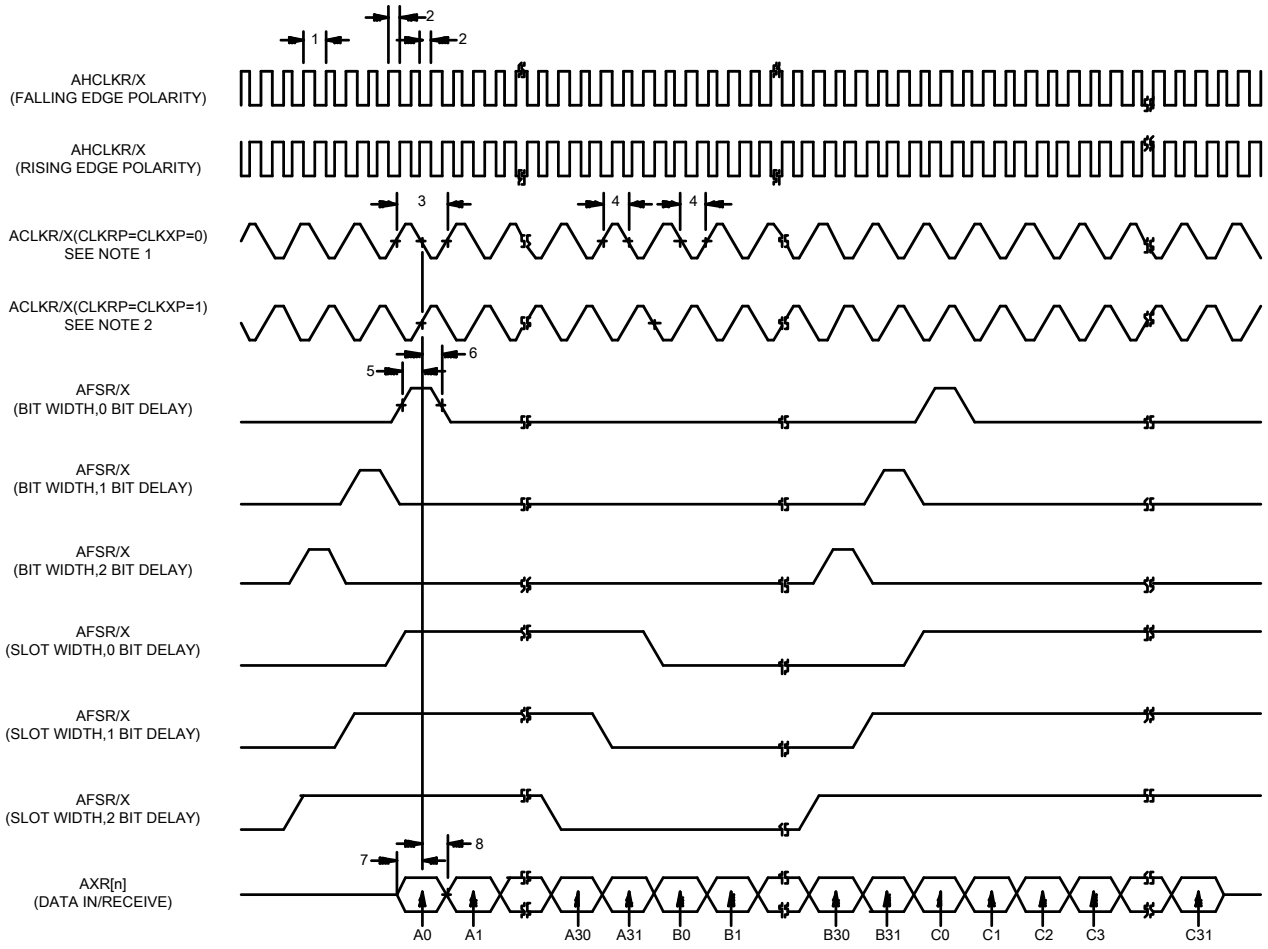


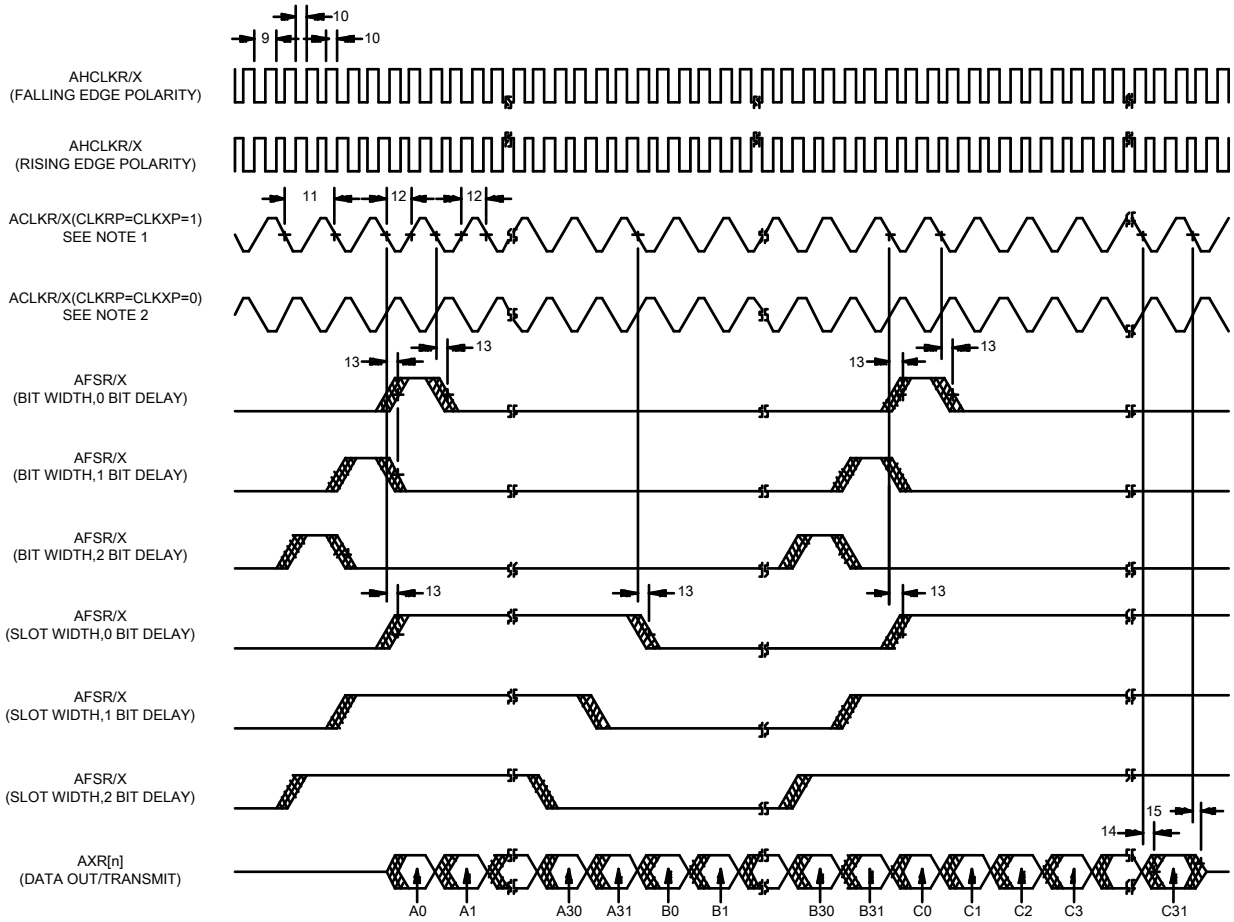
FIGURE 22. McASP block diagram.



NOTES:

1. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shif data out) and the McASP receiver is configured for falling edge (to shift data in).
2. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shif data out) and the McASP receiver is configured for rising edge (to shift data in).

FIGURE 23. McASP input timings.



NOTES:

1. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shif data out) and the McASP receiver is configured for rising edge (to shift data in).
2. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shif data out) and the McASP receiver is configured for falling edge (to shift data in).

FIGURE 24. McASP output timings.

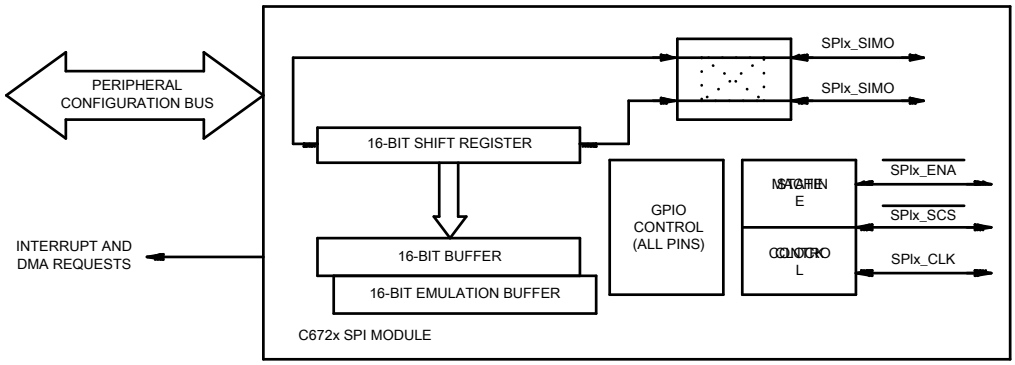


FIGURE 25. Block diagram of SPI module.

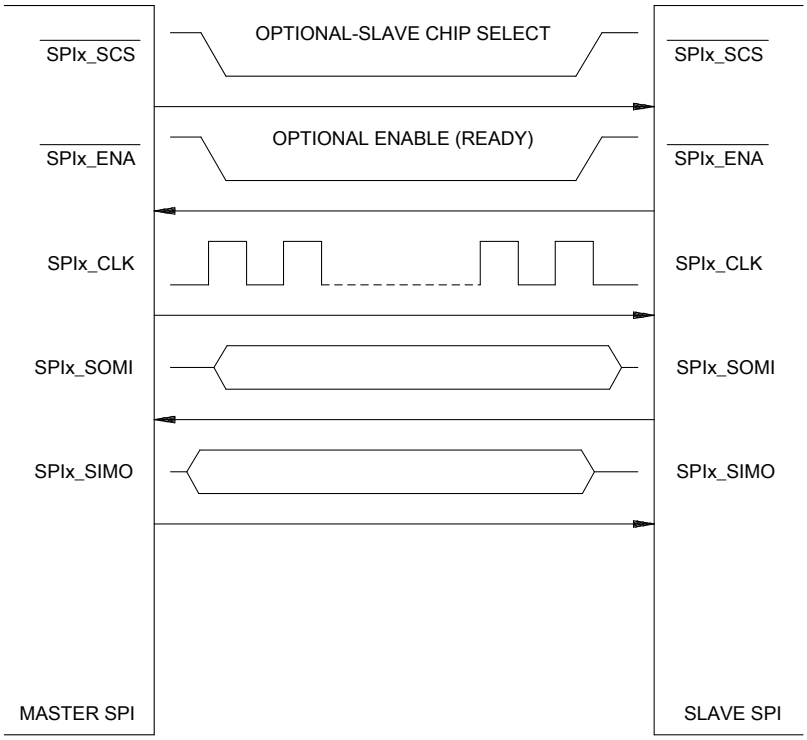


FIGURE 26. Illustration of SPI master to SPI slave connection.

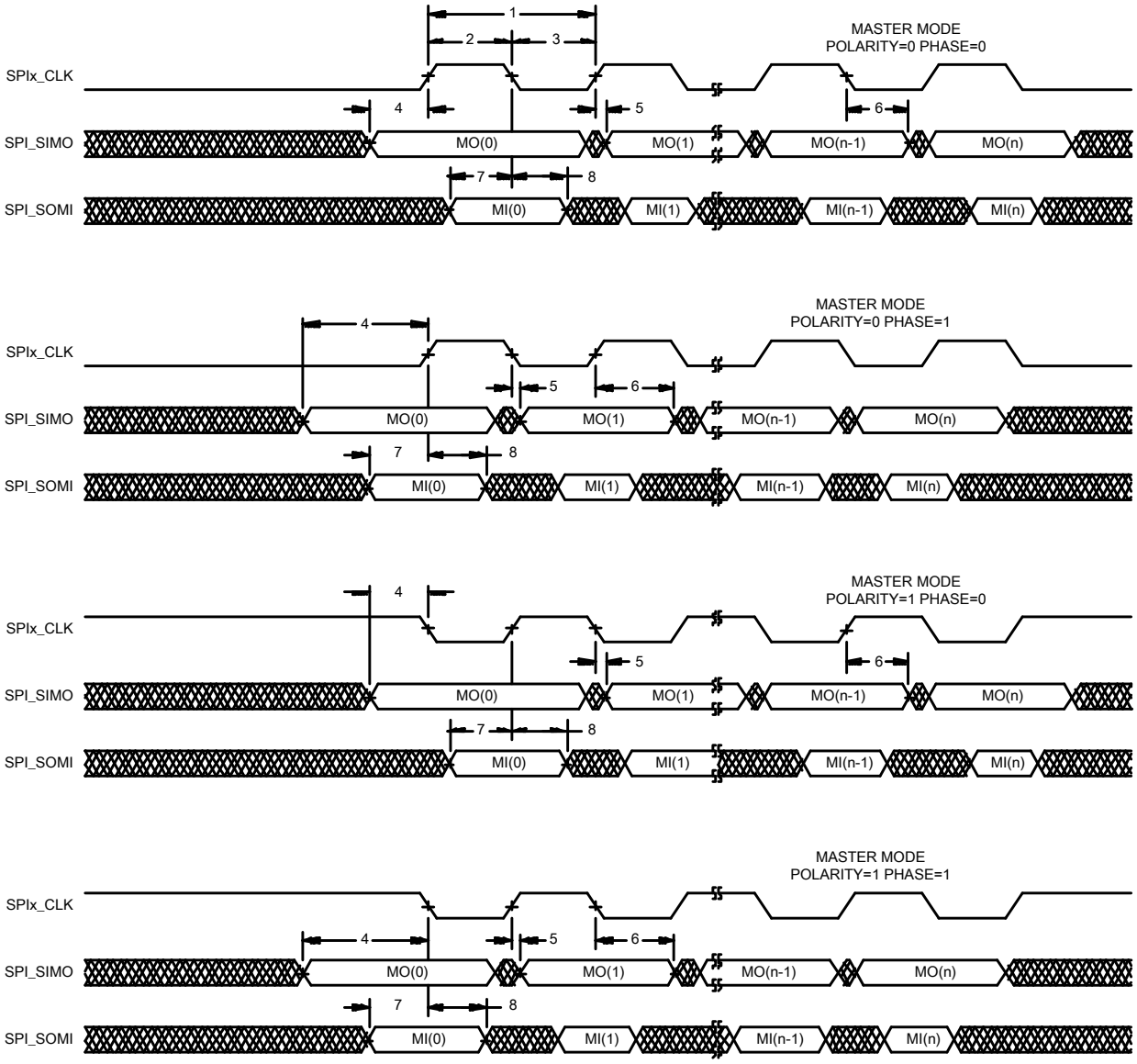


FIGURE 27. SPI timings – Master mode.

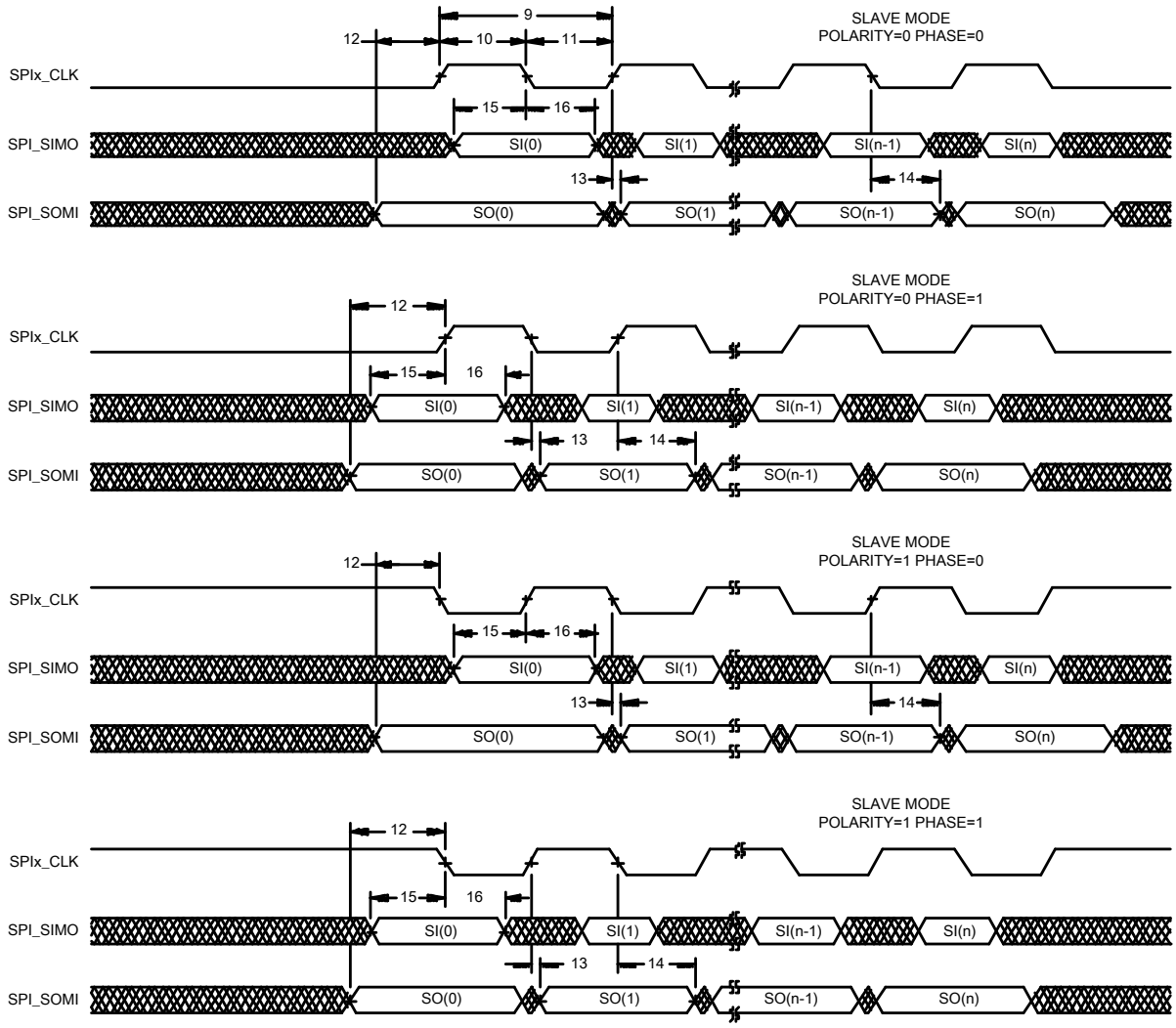
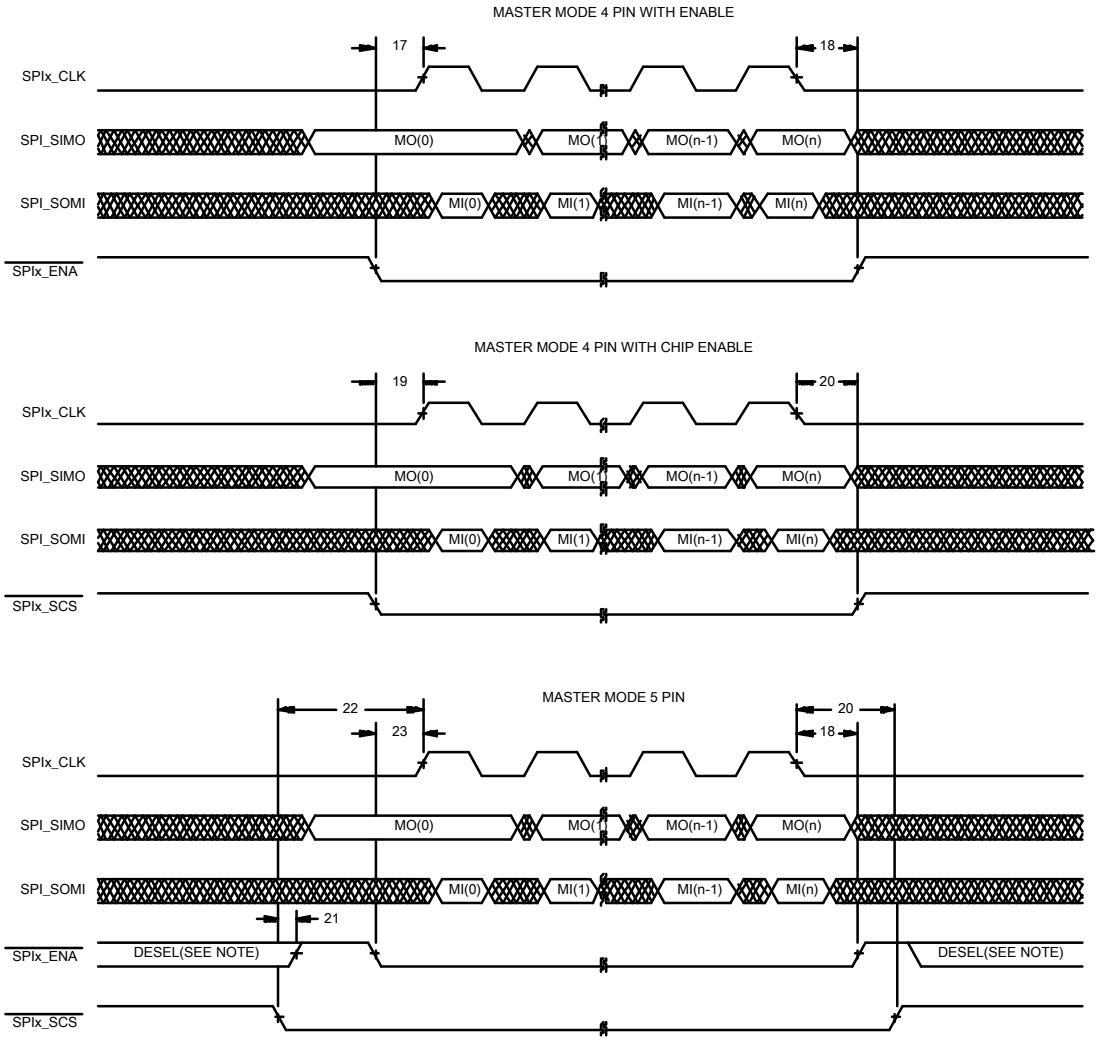


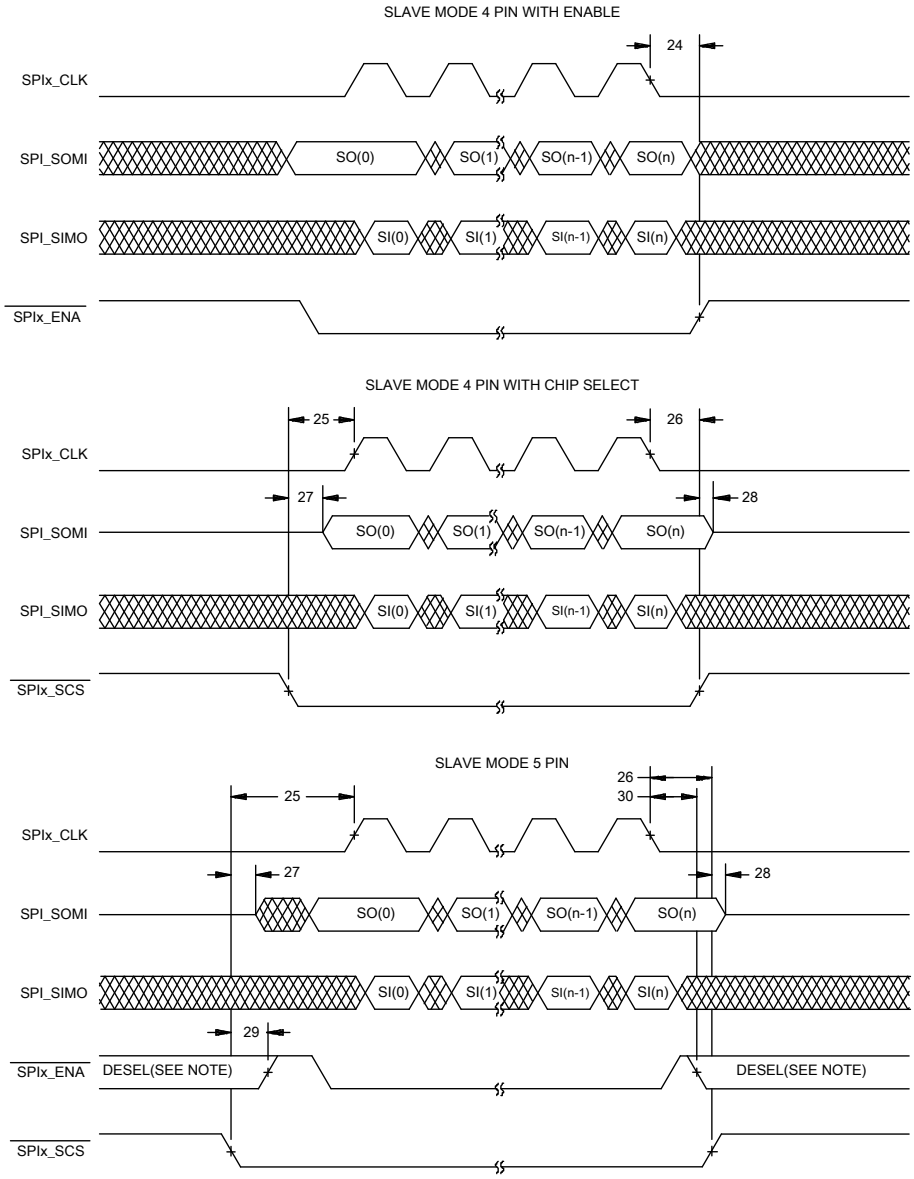
FIGURE 28. SPI timings – Slave mode.



NOTES:

1. Deselected is programmable either high or 3-state (Requires external pullup)

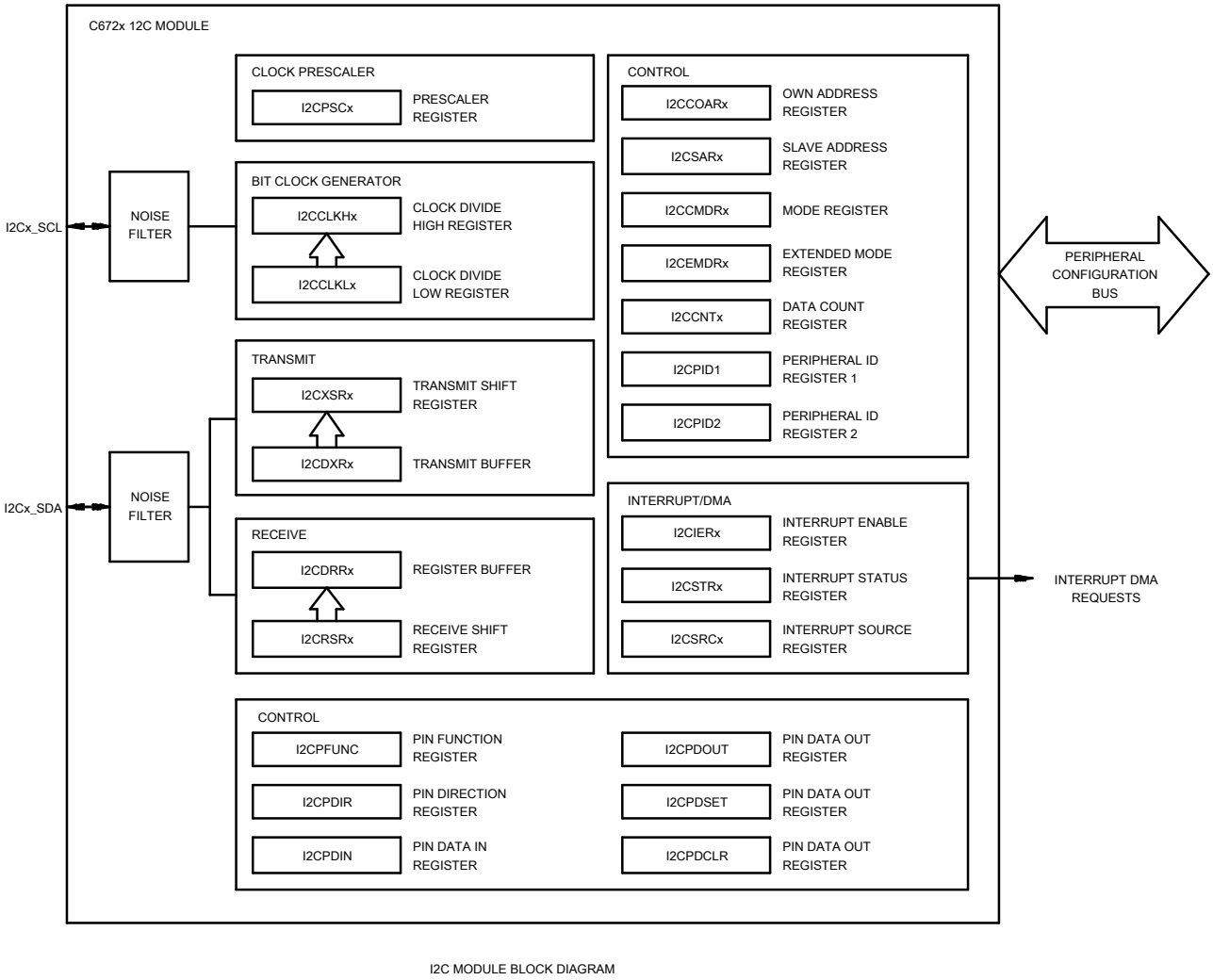
FIGURE 29. SPI timings – Master mode (4-Pin and 5-Pin).



NOTES:

1. Deselected is programmable either high or 3-state (Requires external pullup)

FIGURE 30. SPI timings – Slave mode (4-Pin and 5-Pin).



I2C MODULE BLOCK DIAGRAM

FIGURE 31. I2C module block diagram.

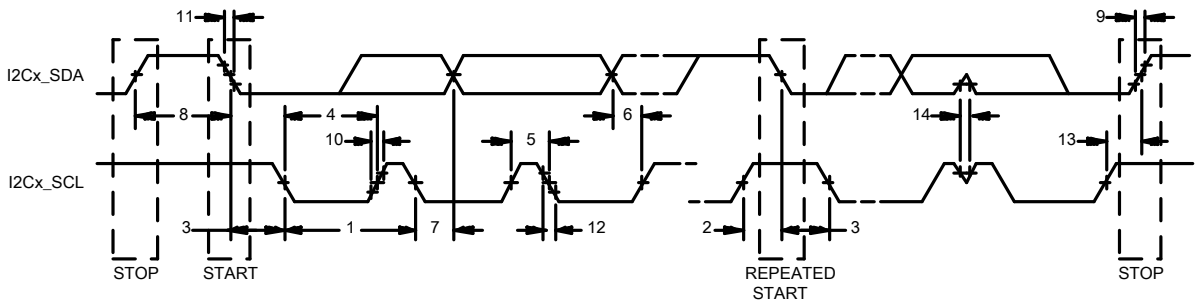


FIGURE 32. I2C receive timings.

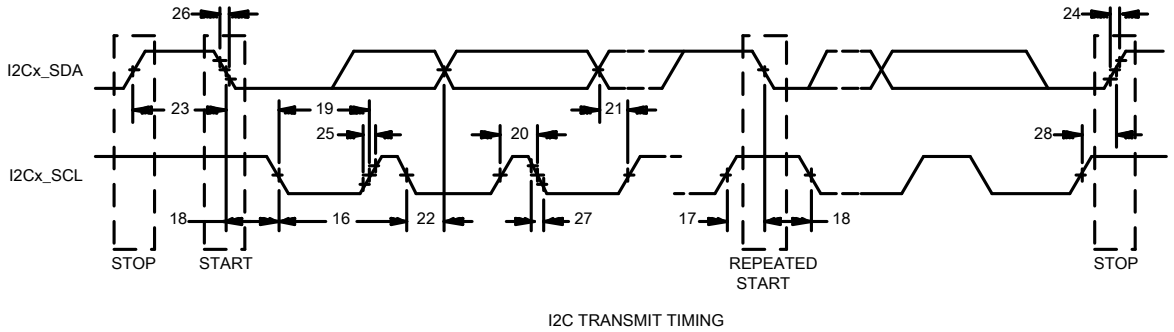


FIGURE 33. I2C transmit timings.

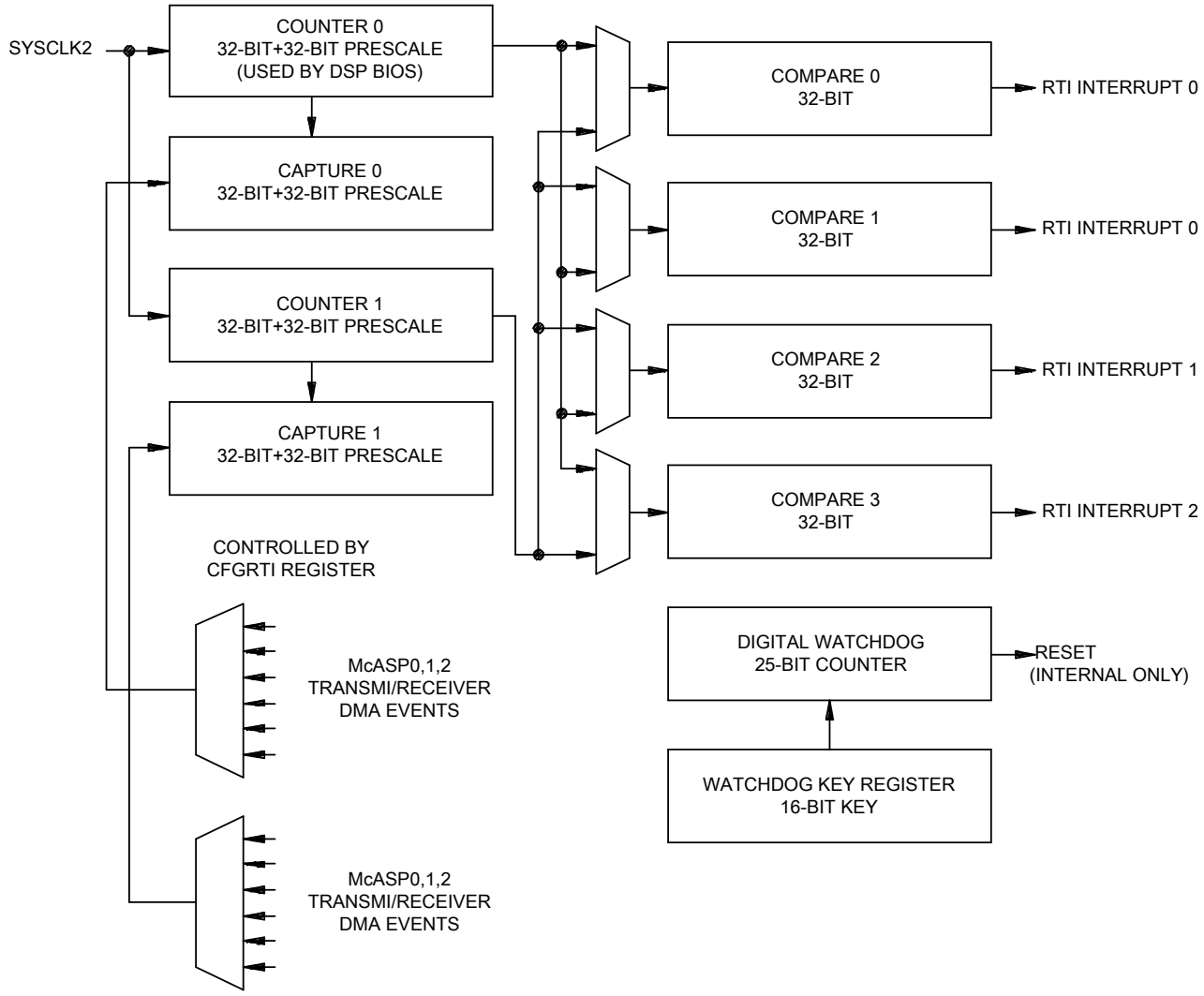


FIGURE 34. RTI timer block diagram.

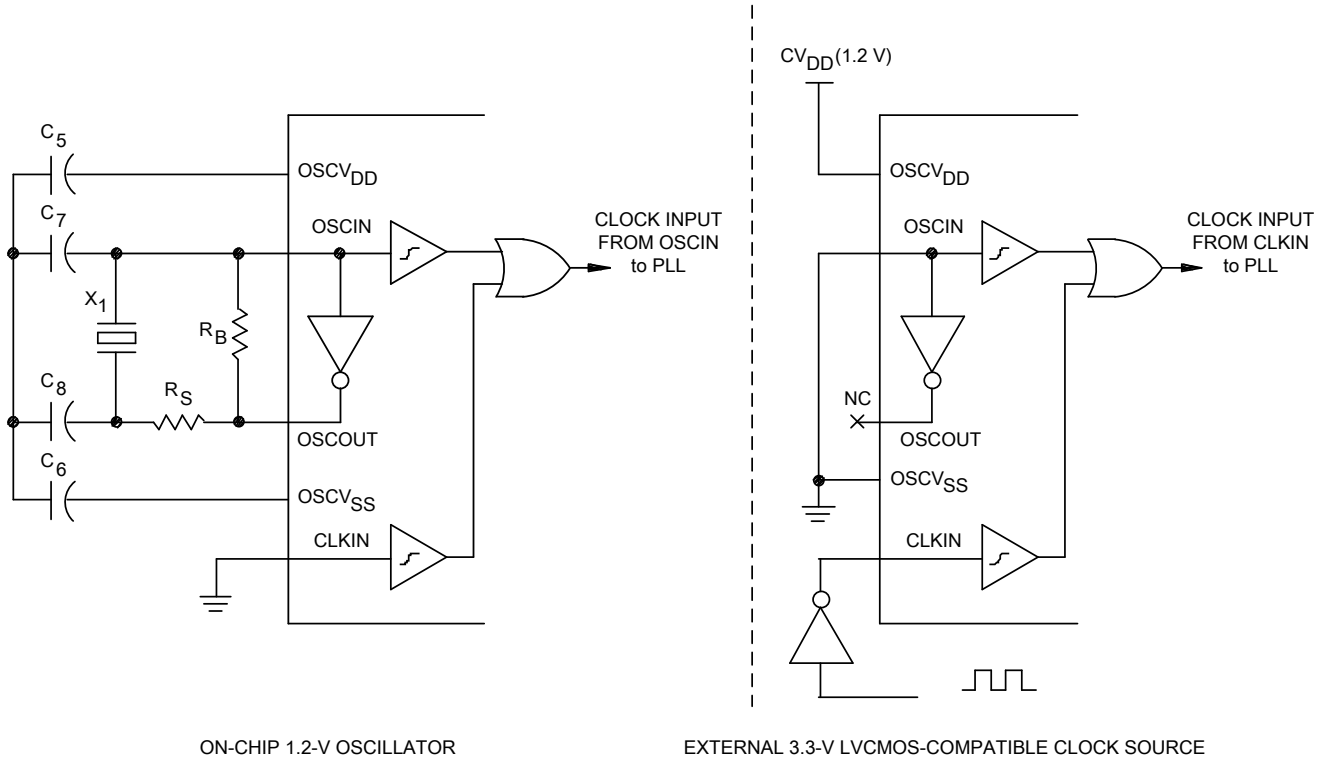


FIGURE 35. Clock input options.

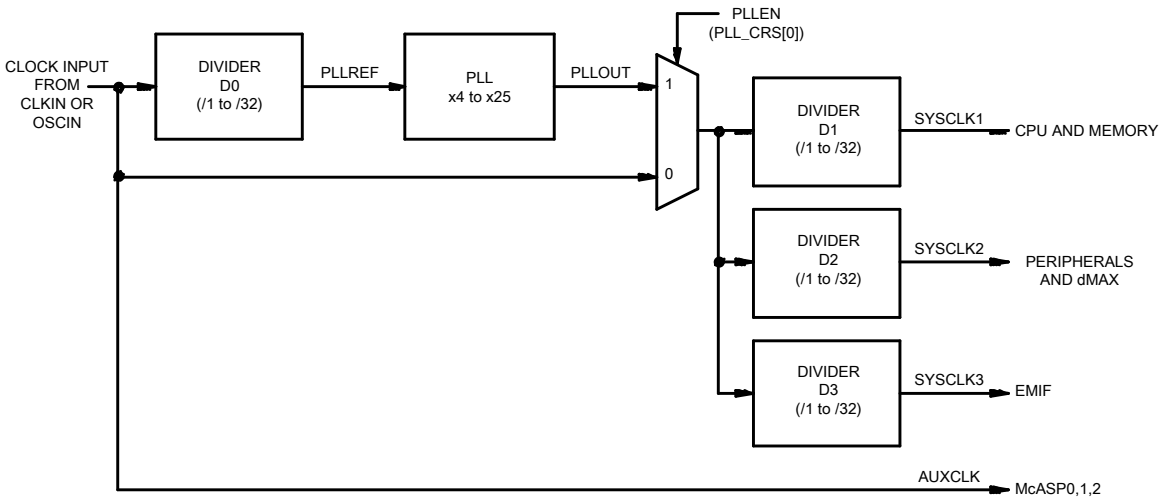


FIGURE 36. PLL topology.

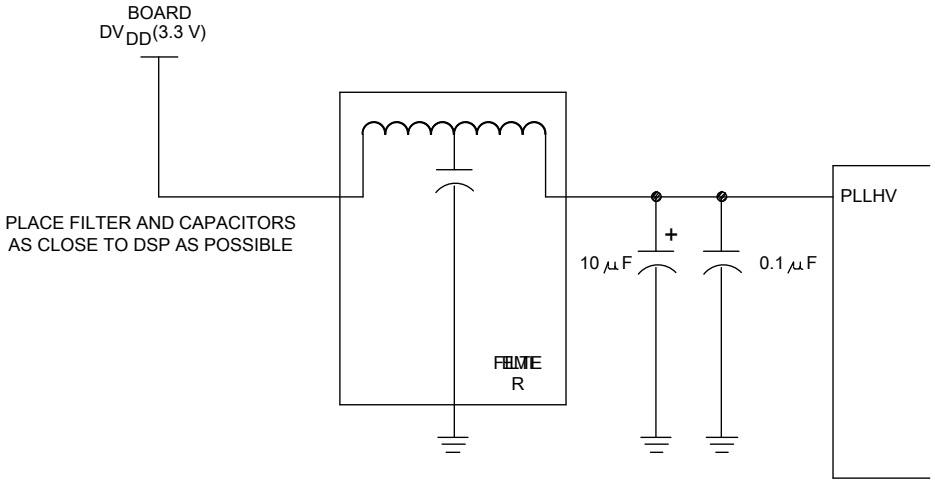


FIGURE 37. PLL power supply filter.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11617-01XE	01295	SM320C6727BGDHMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493