



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/11613</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	MSP430F2013	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	15	JEDEC MO-220	Quad flatpack, No-leads

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Voltage applied at $V_{CC}$ to $V_{SS}$ .....	-0.3 V to +17 V
Voltage apply to any pin .....	-0.3 V to $V_{CC} + 0.3$ V 2/
Diode current at any device terminal .....	$\pm 2$ mA
Storage temperature 3/	
Unprogrammed device .....	-55°C to 150°C
Programmed device .....	-40°C to 150°C
Thermal information 4/	

Case outline letter	X	Units
Junction to ambient thermal resistance( $\theta_{JA}$ ) 5/	38.1	°C/W
Junction to case (top) thermal resistance ( $\theta_{JCTop}$ ) 6/	26	
Junction to board thermal resistance ( $\theta_{JB}$ ) 7/	7.5	
Junction to top characterization parameter ( $\psi_{JT}$ ) 8/	0.3	
Junction to board characterization parameter ( $\psi_{JB}$ ) 9/	5.7	
Junction to case (bottom) thermal resistance ( $\theta_{JCbott}$ ) 10/	1.9	

1.4 Recommended operating conditions.

Supply voltage ( $V_{CC}$ )	
During program execution .....	1.8 V to 3.6 V
During flash program/erase .....	2.2 V to 3.6 V
Supply voltage ( $V_{SS}$ ) .....	0 V
Operating free air temperature (TA) .....	-40°C to 125°C
Processor frequency (maximum MCLK frequency) 11/ 12/	
$V_{CC} = 1.8$ V, Duty cycle = 50% $\pm 10\%$ .....	6 MHz
$V_{CC} = 2.7$ V, Duty cycle = 50% $\pm 10\%$ .....	12 MHz
$V_{CC} = 3.3$ V, Duty cycle = 50% $\pm 10\%$ .....	16 MHz

- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- 2/ All voltage referenced to  $V_{SS}$ . The JTAG fuse blow voltage,  $V_{FB}$  is allow to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- 3/ Higher temperature may be applied during board soldering according to the current JEDEC J-STD 020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
- 4/ For more information about traditional and new thermal metrics, see manufacturer data.
- 5/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC standard, high K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- 6/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- 7/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- 8/ The junction to top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (section 6 and 7).
- 9/ The junction to top characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (section 6 and 7).
- 10/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard exists, but a close description can be found in the ANSI SEMI standard G30-88.
- 11/ This MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- 12/ Modules might have a different maximum input clock specification of the respective module in manufacturer data sheet.

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## 2. APPLICABLE DOCUMENTS

### JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

### 3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional diagram. The functional diagram shall be as shown in figure 3.

3.5.4 Safe operating area. The safe operating area shall be as shown in figure 4.

3.5.5 Operating derate chart. The operating derate chart shall be as shown in figure 5.

3.5.6 Active mode supply current (into V<sub>CC</sub>). The active mode supply current (into V<sub>CC</sub>) shall be as shown in figure 6.

3.5.7 Typical characteristics - Output. The typical characteristics - Output shall be as shown in figure 7.

3.5.8 POR/Brownout Reset (BOR) vs Supply voltage. The POR/Brownout Reset (BOR) vs Supply voltage shall be as shown in figure 8.

3.5.9 Typical characteristics – POR/Brownout reset (BOR). The typical characteristics – POR/Brownout reset (BOR) shall be as shown in figure 9.

3.5.10 Typical characteristics – Calibrated 1 – MHz DCO frequency. The typical characteristics – Calibrated 1 – MHz DCO frequency shall be as shown in figure 10.

3.5.11 Typical characteristics – DCO clock wake up time from LPM3/4. The typical characteristics – DCO clock wake up time from LPM3/4 shall be as shown in figure 11.

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- 3.5.12 Typical characteristics – USI low level output voltage on SDA and SCL. The typical characteristics – USI low level output voltage od SDA and SCL shall be as shown in figure 12.
- 3.5.13 Typical characteristics – SD16 A SINAD performance over OSR. The typical characteristics – SD16 A SINA performance over OSR shall be as shown in figure 13.

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/11613</b></p>
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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>Active Mode Supply Current into V<sub>CC</sub> Excluding External Current</b> 3/ 4/ (See figure 5)							
Active mode (AM) Current (1 MHz)	I <sub>AM, 1MHz</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 1 MHz, f <sub>ACLK</sub> = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		280	μA
				3V		380	
Active mode (AM) Current (1 MHz)	I <sub>AM, 1MHz</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 1 MHz, f <sub>ACLK</sub> = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V	190 TYP		μA
				3 V	265 TYP		
Active mode (AM) Current (4 kHz)	I <sub>AM, 4kHz</sub>	f <sub>MCLK</sub> = f <sub>SMCLK</sub> = f <sub>ACLK</sub> = 32768 Hz/8 = 4096 Hz, f <sub>DCO</sub> = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		3	μA
			125°C	2.2 V		6	
			-40°C to 85°C	3V		4	
			125°C	3 V		7	
Active mode (AM) Current (100 kHz)	I <sub>AM, 100kHz</sub>	f <sub>MCLK</sub> = f <sub>SMCLK</sub> = f <sub>DCO(0, 0)</sub> ≈ = 100 kHz, f <sub>ACLK</sub> = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		50	μA
			125°C	2.2 V		65	
			-40°C to 85°C	3V		55	
			125°C	3 V		70	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>Low Power mode supply Currents (Into V<sub>CC</sub>) Excluding External Current</b> <u>3/</u> <u>4/</u> ( See figure 6 and 7)							
Low power mode 0 (LPM0) current <u>5/</u>	I <sub>LPM0, 1MHz</sub>	f <sub>MCLK</sub> = 0 MHz, f <sub>SMCLK</sub> = f <sub>DCO</sub> = 1 MHz f <sub>ACLK</sub> = 32768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		86	μA
				3 V		108	
Low power mode 0 (LPM0) current <u>5/</u>	I <sub>LPM0, 100kHz</sub>	f <sub>MCLK</sub> = 0 MHz, f <sub>SMCLK</sub> = f <sub>DCO(0, 0)</sub> ≈ 100 kHz f <sub>ACLK</sub> = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 1, SCG1 = 0, OSCOFF = 1		2.2 V		52	μA
				3 V		56	
Low power mode 2 (LPM2) current <u>6/</u>	I <sub>LPM2</sub>	f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz, f <sub>DCO</sub> = 1 MHz f <sub>ACLK</sub> = 32768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		29	μA
			125°C			34	
			-40°C to 85°C	3 V		32	
			125°C			37	
Low power mode 3 (LPM3) current <u>5/</u>	I <sub>LPM3,LFXT1</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz f <sub>ACLK</sub> = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		1.2	μA
			25°C			1	
			85°C			2.3	
			125°C			6.5	
			-40°C	3 V		1.2	
			25°C			1.2	
			85°C			28	
			125°C			7.6	
Low power mode 3 (LPM3) current <u>6/</u>	I <sub>LPM3,VLO</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz f <sub>ACLK</sub> from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.7	μA
			25°C			0.7	
			85°C			1.6	
			125°C			5.5	
			-40°C	3 V		0.9	
			25°C			0.9	
			85°C			1.8	
			125°C			6.5	
Low power mode 3 (LPM4) current <u>7/</u>	I <sub>LPM3,VLO</sub>	f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> = 0 MHz f <sub>ACLK</sub> = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V/3 V		0.5	μA
			25°C			0.5	
			85°C			1.5	
			125°C			4.4	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>Schmitt Trigger Inputs (Ports P1 and P2)</b>						
Positive going input threshold voltage	V <sub>IT+</sub>			0.45 V <sub>CC</sub>	0.75 V <sub>CC</sub>	V
			2.2 V	1.00	1.65	
			3 V	1.35	2.25	
Negative going input threshold voltage	V <sub>IT+</sub>			0.25 V <sub>CC</sub>	0.55 V <sub>CC</sub>	V
			2.2 V	0.55	1.20	
			3 V	0.75	1.65	
Input voltage hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )	V <sub>hys</sub>		2.2 V	0.2	1.0	V
			3 V	0.3	1.0	
Pullup/Pulldown resistor	R <sub>Pull</sub>	For pullup: V <sub>IN</sub> = V <sub>SS</sub> , For pulldown: V <sub>IN</sub> = V <sub>CC</sub>		20	50	kΩ
Input capacitance	C <sub>I</sub>	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>		5 TYP		pF
<b>Inputs (Ports P1 and P2)</b>						
External interrupt timing	t <sub>(int)</sub>	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag <u>8/</u>	2.2 V/3 V	25		ns
<b>Leakage current (Ports P1 and P2)</b>						
High impedance leakage current	I <sub>lkg(Px.y)</sub>	<u>9/</u> <u>10/</u>	2.2 V/3 V		±50	nA
<b>Outputs (Ports P1 and P2)</b> See figure 6 and 7						
High level output voltage	V <sub>OH</sub>	I <sub>(OHmax)</sub> = -1.5 mA <u>11/</u>	2.2 V	V <sub>CC</sub> - 0.25	V <sub>CC</sub>	V
		I <sub>(OHmax)</sub> = -6 mA <u>12/</u>	2.2 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub>	
		I <sub>(OHmax)</sub> = -1.5 mA <u>11/</u>	3 V	V <sub>CC</sub> - 0.25	V <sub>CC</sub>	
		I <sub>(OHmax)</sub> = -6 mA <u>12/</u>	3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub>	
Low level output voltage	V <sub>OL</sub>	I <sub>(OLmax)</sub> = 1.5 mA <u>11/</u>	2.2 V	V <sub>SS</sub>	V <sub>SS</sub> + 0.25	V
		I <sub>(OLmax)</sub> = 6 mA <u>12/</u>	2.2 V	V <sub>SS</sub>	V <sub>SS</sub> + 0.6	
		I <sub>(OLmax)</sub> = 1.5 mA <u>11/</u>	3 V	V <sub>SS</sub>	V <sub>SS</sub> + 0.25	
		I <sub>(OLmax)</sub> = 6 mA <u>12/</u>	3 V	V <sub>SS</sub>	V <sub>SS</sub> + 0.6	
<b>Output frequency (Ports P1 and P2)</b>						
Port output frequency (with load)	f <sub>Px.y</sub>	P1.4/SMCLK, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ <u>13/</u> <u>14/</u>	2.2 V		10	MHz
			3 V		12	
Clock output frequency	f <sub>Port+CLK</sub>	P2.0/ACLK, P1.4/SMCLK, C <sub>L</sub> = 20 pF <u>14/</u>	2.2 V		12	MHz
			3 V		16	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>POR/Brownout Reset (BOR) <u>15/</u></b>						
See figure 8	V <sub>CC(start)</sub>	dV <sub>CC</sub> /dt ≤ 3 V/s		0.7 x V <sub>(B_IT-)</sub> TYP		V
See figure 8 to 10	V <sub>(B_IT-)</sub>	dV <sub>CC</sub> /dt ≤ 3 V/s			1.71	V
See figure 8	V <sub>hys(B_IT-)</sub>	dV <sub>CC</sub> /dt ≤ 3 V/s		70	210	mV
See figure 8	t <sub>d(BOR)</sub>					μs
Pulse length needed at $\overline{\text{RST}}$ /NMI pin to accepted reset internally <u>16/</u>						
<b>DCO frequency</b>						
Supply voltage	V <sub>CC</sub>	RSELx < 14		1.8	3.6	V
		RSELx = 14		2.2	3.6	
		RSELx = 15		3.0	3.6	
DCO frequency (0, 0)	f <sub>DCO(0,0)</sub>	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06	0.14	MHz
DCO frequency (0, 3)	f <sub>DCO(0,3)</sub>	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07	0.17	
DCO frequency (1, 3)	f <sub>DCO(1,3)</sub>	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10	0.20	
DCO frequency (2, 3)	f <sub>DCO(2,3)</sub>	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14	0.28	
DCO frequency (3, 3)	f <sub>DCO(3,3)</sub>	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20	0.40	
DCO frequency (4, 3)	f <sub>DCO(4,3)</sub>	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28	0.54	
DCO frequency (5, 3)	f <sub>DCO(5,3)</sub>	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39	0.77	
DCO frequency (6, 3)	f <sub>DCO(6,3)</sub>	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54	1.06	
DCO frequency (7, 3)	f <sub>DCO(7,3)</sub>	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80	1.50	
DCO frequency (8, 3)	f <sub>DCO(8,3)</sub>	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10	2.10	
DCO frequency (9, 3)	f <sub>DCO(9,3)</sub>	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.6	3.00	
DCO frequency (10, 3)	f <sub>DCO(10,3)</sub>	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50	4.30	
DCO frequency (11, 3)	f <sub>DCO(11,3)</sub>	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00	5.50	
DCO frequency (12, 3)	f <sub>DCO(12,3)</sub>	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30	7.30	
DCO frequency (13, 3)	f <sub>DCO(13,3)</sub>	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00	9.60	
DCO frequency (14, 3)	f <sub>DCO(14,3)</sub>	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60	13.9	
DCO frequency (15, 3)	f <sub>DCO(15,3)</sub>	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0	18.5	
DCO frequency (15, 7)	f <sub>DCO(15,7)</sub>	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0	26.0	
Frequency step between range RSEL and RSEL + 1	S <sub>RSEL</sub>	S <sub>RSEL</sub> = f <sub>DCO(RSEL = 1, DCO)/f<sub>DCO(RSEL, DCO)</sub></sub>	2.2 V/3 V		1.55	ratio
Frequency step between tap DCO and DCO + 1	S <sub>DCO</sub>	S <sub>DCO</sub> = f <sub>DCO(RSE, DCO + 1)/f<sub>DCO(RSEL, DCO)</sub></sub>	2.2 V/3 V	1.03	1.14	
Duty sysle		Measured at P1.4/SMCLK	2.2 V/3 V	40	60	%

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>Calibrated DCO frequencies – Tolerance at Calibration</b>							
Frequency tolerance at calibration			25°C	3 V	-1	+1	%
1-MHz calibration value	f <sub>CAL(1MHz)</sub>	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gaiting time: 5 ms	25°C	3 V			MHz
8-MHz calibration value	f <sub>CAL(8MHz)</sub>	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gaiting time: 5 ms	25°C	3 V			MHz
12-MHz calibration value	f <sub>CAL(12MHz)</sub>	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gaiting time: 5 ms	25°C	3 V			MHz
16-MHz calibration value	f <sub>CAL(16MHz)</sub>	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gaiting time: 2 ms	25°C	3 V			MHz
<b>Calibrated DCO frequencies – Tolerance over temperature -40°C to 125°C</b>							
1 MHz tolerance over temperature			-40°C to 125°C	3V	-2.5	+2.5	%
8 MHz tolerance over temperature			-40°C to 125°C	3V	-2.5	+2.5	%
12 MHz tolerance over temperature			-40°C to 125°C	3V	-2.5	+2.5	%
16 MHz tolerance over temperature			-40°C to 125°C	3V	-3	+3	%
1-MHz calibration value	f <sub>CAL(1MHz)</sub>	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gaiting time: 5 ms	-40°C to 125°C	2.2 V	0.97	1.03	MHz
				3 V	0.975	1.025	
				3.6 V	0.97	1.03	
8-MHz calibration value	f <sub>CAL(8MHz)</sub>	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gaiting time: 5 ms	-40°C to 125°C	2.2 V	7.6	8.4	
				3 V	7.6	8.4	
				3.6 V	7.6	8.4	
12-MHz calibration value	f <sub>CAL(12MHz)</sub>	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gaiting time: 5 ms	-40°C to 125°C	2.2 V	11.6	12.3	
				3 V	11.6	12.3	
				3.6 V	11.6	12.3	
16-MHz calibration value	f <sub>CAL(16MHz)</sub>	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gaiting time: 2 ms	-40°C to 125°C	3 V	15	16.48	
				3.6 V	15	16.48	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>Calibrated DCO frequencies – Tolerance over supply voltage V<sub>CC</sub></b>							
1 MHz tolerance over temperature			25°C	1.8 V to 3.6 V	-3	+3	%
8 MHz tolerance over temperature			25°C	1.8 V to 3.6 V	-3	+3	%
12 MHz tolerance over temperature			25°C	2.2 V to 3.6 V	-3	+3	%
16 MHz tolerance over temperature			25°C	3 V to 3.6 V	-6	+3	%
1-MHz calibration value	f <sub>CAL(1MHz)</sub>	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gaiting time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1.03	MHz
8-MHz calibration value	f <sub>CAL(8MHz)</sub>	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gaiting time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8.24	
12-MHz calibration value	f <sub>CAL(12MHz)</sub>	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gaiting time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12.36	
16-MHz calibration value	f <sub>CAL(16MHz)</sub>	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gaiting time: 2 ms	25°C	3 V to 3.6 V	15	16.48	
<b>Calibrated DCO frequencies – Overall Tolerance</b>							
1 MHz tolerance over temperature				1.8 V to 3.6 V	-6	+6	%
8 MHz tolerance over temperature				1.8 V to 3.6 V	-6	+6	%
12 MHz tolerance over temperature				2.2 V to 3.6 V	-6	+6	%
16 MHz tolerance over temperature				3 V to 3.6 V	-6	+6	%
1-MHz calibration value	f <sub>CAL(1MHz)</sub>	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gaiting time: 5 ms		1.8 V to 3.6 V	0.95	1.05	MHz
8-MHz calibration value	f <sub>CAL(8MHz)</sub>	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gaiting time: 5 ms		1.8 V to 3.6 V	7.6	8.4	
12-MHz calibration value	f <sub>CAL(12MHz)</sub>	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gaiting time: 5 ms		2.2 V to 3.6 V	11.4	12.6	
16-MHz calibration value	f <sub>CAL(16MHz)</sub>	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gaiting time: 2 ms		3 V to 3.6 V	15	17	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>Wake up from lower Power Modes (LPM3/4)</b> <u>17/</u> See figure 12							
DCO clock wake up time from LPM3/4 <u>18/</u>	t <sub>DCO,LPM3/4</sub>	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz,	105°C	2.2 V/3 V		2	μs
		BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz,				1.5	
		BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz,				1	
		BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz,				1	
CPU wake up time from LPM3/4	t <sub>CPU,LPM3/4</sub>				1/ f <sub>MCLK</sub> + t <sub>clock, LPM3/4</sub>		
<b>Crystal oscillator, XT1, Low frequency Mode</b> <u>20/ 21/</u>							
LFXT1 oscillator crystal frequency, LF mode 0, 1	f <sub>LFXT1,LF</sub>	XTS = 0, LFXT1Sx = 0 or 1	105°C	1.8 V to 3.6 V	32768 TYP		Hz
LFXT1 oscillator logic level square wave input frequency, LF mode	f <sub>LFXT1,LF, logic</sub>	XTS = 0, LFXT1Sx = 3		1.8 V to 3.6 V	10	50	KHz
Oscillation allowance for LF crystals	OA <sub>LF</sub>	XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF			500 TYP		kΩ
		XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF			200 TYP		
Integrated effective load Capacitance, LF mode <u>22/</u>		XTS = 0, XCAPx = 0			1 TYP		pF
		XTS = 0, XCAPx = 1			5.5 TYP		
		XTS = 0, XCAPx = 2			8.5 TYP		
		XTS = 0, XCAPx = 3		11 TYP			
Duty cycle, LF mode		XTS = 0, Measured at P1.0/ACLK f <sub>LFXT1,LF</sub> = 32768 Hz		2V/3 V	30	70	%
Oscillator fault frequency, LF mode <u>23/</u>		XTS = 0, LFXT1Sx = 3 <u>24/</u>		2V/3 V	10	10000	Hz
<b>Internal Very low Power Low Frequency Osillator (VLO)</b>							
VLO frequency	f <sub>VLO</sub>		-40°C to 85°C	2.2 V/3 V	4	20	kHz
			125°C			22	
VLO frequency temperature drift <u>25/</u>	df <sub>VLO</sub> /dT		-40°C to 85°C	2.2 V/3 V	0.68 TYP		%/°C
VLO frequency supply voltage drift <u>26/</u>	df <sub>VLO</sub> /dV <sub>CC</sub>		125°C	1.8 V to 3.6 V	4 TYP		%/V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit	
					Min	Max		
<b>Timer_A</b>								
Timer_A clock frequency	f <sub>TA</sub>	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ±10%	105°C	2.2 V		10	MHz	
				3 V		16		
Timer_A capture timing <u>17/</u>	f <sub>TA,cap</sub>	TA0, TA1		2.2 V/3 V	20		ns	
<b>USI, Universal Serial Interface</b> <u>17/</u> See figure 13								
USI clock frequency	f <sub>USI</sub>	External: SCLK, Duty cycle = 50% ±10% SPI slave mode	105°C	2.2 V		10	MHz	
				3 V		16		
Low level output voltage on SDA and SCL	V <sub>OL,I2C</sub>	USI module in I2C mode, I <sub>OL,max</sub> = 1.5 mA		2.2 V/3 V	V <sub>SS</sub>	V <sub>SS</sub> + 0.4	V	
<b>SD16_A, Power Supply and Recommended Operating conditions</b> <u>17/</u>								
Analog supply voltage range	AV <sub>CC</sub>	AV <sub>CC</sub> = DV <sub>CC</sub> = V <sub>CC</sub> , AV <sub>SS</sub> = DV <sub>SS</sub> = V <sub>SS</sub> = 0 V			2.5	3.6	V	
Analog supply current including Internal reference	I <sub>SD16</sub>	SD16LP = 0, f <sub>SD16</sub> = 1 MHz, SED16OSR = 256	Gain: 1, 2	-40°C to 85°C	3 V		1050	µA
				105°C			1170	
			Gain: 4, 8, 16	-40°C to 85°C			1150	
				105°C			1300	
			Gain: 32	-40°C to 85°C			1700	
				105°C			1850	
		SD16LP = 1, f <sub>SD16</sub> = 1 MHz, SED16OSR = 256	Gain: 1	-40°C to 85°C			1030	
				105°C			1160	
			Gain: 32	-40°C to 85°C			1150	
				105°C			1300	
SD16 input clock frequency	f <sub>SD16</sub>	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1.1	MHz	
		SD16LP = 1 (Low power mode enabled)			0.03			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u> $T_A = 105^\circ\text{C}$	$V_{CC}$	Limits		Unit	
				Min	Max		
<b>SD16_A, Input Range</b> <u>17/</u>							
Differential full scale input voltage range <u>27/</u>	$V_{ID,FSR}$	Bipolar mode, SD16UNI = 0		$-(V_{REF}/2)/\text{GAIN}$	$+(V_{REF}/2)/\text{GAIN}$	mV	
		Unipolar mode, SD16UNI = 1		0	$+(V_{REF}/2)/\text{GAIN}$		
Differential input voltage range for specified performance <u>27/</u>	$V_{ID}$	SD16REFON = 1	SD16GAINx = 1	±500 TYP		mV	
			SD16GAINx = 2	±250 TYP			
			SD16GAINx = 4	±125 TYP			
			SD16GAINx = 8	±62 TYP			
			SD16GAINx = 16	±31 TYP			
			SD16GAINx = 32	±15 TYP			
Input impedance (one input pin to $AV_{SS}$ )	$Z_I$		SD16GAINx = 1	3 V	200 TYP		kΩ
			SD16GAINx = 32		75 TYP		
Differential input impedance (IN+ to IN-)	$Z_{ID}$		SD16GAINx = 1	3 V	300		kΩ
			SD16GAINx = 32		100		
Absolute input voltage range	$V_I$				$AV_{SS} - 0.1$	$AV_{CC}$	V
Common-mode input voltage range	$V_{IC}$				$AV_{SS} - 0.1$	$AV_{CC}$	V
<b>SD16_A, SINAD Performance (fSD16 = 1 MHz, SD16OSRx = 1024, SD16REFON = 1)</b> <u>17/</u>							
Signal to noise + distortion ratio (OSR = 1024)	SINAD <sub>1024</sub>	SD16GAINx = 1, Signal amplitude: $V_{IN} = 500$ mV, Signal frequency: $f_{IN} = 100$ Hz		3 V	86	87	dB
		SD16GAINx = 2, Signal amplitude: $V_{IN} = 250$ mV, Signal frequency: $f_{IN} = 100$ Hz			82	83	
		SD16GAINx = 4, Signal amplitude: $V_{IN} = 125$ mV, Signal frequency: $f_{IN} = 100$ Hz			78	79	
		SD16GAINx = 8, Signal amplitude: $V_{IN} = 62$ mV, Signal frequency: $f_{IN} = 100$ Hz			73	74	
		SD16GAINx = 16, Signal amplitude: $V_{IN} = 31$ mV, Signal frequency: $f_{IN} = 100$ Hz			68	69	
		SD16GAINx = 32, Signal amplitude: $V_{IN} = 15$ mV, Signal frequency: $f_{IN} = 100$ Hz			62	63	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u> $T_A = 105^\circ\text{C}$	$V_{CC}$	Limits		Unit
				Min	Max	
<b>SD16_A, SINAD Performance (fSD16 = 1 MHz, SD16OSRx = 526, SD16REFON = 1) <u>17/</u></b>						
Signal to noise + distortion ratio (OSR = 256)	SINAD <sub>256</sub>	SD16GAINx = 1, Signal amplitude: $V_{IN} = 500\text{ mV}$ , Signal frequency: $f_{IN} = 100\text{ Hz}$	3 V	82	83	dB
		SD16GAINx = 2, Signal amplitude: $V_{IN} = 250\text{ mV}$ , Signal frequency: $f_{IN} = 100\text{ Hz}$		76	77	
		SD16GAINx = 4, Signal amplitude: $V_{IN} = 125\text{ mV}$ , Signal frequency: $f_{IN} = 100\text{ Hz}$		71	72	
		SD16GAINx = 8, Signal amplitude: $V_{IN} = 62\text{ mV}$ , Signal frequency: $f_{IN} = 100\text{ Hz}$		67	68	
		SD16GAINx = 16, Signal amplitude: $V_{IN} = 31\text{ mV}$ , Signal frequency: $f_{IN} = 100\text{ Hz}$		63	64	
		SD16GAINx = 32, Signal amplitude: $V_{IN} = 15\text{ mV}$ , Signal frequency: $f_{IN} = 100\text{ Hz}$		57	58	
<b>SD16_A, SINAD Performance (fSD16 = 1 MHz, SD16OSRx = 256, SD16REFON = 1) <u>17/</u></b>						
Nominal gain	G	SD16GAINx = 1	3 V	0.97	1.02	
		SD16GAINx = 2		1.90	2.02	
		SD16GAINx = 4		3.76	3.96	
		SD16GAINx = 8		7.36	7.84	
		SD16GAINx = 16		14.56	15.52	
		SD16GAINx = 32		27.20	29.76	
Gain temperature drift	$\Delta G/\Delta t$	SD16GAINx = 1 <u>28/</u>	3 V	15 TYP		ppm/ $^\circ\text{C}$
Offset error	$E_{OS}$	SD16GAINx = 1	3 V		$\pm 0.2$	%FSR
		SD16GAINx = 32			$\pm 1.5$	
Offset error temperature coefficient	$\Delta E_{OS}/\Delta t$	SD16GAINx = 1	3 V		$\pm 20$	ppm FSR/ $^\circ\text{C}$
		SD16GAINx = 32			$\pm 100$	
Common mode rejection ratio	CMRR	SD16GAINx = 1, Common mode input signal: $V_{ID} = 500\text{ mV}$ , $f_{IN} = 50\text{ Hz}$ , $100\text{ Hz}$	3 V	> 90 TYP		dB
		SD16GAINx = 32, Common mode input signal: $V_{ID} = 16\text{ mV}$ , $f_{IN} = 50\text{ Hz}$ , $100\text{ Hz}$		> 75 TYP		
DC power supply rejection	DC PSR	SD16GAINx = 1, $V_{IN} = 500\text{ mV}$ , $V_{CC} = 2.5\text{ V}$ to $3.6$ <u>29/</u>	2.5 V to 3.6 V	0.35 TYP		%/V
AC power supply rejection ratio	AC PSRR	SD16GAINx = 1, $V_{CC} = 3\text{ V} \pm 10\text{ mV}$ , $f_{IN} = 50\text{ Hz}$	3 V	> 80 TYP		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	T <sub>A</sub>	V <sub>CC</sub>	Limits		Unit
					Min	Max	
<b>SD16_A Built in Voltage Reference</b> 17/							
Internal reference voltage	V <sub>REF</sub>	SD16REFON = 1 SD16VMIDON = 0	105°C	3 V	1.14	1.26	V
Reference supply current	I <sub>REF</sub>	SD16REFON = 1 SD16VMIDON = 0	-40°C to 85°C	3 V		280	μA
			105°C			295	
Temperature coefficient	TC	SD16REFON = 1 SD16VMIDON = 0	105°C	3 V		50	ppm/°C
V <sub>REF</sub> load capacitance	C <sub>REF</sub>	SD16REFON = 1 SD16VMIDON = 0 30/	105°C	3 V	100 TYP		nF
V <sub>REF(I)</sub> maximum load current	I <sub>LOAD</sub>	SD16REFON = 1 SD16VMIDON = 0	105°C	3 V		±200	nA
Turn on time	t <sub>ON</sub>	SD16REFON = 0 → 1 SD16VMIDON = 0, C <sub>REF</sub> = 100 nF	105°C	3 V	5 TYP		ms
DC power supply rejection ΔV <sub>REF</sub> /ΔV <sub>CC</sub>	DC PSR	SD16REFON = 1 SD16VMIDON = 0 V <sub>CC</sub> = 2.5 V to 3.6 V	105°C	2.5 V to 3.6 V	100 TYP		μV/V
<b>SD16_A Reference output Buffer</b> 17/							
Reference buffer output voltage	V <sub>REF,BUF</sub>	SD16REFON = 1 SD16VMIDON = 1	105°C	3 V	1.2 TYP		V
Reference supply + reference Output buffer quiescent current	I <sub>REF,BUF</sub>	SD16REFON = 1 SD16VMIDON = 1	-40°C to 85°C	3 V		600	μA
			105°C			600	
Required load capacitance on V <sub>REF</sub>	C <sub>REF(O)</sub>	SD16REFON = 1 SD16VMIDON = 1	105°C	3 V	470		nF
Maximum load current on V <sub>REF</sub>	I <sub>LOAD,Max</sub>	SD16REFON = 1 SD16VMIDON = 1	105°C	3 V		±1	mA
Maximum voltage variation vs Load current		I <sub>LOAD</sub>   = 0 to 1 mA	105°C	3 V	-15	+15	mV
Turn on time	t <sub>ON</sub>	SD16REFON = 0 → 1 SD16VMIDON = 1, C <sub>REF</sub> = 470 nF	105°C	3 V	100 TYP		μs
<b>SD16_A, External Reference Input</b> 17/							
Input voltage range	V <sub>REF(I)</sub>	SD16REFON = 0	105°C	3 V	1	1.5	V
Input current	I <sub>REF(I)</sub>	SD16REFON = 0	105°C	3 V		50	nA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u> $T_A = 105^\circ\text{C}$	$V_{CC}$	Limits		Unit
				Min	Max	
<b>SD16_A, Temperature sensor</b> <u>17/</u> <u>31/</u>						
Sensor temperature coefficient	$TC_{\text{Sensor}}$			1.18	1.46	mV/ $^\circ\text{C}$
Sensor offset voltage	$V_{\text{Offset, Sensor}}$			-100	100	mV
Sensor output voltage <u>32/</u>	$V_{\text{Sensor}}$	Temperature sensor voltage at $T_A = 85^\circ\text{C}$	3 V	435	515	mV
		Temperature sensor voltage at $T_A = 25^\circ\text{C}$		355	435	
		Temperature sensor voltage at $T_A = 0^\circ\text{C}$		320	400	
<b>Flash Memory</b> <u>17/</u> <u>33/</u>						
Program and erase supply voltage	$V_{CC(\text{PGM/ERASE})}$			2.2	3.6	V
Flash timing generator frequency	$f_{\text{FTG}}$			2.57	476	kHz
Supply current from $V_{CC}$ during program	$I_{\text{PGM}}$		2.2 V/3.6 V		5	mA
Supply current from $V_{CC}$ during erase	$I_{\text{ERASE}}$		2.2 V/3.6 V		7	mA
Cumulative program time <u>34/</u>	$t_{\text{CPT}}$		2.2 V/3.6 V		10	ms
Cumulative mass erase time	$t_{\text{CMERASE}}$		2.2 V/3.6 V	20		ms
Program/Erase endurance		$-40^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$		$10^4$		cycles
Data retention duration	$t_{\text{retention}}$	$T_J = 25^\circ\text{C}$		100		years
Word or byte program time	$t_{\text{Word}}$	See <u>35/</u>		30 TYP		$t_{\text{FTG}}$
Block program time for first byte or word	$t_{\text{Block, 0}}$	See <u>35/</u>		25 TYP		
Block program time for each additional byte or word	$t_{\text{Block, 1-63}}$	See <u>35/</u>		18 TYP		
Block program end sequence wait time	$t_{\text{Block, End}}$	See <u>35/</u>		6 TYP		
Mass erase time	$t_{\text{Mass, Erase}}$	See <u>35/</u>		10593 TYP		
Segment erase time	$t_{\text{Seg, Erase}}$	See <u>35/</u>		4819 TYP		
<b>RAM</b> <u>17/</u>						
RAM retention supply voltage <u>36/</u>	$V_{(\text{RAMh})}$	CPU halted		1.6		V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	V <sub>CC</sub>	Limits		Unit
				Min	Max	
<b>JTAG and Spy-Bi-Wire interface</b>						
Spy-Bi-Wire input frequency	f <sub>SBW</sub>		2.2 V/3 V	0	20	MHz
Spy-Bi-Wire low clock pulse length <u>17/</u>	t <sub>SBW,Low</sub>		2.2 V/3 V	0.025	15	μs
Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge <u>37/</u> )	f <sub>SBW,En</sub>		2.2 V/3 V		1	μs
Spy-Bi-Wire return to normal operation time	f <sub>SBW,Ret</sub>		2.2 V/3 V	15	100	μs
TCK input frequency <u>38/</u>	f <sub>TCK</sub>		2.2 V	0	5	MHz
			3 V	0	10	
Internal pulldown resistance on TEST	R <sub>Internal</sub>		2.2 V/3 V	25	90	kΩ
<b>JTAG Fuse <u>39/</u></b>						
Supply voltage during fuse blow condition	V <sub>CC(FB)</sub>	T <sub>A</sub> = 25°C		2.5		V
Voltage level on TEST for fuse blow	V <sub>FB</sub>			6	7	V
Supply current into TEST during fuse blow	I <sub>FB</sub>				100	mA
Time to blow fuse	t <sub>FB</sub>				1	ms

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).
- 3/ All inputs tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.
- 4/ External crystal not used. The currents are characterized with a clock derived from alternate external clock source.
- 5/ Current for brownout and WDT clocked by SMCLK included.
- 6/ Current for brownout and WDT clocked by ACLK included.
- 7/ Current for brownout included.
- 8/ An external signal sets the interrupt flag every time the minimum interrupt pulse width  $t_{(int)}$  is met. It may be set even with trigger signals shorter than  $t_{(int)}$ .
- 9/ The leakage current is measured with VSS or VCC to the corresponding pin(s), unless otherwise noted.
- 10/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
- 11/ The maximum total current,  $I_{(OHmax)}$  and  $I_{(OLmax)}$ , for all outputs combined should not exceed  $\pm 12$  mA to hold the maximum voltage drop specified.
- 12/ The maximum total current,  $I_{(OHmax)}$  and  $I_{(OLmax)}$ , for all outputs combined should not exceed  $\pm 48$  mA to hold the maximum voltage drop specified.
- 13/ A resistive divider with  $2 \times 0.5$  k $\Omega$  between  $V_{CC}$  and  $V_{SS}$  is used as load. The output is connected to the center tap of the divider.
- 14/ The output voltage reaches at least 10% and 90%  $V_{CC}$  at the specified toggle frequency.
- 15/ The current consumption of the brownout module is already included in the ICC current consumption data. The voltage level  $V_{(B\_IT-)} + V_{hys(B\_IT-)}$  is  $\leq 1.8$  V.
- 16/ Minimum and maximum parameters are characterized up to  $T_A = 105^\circ\text{C}$  unless otherwise noted.
- 17/ Parameters are characterized up to  $T_A = 105^\circ\text{C}$  unless otherwise noted.
- 18/ The DCO clock wake up time is measured from the edge of an external wake up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK)
- 19/ Parameter applicable only if DCLOCK is used for MCLK.
- 20/ To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - a. Keep the trace between the device and the crystal as short as possible.
  - b. Design a good ground plane around oscillator pin.
  - c. Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - d. Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
  - g. Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other Crystal documentation. This signal is no longer required for the serial programming adapter.
- 21/ Crystal oscillator cannot be operated beyond  $105^\circ\text{C}$ . Parameters are characterized up to  $T_A = 105^\circ\text{C}$  unless otherwise noted.
- 22/ Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct set up, the effective load capacitance should always match the specification of the used crystal.
- 23/ Frequencies below the MIN specification set the fault flag. Frequency above the MAX specification do not set the fault flag. Frequency in between might set the flag.
- 24/ Measured with logic level input frequency but also applies to operation with crystals.
- 25/ Calculated using the box method:  $(\text{MAX}(-40^\circ\text{C to } 125^\circ\text{C}) - \text{MIN}(-40^\circ\text{C to } 125^\circ\text{C})) / \text{MIN}(-40^\circ\text{C to } 125^\circ\text{C}) / (125^\circ\text{C} - 40^\circ\text{C})$
- 26/ Calculated using the box method:  $(\text{MAX}(1.8 \text{ to } 3.6 \text{ V}) - \text{MIN}(1.8 \text{ to } 3.6 \text{ V})) / \text{MIN}(1.8 \text{ to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$
- 27/ The analog input range depends on the reference voltage applied to  $V_{REF}$ . If  $V_{REF}$  is source externally, the full scale range is defined by  $V_{FSR+} = +(V_{REF}/2)/\text{GAIN}$  and  $V_{FSR-} = -(V_{REF}/2)/\text{GAIN}$ . The analog input range should not exceed 80% of  $V_{FSR+}$  or  $V_{FSR-}$ .
- 28/ Calculated using the box method:  $(\text{MAX}(-40^\circ\text{C to } 85^\circ\text{C}) - \text{MIN}(-40^\circ\text{C to } 85^\circ\text{C})) / \text{MIN}(-40^\circ\text{C to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$
- 29/ Calculated using the ADC output code and the box method:  
 $(\text{MAX-code}(2.5 \text{ V to } 3.6 \text{ V}) - \text{MIN-code}(2.5 \text{ V to } 3.6 \text{ V})) / \text{MIN-code}(2.5 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 2.5 \text{ V})$
- 30/ There is no capacitance required on VREF. However, a capacitance of at least 100 nF is recommended to reduce any reference voltage noise.

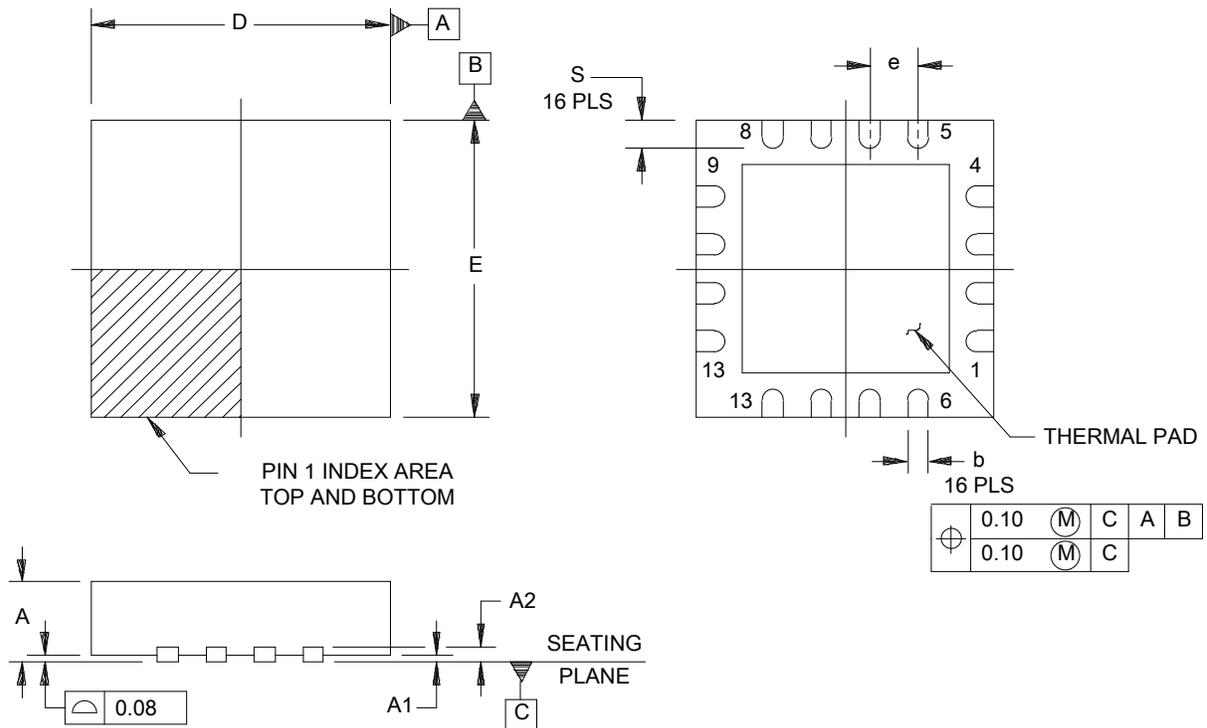
<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11613</b>
		REV	PAGE 19

TABLE I. Electrical performance characteristics - Continued.

- 31/ Values are not based on calculations using  $TC_{\text{Sensor}}$  or  $V_{\text{Offset,Sensor}}$  but on measurements.
- 32/ The following formula can be used to calculate the temperature sensor output voltage:  
 $V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}] + V_{\text{Offset,Sensor}} [\text{mV}]$  or  
 $V_{\text{Sensor,typ}} = TC_{\text{Sensor}} T [^{\circ}\text{C}] + V_{\text{Sensor}}(T_A = 0^{\circ}\text{C}) [\text{mV}]$
- 33/ Additional flash retention documentation located in manufacturer application report (SLAA392).
- 34/ The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- 35/ These values are hardwired into the Flash Controller's state machine ( $t_{\text{FTG}} = 1/f_{\text{FTG}}$ ).
- 36/ This parameter defines the minimum supply voltage VCC when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.
- 37/ Tools accessing the Spy-Bi-Wire interface need to wait for the maximum  $t_{\text{SBW,En}}$  time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
- 38/  $f_{\text{TCK}}$  may be restricted to meet the timing requirements of the module selected.
- 39/ Once the fuse is blown, no further access to the JTAG/Test, SPY-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	3.90	4.10
A1	0.00	0.05	e	0.65 BSC	
A2	0.20 REF		S	0.30	0.50
b	0.23	0.38			

**NOTES:**

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Quad Flatpack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance.
5. See the addition figure in the manufacturer product data sheet for details regarding the exposed thermal pad features and dimensions.
6. Fall within JEDEC MO-220.

FIGURE 1. Case outline.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	SIZE <b>A</b>	CODE IDENT NO. <b>16236</b>	DWG NO. <b>V62/11613</b>
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Case outline X			
Device type 01			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P1.0/TACLK/ACLK/A0+	9	$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$
2	P1.1/TA0/A0-/A4+	10	TEST/SBWTCK
3	P1.2/TA1/A1+/A4-	11	XOUT/P2.7
4	PA.3/VREF/A1-	12	XIN/P2.6/TA1
5	P1.4/SMCLK/A2+/TCK	13	AV <sub>SS</sub>
6	P1.5/TA0/A2-/SCLK/TMS	14	DV <sub>SS</sub>
7	P1.6/TA1/A3+/SDO/SCL/TDI/TCLK	15	AV <sub>CC</sub>
8	P1.7/A3-/SDI/SDA/TDO/TDI	16	DV <sub>CC</sub>

FIGURE 2. Terminal connections.

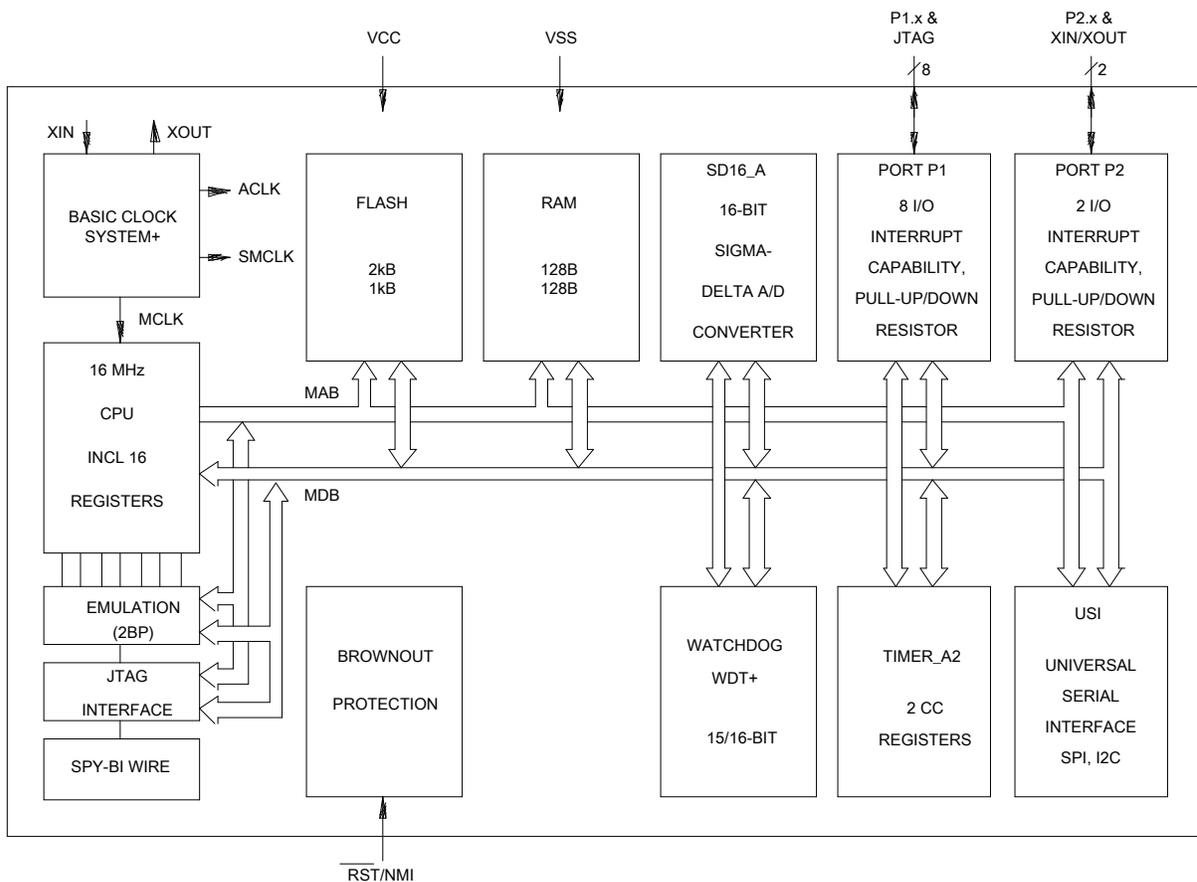


FIGURE 3. Functional diagram.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11613</b>
		REV	PAGE 22

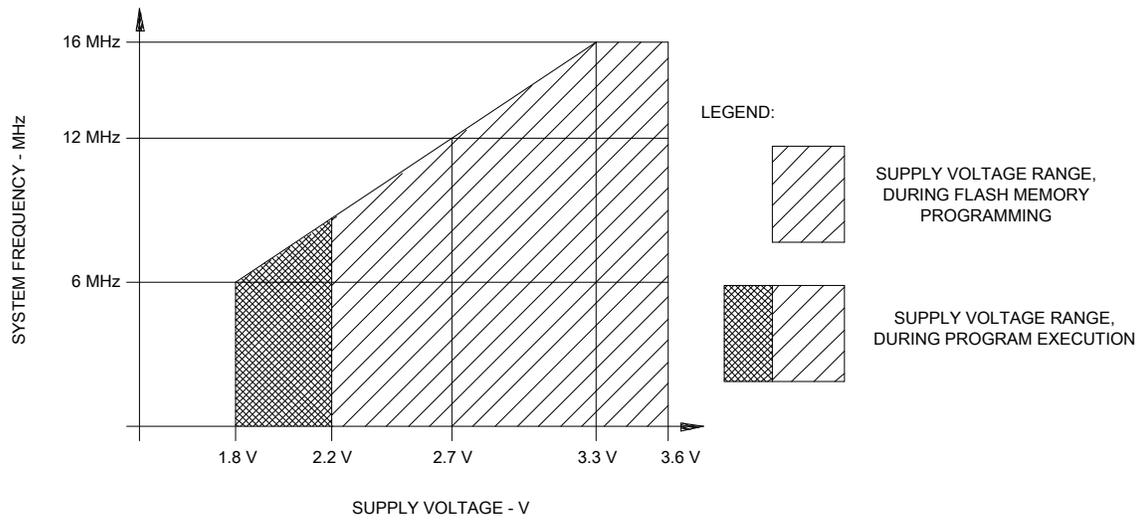


FIGURE 4. Safe operating area.

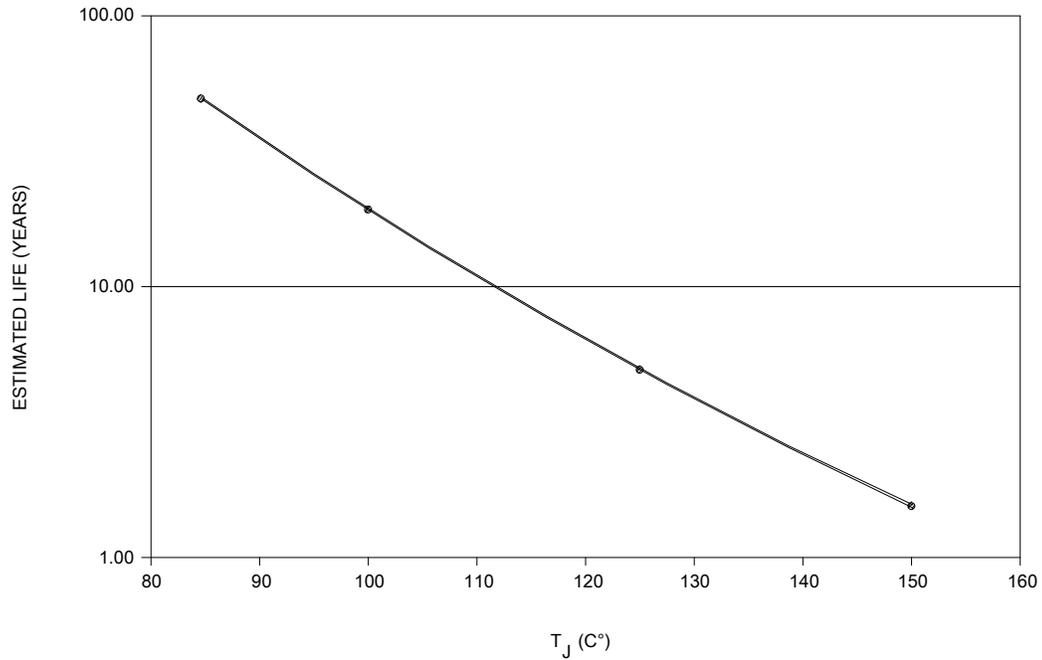


FIGURE 5. Operating life derating chart.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11613</b>
		<b>REV</b>	<b>PAGE 23</b>

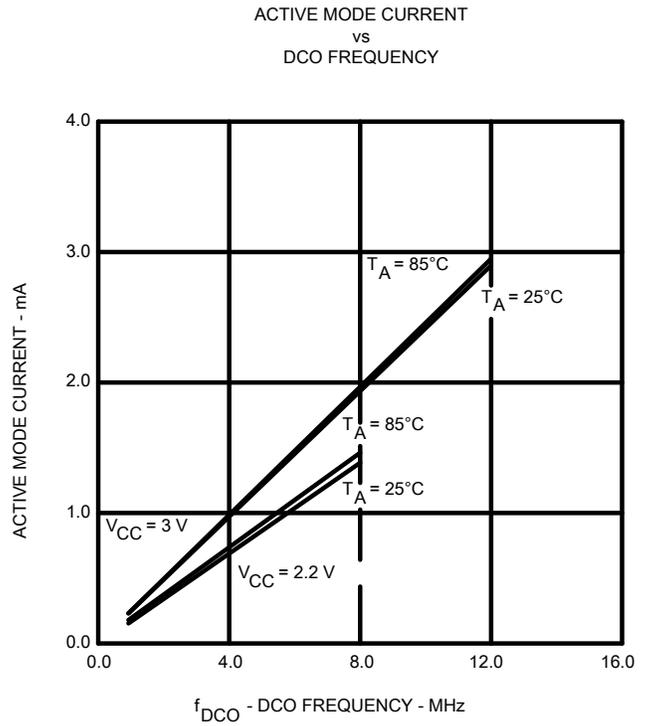
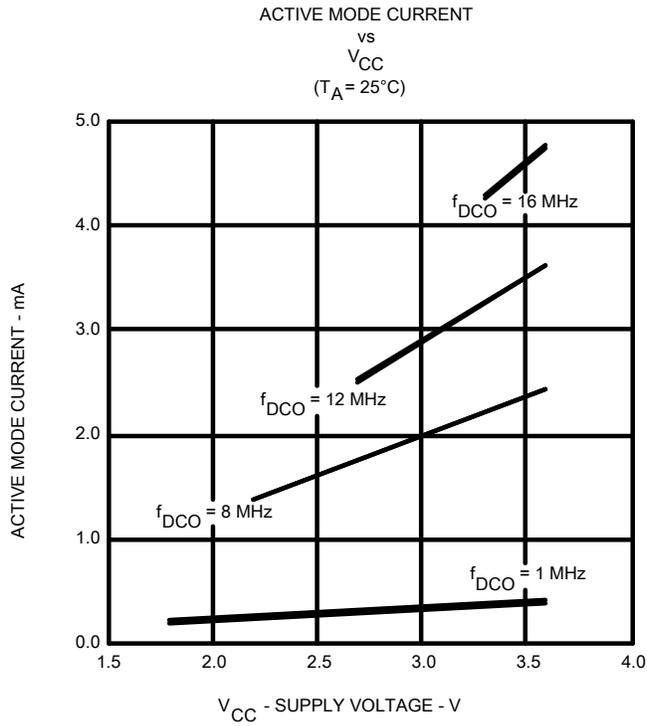


FIGURE 6. Active mode supply current (Into  $V_{CC}$ ).

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/11613
		REV	PAGE 24

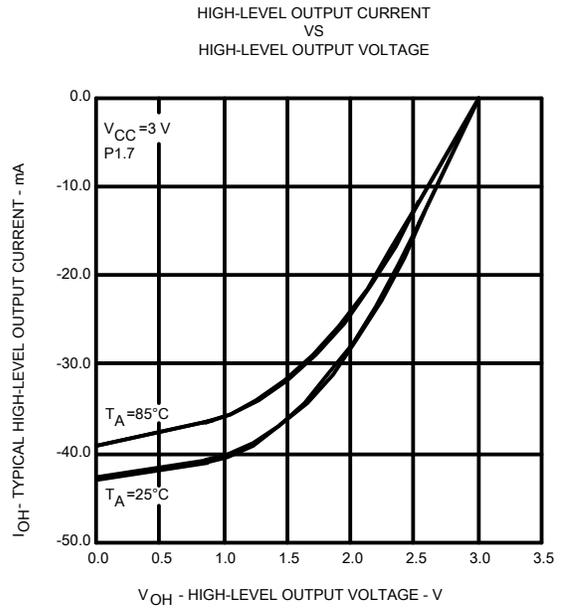
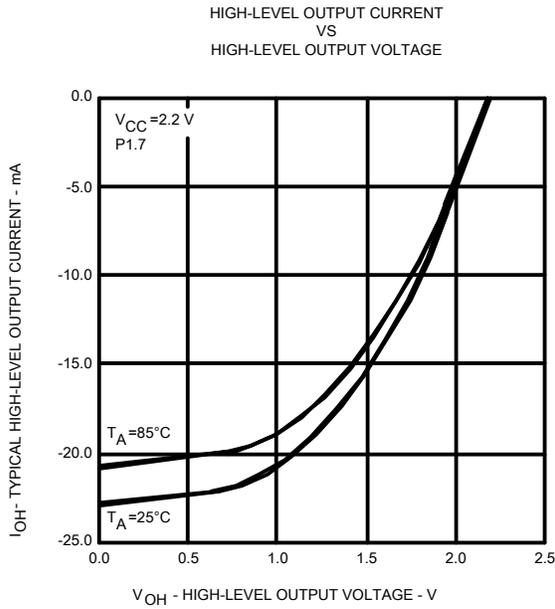
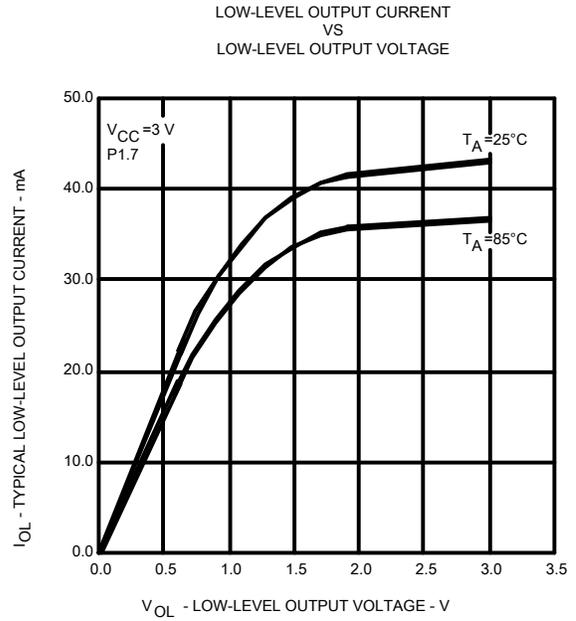
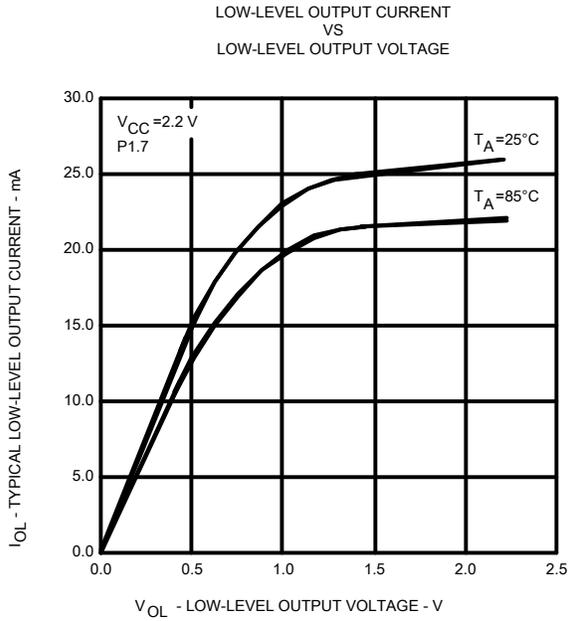


FIGURE 7. Typical characteristics - Output.

<p><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/11613</b></p>
		<p>REV</p>	<p>PAGE 25</p>

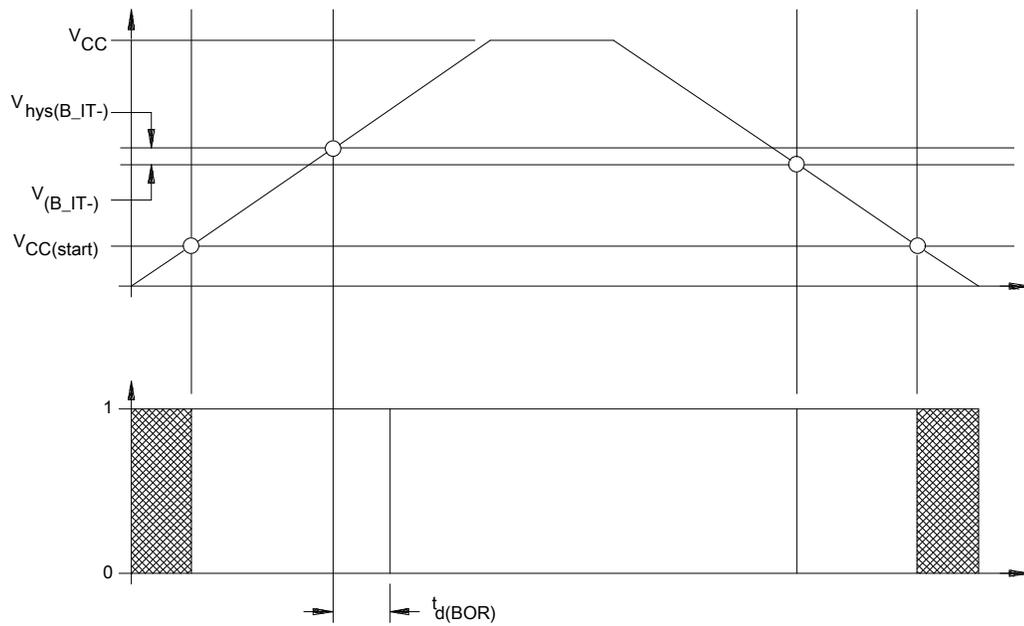


FIGURE 8. POR/Brownout Reset (BOR) vs Supply Voltage.

<p style="text-align: center;"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p style="text-align: center;">SIZE <b>A</b></p>	<p style="text-align: center;">CODE IDENT NO. <b>16236</b></p>	<p style="text-align: center;">DWG NO. <b>V62/11613</b></p>
		<p style="text-align: center;">REV</p>	<p style="text-align: center;">PAGE 26</p>

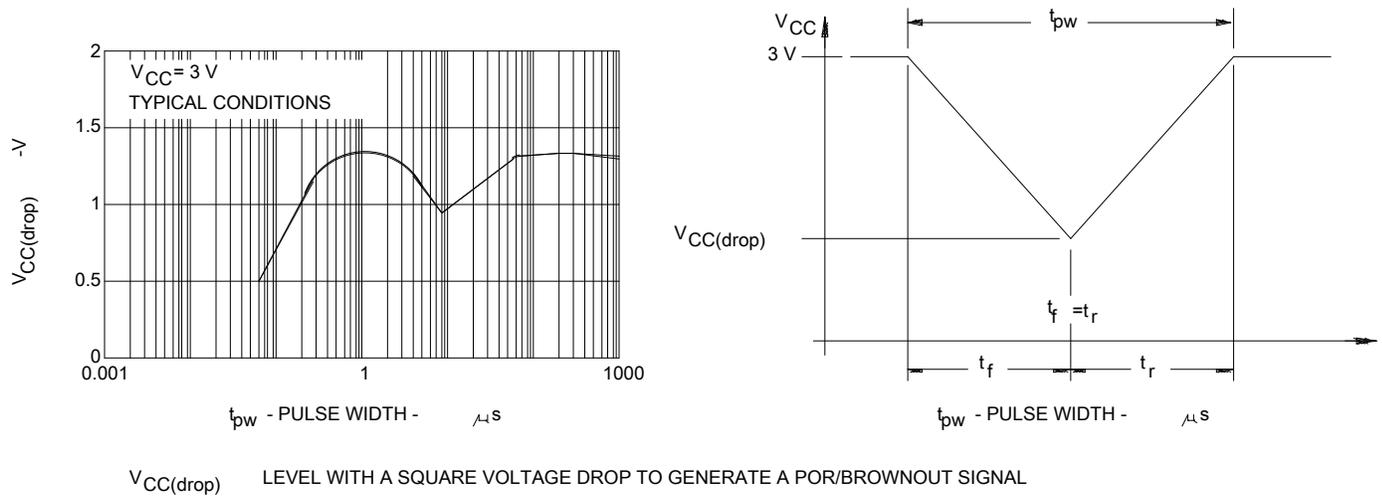
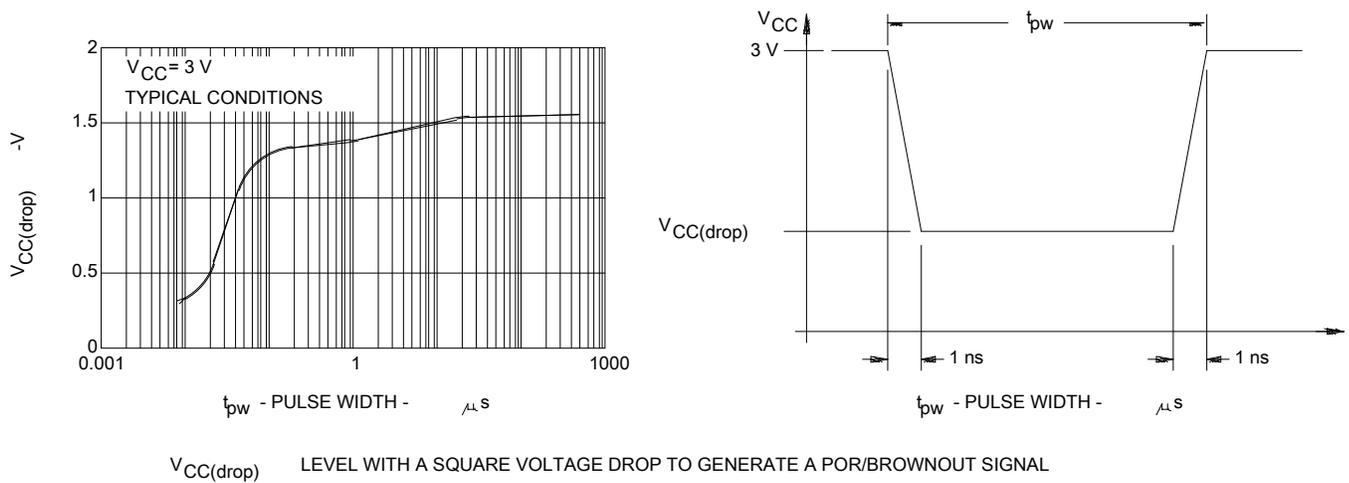


FIGURE 9. Typical characteristics – POR/Brownout reset (BOR).

<p align="center"><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p align="center"><b>SIZE A</b></p>	<p align="center"><b>CODE IDENT NO. 16236</b></p>	<p align="center"><b>DWG NO. V62/11613</b></p>
		<p align="center">REV</p>	<p align="center">PAGE 27</p>

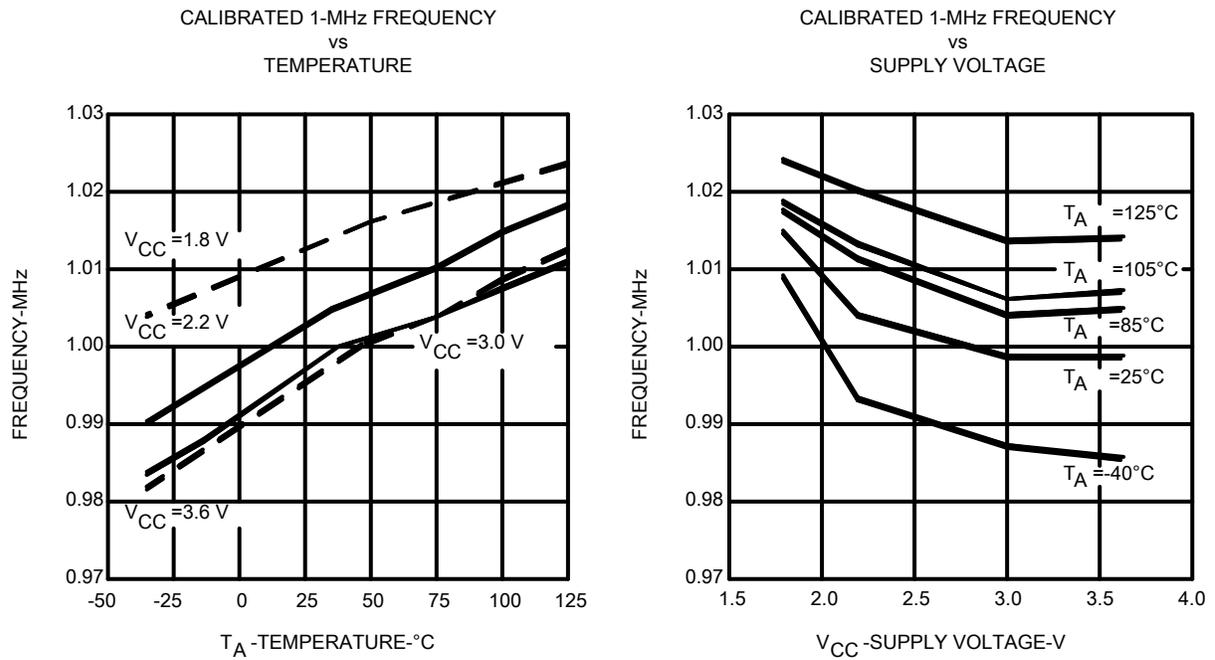


FIGURE 10. Typical characteristics – Calibrated 1 – MHz DCO frequency

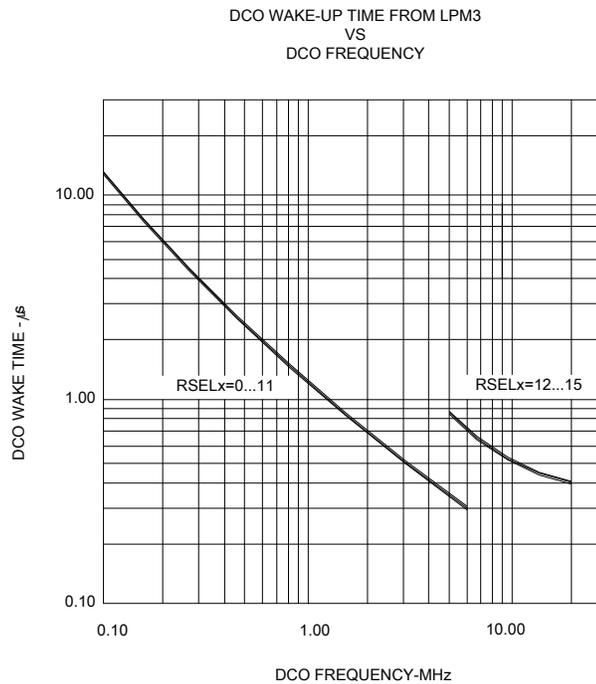


FIGURE 11. Typical characteristics – DCO clock wake up time from LPM3/4

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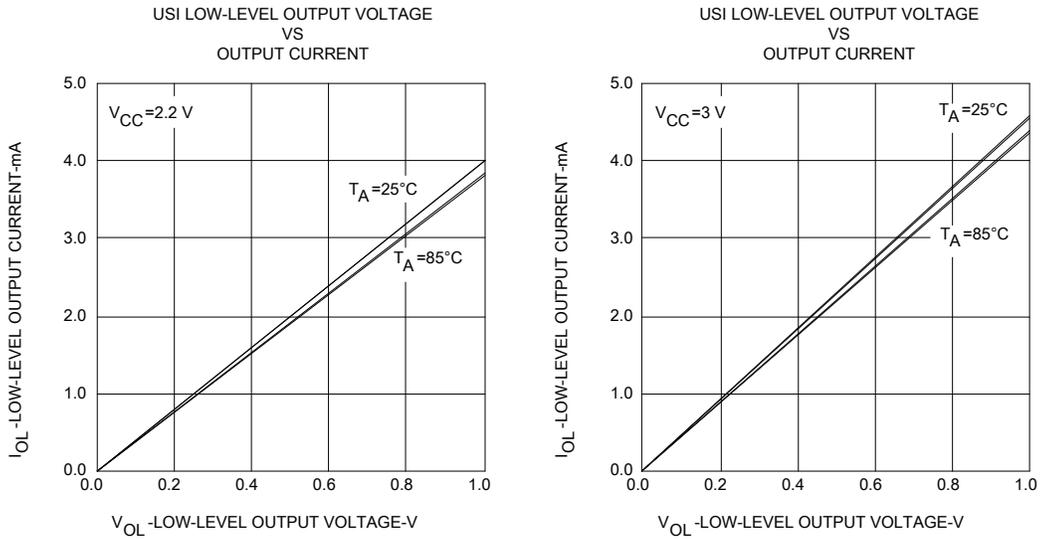


FIGURE 12. Typical characteristics – USI low level output voltage on SDA and SCL.

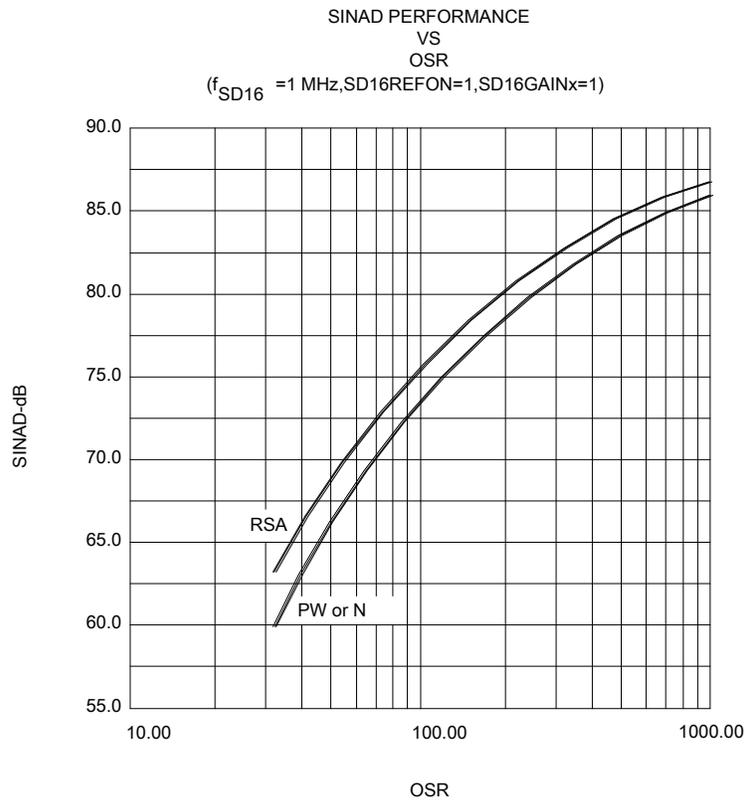


FIGURE 13. Typical characteristics – SD16. A SINAD performance over OSR

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		<b>REV</b>	<b>PAGE 29</b>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/11613-01XE	01295	MSP430F2013QRSATEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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		<b>REV</b>	<b>PAGE 30</b>