

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add nominal dimension limits under figure 1. Update document paragraphs to current requirements. - ro	17-06-15	C. SAFFLE
B	Add lead finish "E" to the devices. - PHN	18-02-15	Thomas M. Hess
C	Update document paragraphs to current requirements. - ro	23-03-03	James R. Eschmeyer



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

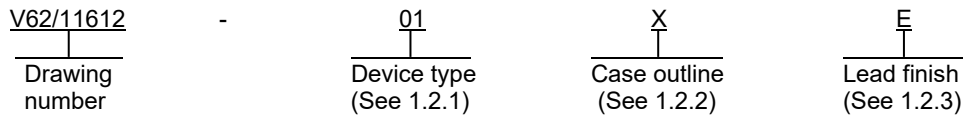
REV	C	C																				
SHEET	23	24																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A Original date of drawing YY-MM-DD 11-07-21	PREPARED BY RICK OFFICER		DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime																			
	CHECKED BY RAJESH PITHADIA		TITLE MICROCIRCUIT, DIGITAL-LINEAR, 8 CHANNEL, CMOS MULTIPLEXER, MONOLITHIC SILICON																			
	APPROVED BY CHARLES F. SAFFLE		DWG NO. V62/11612																			
	SIZE A	CAGE CODE 16236	PAGE 1 OF 24																			
REV		C																				

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8 channel CMOS multiplexer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADG1408-EP	8 channel CMOS multiplexer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MO-153-AB	Plastic thin shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Positive supply voltage (VDD) to negative supply voltage (VSS)	35 V
VDD to ground (GND)	-0.3 V to +25 V
VSS to GND	+0.3 V to -25 V
Analog inputs, digital inputs 2/	VSS – 0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Continuous current, source (S) or drain (D)	Table I data + 10%
Peak current, S or D (pulsed at 1 ms, 10% duty cycle maximum)	350 mA
Storage temperature range (TSTG)	-65°C to +150°C
Junction temperature (TJ)	+150°C
Lead temperature, soldering:	
Vapor phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Thermal resistance, junction to ambient (θJC)	50°C/W
Thermal resistance, junction to ambient (θJA)	150.4°C/W

1.4 Recommended operating conditions. 3/ 4/

Operating free-air temperature range (TA)	-55°C to +125°C
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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 4/ All ratings and specifications, please refer to relevant EP datasheet.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 4 through 14.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
15 V dual supply.							
Unless otherwise specified, V _{DD} = +1.5 V ±10%, V _{SS} = -15 V, ±10%, GND = 0 V.							
Analog switch section							
Analog signal range			-55°C to +125°C	01		V _{SS} to V _{DD}	V
On resistance	R _{ON}	V _S = ±10 V, I _S = -10 mA, V _{DD} = +13.5 V, V _{SS} = -13.5 V, see figure 4	+25°C	01		4.7	Ω
			-55°C to +125°C			6.7	
On resistance match between channels	ΔR _{ON}	V _S = ±10 V, I _S = -10 mA,	+25°C	01		0.78	Ω
			-55°C to +125°C			1.1	
On resistance flatness	R _{FLAT(ON)}	V _S = ±10 V, I _S = -10 mA,	+25°C	01		0.72	Ω
			-55°C to +125°C			0.92	
Leakage current section. V _{DD} = +16.5 V, V _{SS} = -16.5 V							
Source off leakage	I _{S(off)}	V _S = ±10 V, V _D = $\bar{+}$ 10 V, see figure 5	+25°C	01		±0.2	nA
			-55°C to +125°C			±5	
Drain off leakage	I _{D(off)}	V _S = ±10 V, V _D = $\bar{+}$ 10 V, see figure 5	+25°C	01		±0.45	nA
			-55°C to +125°C			±30	
Channel on leakage	I _D ,	V _S = V _D = ±10 V, see figure 6	+25°C	01		±1.5	nA
	I _{S(on)}		-55°C to +125°C			±30	
Digital inputs section.							
Input high voltage	V _{INH}		-55°C to +125°C	01	2.0		V
Input low voltage	V _{INL}		-55°C to +125°C	01		0.8	V
Input current	I _{IN}	V _{IN} = V _{GND} or V _{DD}	+25°C	01	±0.005 typical		μA
			-55°C to +125°C			±0.1	
Digital input capacitance	C _{IN}		+25°C	01	4 typical		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
15 V dual supply - continued.							
Unless otherwise specified, V _{DD} = +15 V ±10%, V _{SS} = -15 V, ±10%, GND = 0 V.							
Dynamic characteristics section. 2/							
Transition time	t _{TRANSITION}	V _S = 10 V, R _L = 100 Ω, C _L = 35 pF, see figure 7	+25°C	01		170	ns
			-55°C to +125°C			240	
Break before make time delay	t _{BBM}	V _{S1} = V _{S2} = 10 V, R _L = 100 Ω, C _L = 35 pF, see figure 8	+25°C	01	50 typical		ns
			-55°C to +125°C		19		
Active high digital input on time	t _{ON(EN)}	V _S = 10 V, R _L = 100 Ω, C _L = 35 pF, see figure 9	+25°C	01		120	ns
			-55°C to +125°C			165	
Active high digital input off time	t _{OFF(EN)}	V _S = 10 V, R _L = 100 Ω, C _L = 35 pF, see figure 9	+25°C	01		120	ns
			-55°C to +125°C			170	
Charge injection		V _S = 0 V, R _S = 0 Ω, C _L = 1 nF, see figure 10	+25°C	01	-50 typical		pC
Off isolation		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 11	+25°C	01	-70 typical		dB
Channel to channel crosstalk		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 12	+25°C	01	-70 typical		dB
Total harmonic distortion	THD+N	f = 20 Hz to 20 kHz, R _L = 110 Ω, 15 V _{PP} , see figure 13	+25°C	01	0.025 typical		%
-3 dB bandwidth		R _L = 50 Ω, C _L = 5 pF, see figure 14	+25°C	01	60 typical		MHz
Insertion loss		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 14	+25°C	01	0.24 typical		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
15 V dual supply - continued.							
Unless otherwise specified, V _{DD} = +15 V ±10%, V _{SS} = -15 V, ±10%, GND = 0 V.							
Dynamic section section – continued. 2/							
Source capacitance off	C _{S(off)}	f = 1 MHz	+25°C	01	14 typical		pF
Drain capacitance off	C _{D(off)}	f = 1 MHz	+25°C	01	80 typical		pF
Drain and source capacitance (on)	C _D , C _S (on)	f = 1 MHz	+25°C	01	135 typical		pF
Power requirements section. V _{DD} = +16.5 V, V _{SS} = -16.5 V							
Positive supply current	I _{DD}	Digital inputs = 0 V or V _{DD}	+25°C	01	0.002 typical		μA
			-55°C to +125°C		1		
		Digital inputs = 5 V	+25°C		220 typical		
			-55°C to +125°C		420		
Negative supply current	I _{SS}	Digital inputs = 0 V, 5 V, or V _{DD}	+25°C	01	0.002 typical		μA
			-55°C to +125°C		1		
Positive power supply voltage	V _{DD}		-55°C to +125°C	01	±4.5		V
Negative power supply voltage	V _{SS}		-55°C to +125°C	01		±16.5	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
12 V single supply .							
Unless otherwise specified. V _{DD} = +12 V ±10%, V _{SS} = 0 V, GND = 0 V.							
Analog switch section.							
Analog signal range			-55°C to +125°C	01		0 to V _{DD}	V
On resistance	R _{ON}	V _S = 0 V to 10 V, I _S = -10 mA, V _{DD} = 10.8 V, V _{SS} = 0 V, see figure 4	+25°C	01		8	Ω
			-55°C to +125°C			11.2	
On resistance match between channels	ΔR _{ON}	V _S = 0 V to 10 V, I _S = -10 mA,	+25°C	01		0.82	Ω
			-55°C to +125°C			1.1	
On resistance flatness	R _{F(ON)}	V _S = 0 V to 10 V, I _S = -10 mA,	+25°C	01		2.5	Ω
			-55°C to +125°C			2.8	
Leakage current section. V _{DD} = 13.2 V							
Source off leakage	I _{S(off)}	V _S = 1 V and 10 V, V _D = 10 V and 1 V, see figure 5	+25°C	01		±0.2	nA
			-55°C to +125°C			±5	
Drain off leakage	I _{D(off)}	V _S = 1 V and 10 V, V _D = 10 V and 1 V, see figure 5	+25°C	01		±0.45	nA
			-55°C to +125°C			±37	
Channel on leakage	I _D , I _{S(on)}	V _S = V _D = 1 V or 10 V, see figure 6	+25°C	01		±0.44	nA
			-55°C to +125°C			±32	
Digital inputs section.							
Input high voltage	V _{INH}		-55°C to +125°C	01	2.0		V
Input low voltage	V _{INL}		-55°C to +125°C	01		0.8	V
Input current	I _{IN}	V _{IN} = V _{GN} D or V _{DD}	+25°C	01	±0.005 typical		μA
			-55°C to +125°C			±0.1	
Digital input capacitance	C _{IN}		+25°C	01	5 typical		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
12 V single supply - continued.							
Unless otherwise specified. V _{DD} = +12 V ±10%, V _{SS} = 0 V, GND = 0 V.							
Dynamic characteristics section. 2/							
Transition time	t _{TRANSITION}	V _S = 8 V, R _L = 100 Ω, C _L = 35 pF, see figure 7	+25°C	01		260	ns
			-55°C to +125°C			380	
Break before make time delay	t _{BBM}	V _{S1} = V _{S2} = 8 V, R _L = 100 Ω, C _L = 35 pF, see figure 8	+25°C	01	90 typical		ns
			-55°C to +125°C		40		
Active high digital input on time	t _{ON(EN)}	V _S = 8 V, R _L = 100 Ω, C _L = 35 pF, see figure 9	+25°C	01		210	ns
			-55°C to +125°C			285	
Active high digital input off time	t _{OFF(EN)}	V _S = 8 V, R _L = 100 Ω, C _L = 35 pF, see figure 9	+25°C	01		145	ns
			-55°C to +125°C			200	
Charge injection		V _S = 6 V, R _S = 0 Ω, C _L = 1 nF, see figure 10	+25°C	01	-12 typical		pC
Off isolation		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 11	+25°C	01	-70 typical		dB
Channel to channel crosstalk		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 12	+25°C	01	-70 typical		dB
-3 dB bandwidth		R _L = 50 Ω, C _L = 5 pF, see figure 14	+25°C	01	36 typical		MHz
Insertion loss		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 14	+25°C	01	0.5 typical		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
12 V single supply – continued.							
Unless otherwise specified, V _{DD} = +12 V ±10%, V _{SS} = 0 V, GND = 0 V.							
Dynamic characteristics section - continued. 2/							
Source capacitance off	C _{S(off)}	f = 1 MHz	+25°C	01	25	typical	pF
Drain capacitance off	C _{D(off)}	f = 1 MHz	+25°C	01	165	typical	pF
Drain and source capacitance (on)	C _D , C _S (on)	f = 1 MHz	+25°C	01	200	typical	pF
Power requirements section. V _{DD} = 13.2 V							
Positive supply current	I _{DD}	Digital inputs = 0 V or V _{DD}	+25°C	01	0.002 typical		μA
			-55°C to +125°C		1		
		Digital inputs = 5 V	+25°C		220 typical		
			-55°C to +125°C		420		
Positive power supply voltage	V _{DD}	V _{SS} = 0 V, GND = 0 V	-55°C to +125°C	01	5	16.5	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
5 V dual supply.							
Unless otherwise specified. VDD = +5 V ±10%, VSS = -5 V, ±10%, GND = 0 V.							
Analog switch section.							
Analog signal range			-55°C to +125°C	01		VSS to VDD	V
On resistance	RON	VS = ±4.5 V, IS = -10 mA, VDD = +4.5 V, VSS = -4.5 V, see figure 4	+25°C	01		9	Ω
			-55°C to +125°C			12	
On resistance match between channels	ΔRON	VS = ±4.5 V, IS = -10 mA,	+25°C	01		0.78	Ω
			-55°C to +125°C			1.1	
On resistance flatness	RFLAT(ON)	VS = ±4.5 V, IS = -10 mA,	+25°C	01		2.5	Ω
			-55°C to +125°C			3	
Leakage current section. VDD = +5.5 V, VSS = -5.5 V							
Source off leakage	IS(off)	VS = ±4.5 V, VD = $\bar{+}$ 4.5 V, see figure 5	+25°C	01		±0.2	nA
			-55°C to +125°C			±5	
Drain off leakage	ID(off)	VS = ±4.5 V, VD = $\bar{+}$ 4.5 V, see figure 5	+25°C	01		±0.45	nA
			-55°C to +125°C			±20	
Channel on leakage	ID, IS(on)	VS = VD = ±4.5 V, see figure 6	+25°C	01		±0.3	nA
			-55°C to +125°C			±22	
Digital inputs section.							
Input high voltage	VINH		-55°C to +125°C	01	2.0		V
Input low voltage	VINL		-55°C to +125°C	01		0.8	V
Input current	IIN	VIN = VGND or VDD	+25°C	01	±0.005 typical		μA
			-55°C to +125°C			±0.1	
Digital input capacitance	CIN		+25°C	01	5 typical		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
5 V dual supply – continued.							
Unless otherwise specified, V _{DD} = +5 V ±10%, V _{SS} = -5 V, ±10%, GND = 0 V.							
Dynamic characteristics section. 2/							
Transition time	t _{TRANSITION}	V _S = 5 V, R _L = 100 Ω, C _L = 35 pF, see figure 7	+25°C	01		440	ns
			-55°C to +125°C			550	
Break before make time delay	t _{BBM}	V _{S1} = V _{S2} = 5 V, R _L = 100 Ω, C _L = 35 pF, see figure 8	+25°C	01	100 typical		ns
			-55°C to +125°C		45		
Active high digital input on time	t _{ON(EN)}	V _S = 5 V, R _L = 100 Ω, C _L = 35 pF, see figure 9	+25°C	01		330	ns
			-55°C to +125°C			440	
Active high digital input off time	t _{OFF(EN)}	V _S = 5 V, R _L = 100 Ω, C _L = 35 pF, see figure 9	+25°C	01		285	ns
			-55°C to +125°C			370	
Charge injection		V _S = 0 V, R _S = 0 Ω, C _L = 1 nF, see figure 10	+25°C	01	-10 typical		pC
Off isolation		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 11	+25°C	01	-70 typical		dB
Channel to channel crosstalk		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 12	+25°C	01	-70 typical		dB
Total harmonic distortion	THD+N	f = 20 Hz to 20 kHz, R _L = 110 Ω, 5 V _{PP} , see figure 13	+25°C	01	0.06 typical		%
-3 dB bandwidth		R _L = 50 Ω, C _L = 5 pF, see figure 14	+25°C	01	40 typical		MHz
Insertion loss		f = 1 MHz, R _L = 50 Ω, C _L = 5 pF, see figure 14	+25°C	01	0.5 typical		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
5 V dual supply – continued.							
Unless otherwise specified. V _{DD} = +5 V ±10%, V _{SS} = -5 V, ±10%, GND = 0 V.							
Dynamic characteristics section - continued. 2/							
Source capacitance off	C _{S(off)}	f = 1 MHz	+25°C	01	20 typical		pF
Drain capacitance off	C _{D(off)}	f = 1 MHz	+25°C	01	130 typical		pF
Drain and source capacitance (on)	C _D , C _S (on)	f = 1 MHz	+25°C	01	180 typical		pF
Power requirements section. V _{DD} = +5.5 V, V _{SS} = -5.5 V							
Positive supply current	I _{DD}	Digital inputs = 0 V or V _{DD}	+25°C	01	0.001 typical		μA
			-55°C to +125°C			1	
Negative supply current	I _{SS}	Digital inputs = 0 V, 5 V, or V _{DD}	+25°C	01	0.001 typical		μA
			-55°C to +125°C			1	
Positive power supply voltage	V _{DD}		-55°C to +125°C	01	±4.5		V
Negative power supply voltage	V _{SS}		-55°C to +125°C	01		±16.5	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Continuous current, per channel, source (S) or drain (D). <u>2/</u>							
Continuous current, 15 V dual supply		VDD = +13.5 V, VSS = -13.5 V	25°C	01		190	mA
			85°C			105	
			125°C			50	
Continuous current, 12 V single supply		VDD = 10.8 V, VSS = 0 V	25°C	01		160	mA
			85°C			95	
			125°C			50	
Continuous current, 5 V dual supply		VDD = +4.5, VSS = -4.5 V	25°C	01		155	mA
			85°C			90	
			125°C			45	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Guaranteed by design, not subject to production test.

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Case X

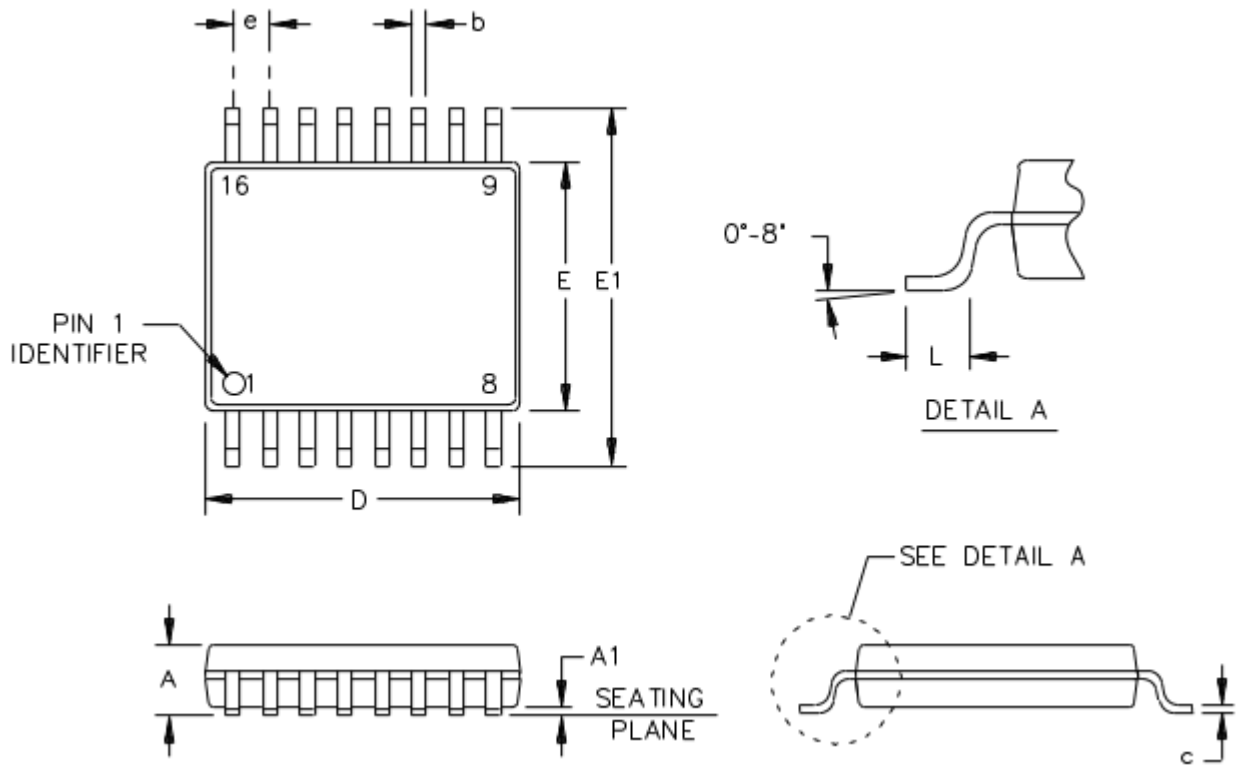


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	.047	---	---	1.20
A1	.001	---	.005	0.05	---	0.15
b	.007	---	.011	0.19	---	0.30
c	.003	---	.007	0.09	---	0.20
D	.192	.196	.200	4.90	5.00	5.10
E	.169	.173	.177	4.30	4.40	4.50
E1	.251 BSC			6.40 BSC		
e	.025 BSC			0.65 BSC		
L	.017	.023	.029	0.45	0.60	0.75

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AB.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	A0	Logic control input.
2	EN	Active high digital input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	VSS	Most negative power supply potential. In supply single applications, it can be connected to ground.
4	S1	Source terminal 1. Can be an input or an output.
5	S2	Source terminal 2. Can be an input or an output.
6	S3	Source terminal 3. Can be an input or an output.
7	S4	Source terminal 4. Can be an input or an output.
8	D	Drain terminal. Can be an input or an output.
9	S8	Source terminal 8. Can be an input or an output.
10	S7	Source terminal 7. Can be an input or an output.
11	S6	Source terminal 6. Can be an input or an output.
12	S5	Source terminal 5. Can be an input or an output.
13	VDD	Most positive power supply potential.
14	GND	Ground (0 V) reference.
15	A2	Logic control input.
16	A1	Logic control input.

FIGURE 2. Terminal connections.

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A2	A1	A0	EN	On switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

FIGURE 3. Truth table.

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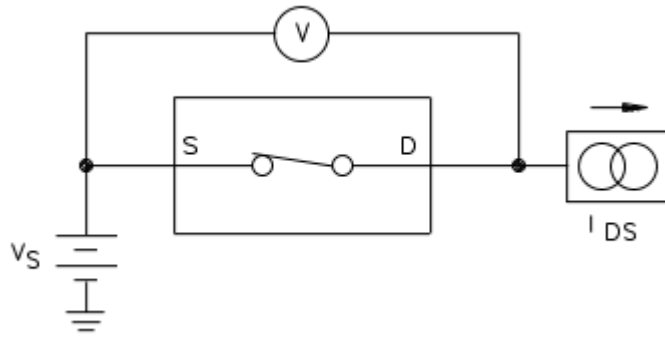


FIGURE 4. On resistance.

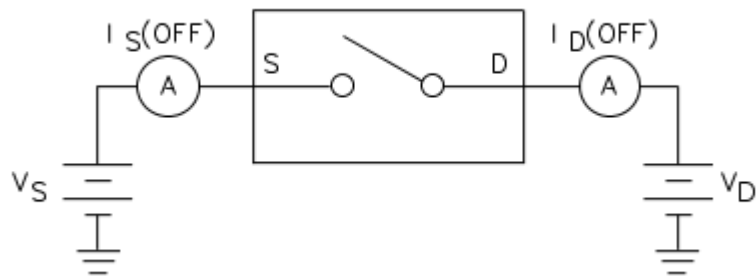


FIGURE 5. Off leakage.

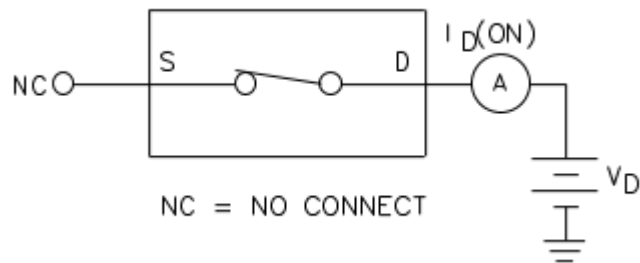


FIGURE 6. On leakage.

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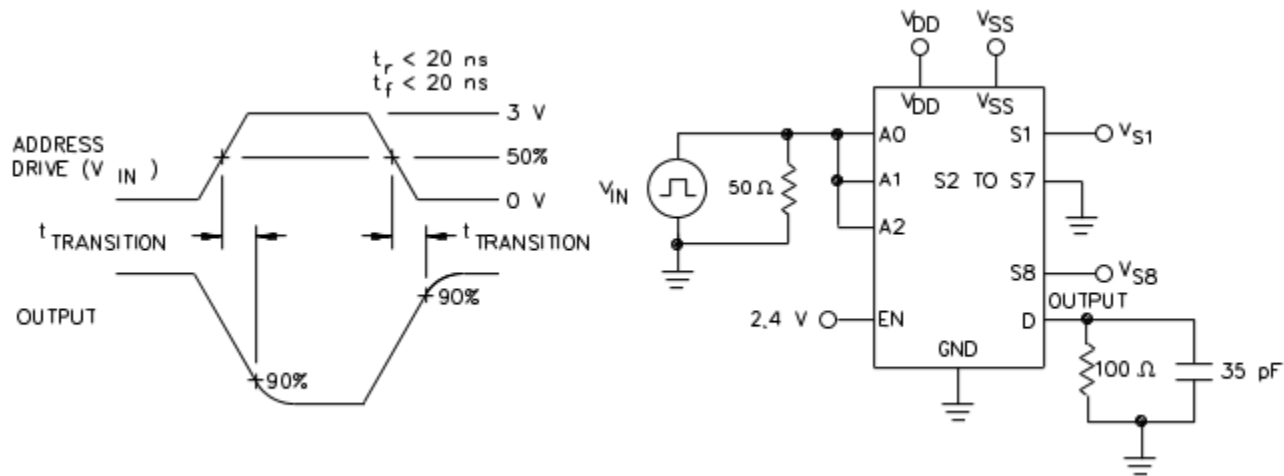


FIGURE 7. Address to output switching times, $t_{\text{TRANSITIONS}}$.

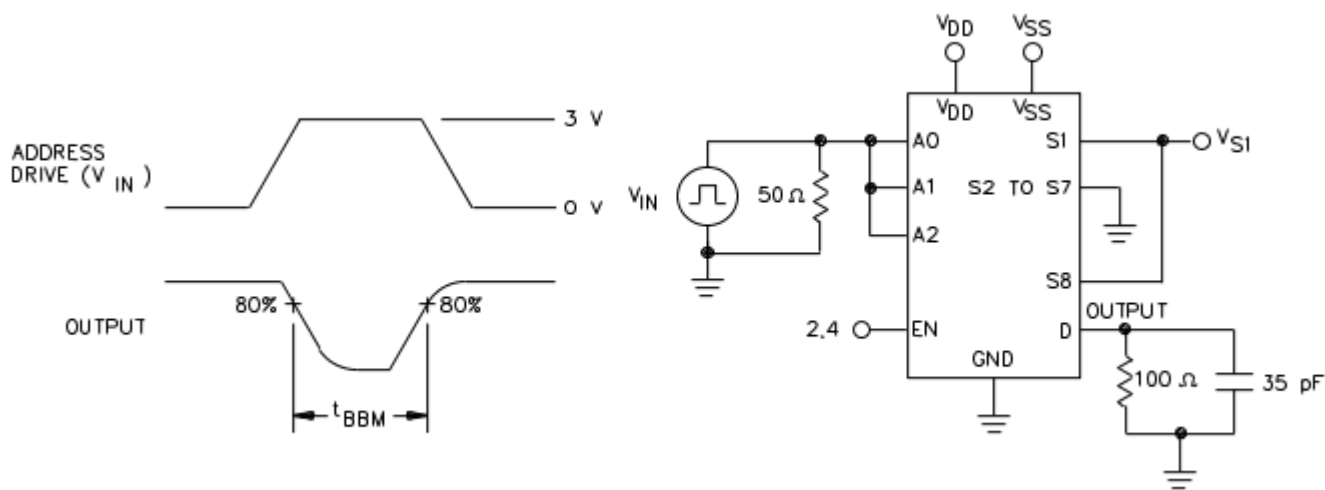


FIGURE 8. Break before make delay, t_{BBM} .

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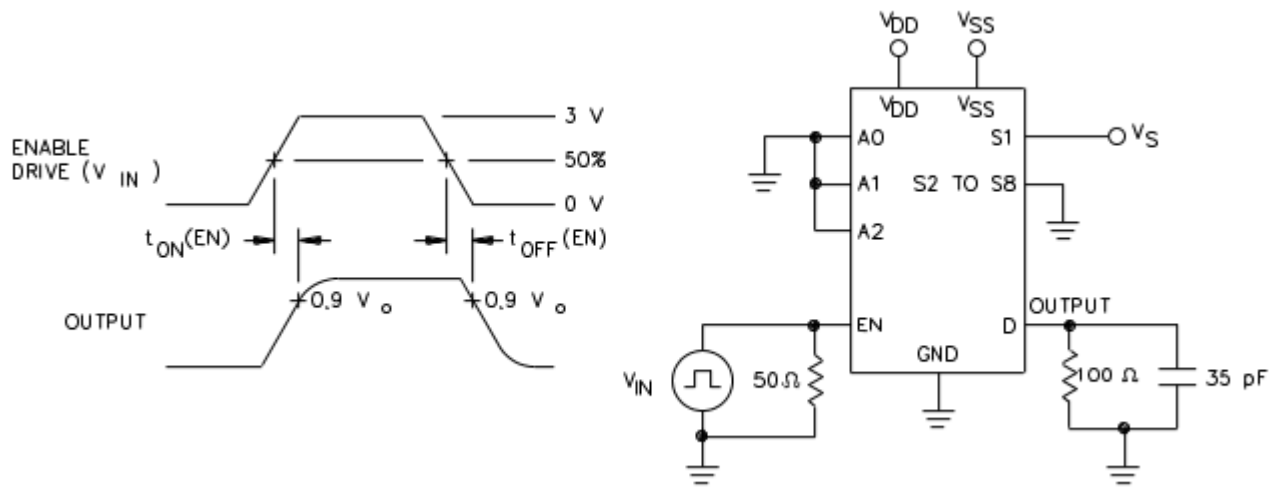


FIGURE 9. Enable delay, $t_{ON}(EN)$, $t_{OFF}(EN)$.

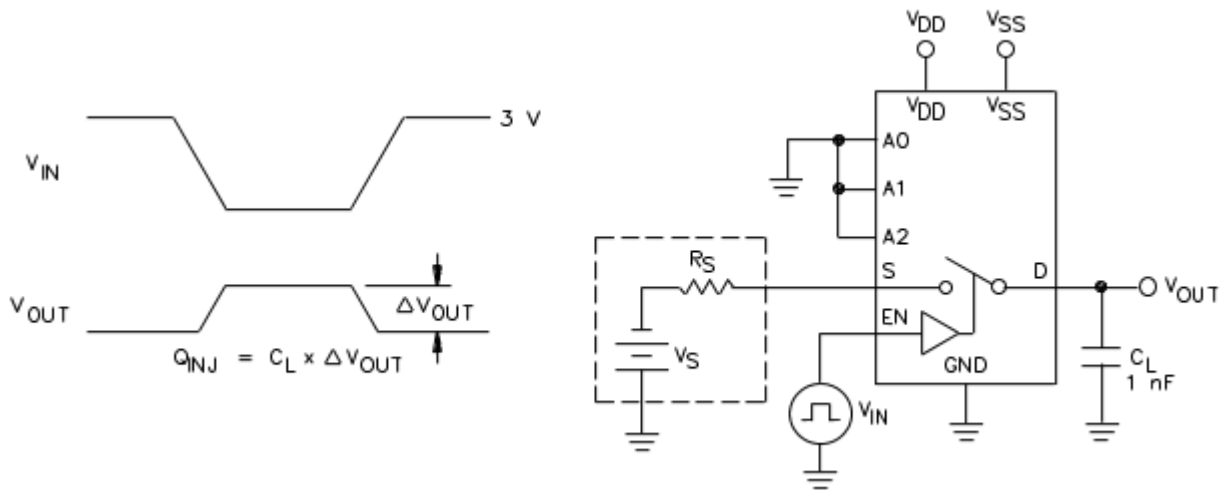
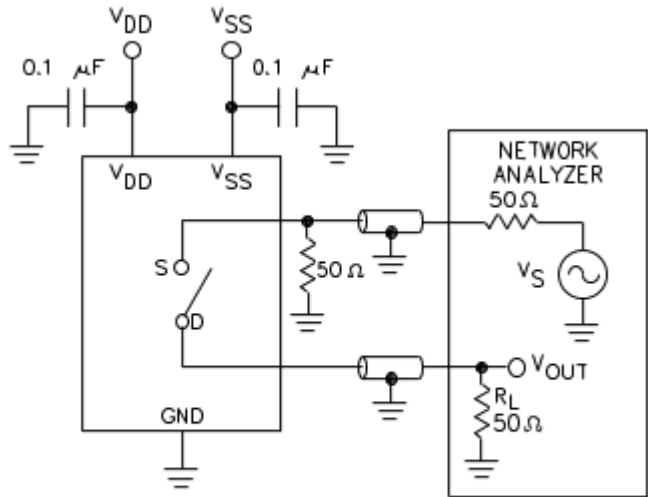


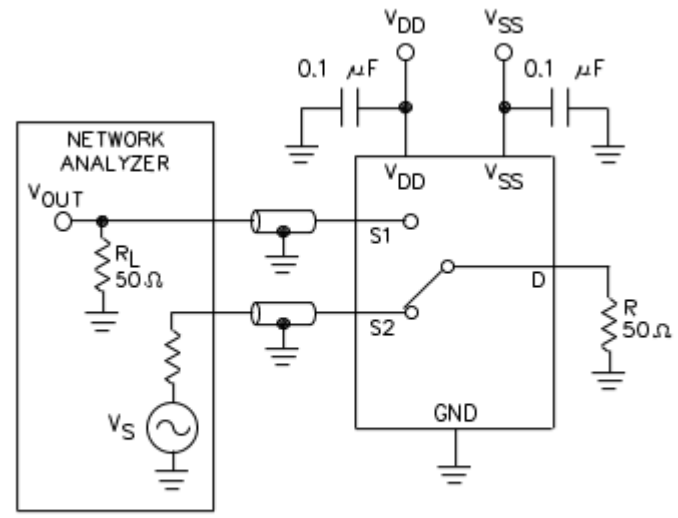
FIGURE 10. Charge injection.

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$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_S}$$

FIGURE 11. Off isolation.



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_S}$$

FIGURE 12. Channel to channel crosstalk.

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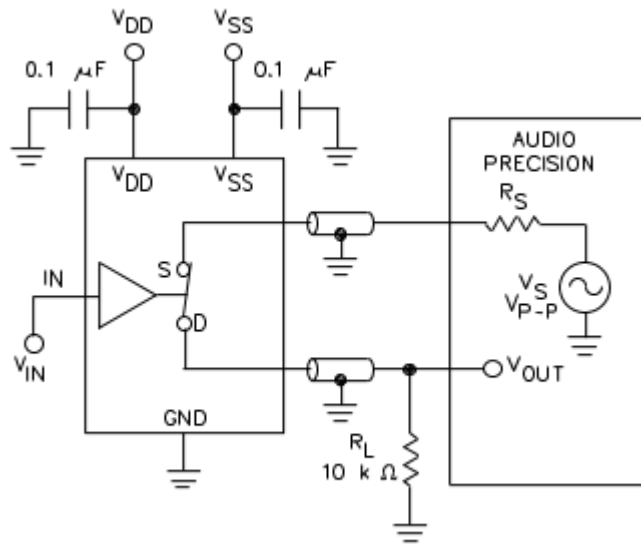
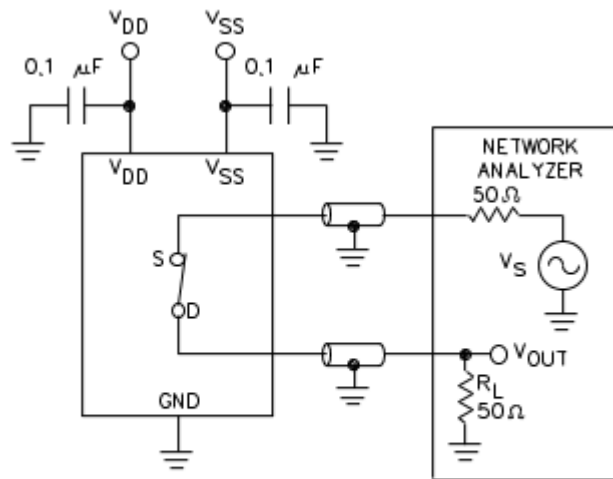


FIGURE 13. THD + noise.



$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

FIGURE 14. Insertion loss.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/11612-01XB	24355	ADG1408SRU-EP-RL7
V62/11612-01XE	24355	ADG1408SRUZ-EP
		ADG1408SRUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: 20 Alpha Road
 Chelmsford, MA 01824-4123

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