REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. - ro	17-04-20	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A					
	PAGE		1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY-MM-DD 11-07-26	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 12-BIT ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/11611**
	REV **A**	**PAGE** 1 **OF** 14

AMSC N/A

5962-V041-17

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12 bit analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V6211611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7476-EP	12 bit analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	6	MO-178-AB	Plastic small outline surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}) to ground (GND)	-0.3 V to +7 V
Analog input voltage to GND	-0.3 V to V_{DD} + 0.3 V
Digital input voltage to GND	-0.3 V to 7 V
Digital output voltage to GND	-0.3 V to V_{DD} + 0.3 V
Input current to any pin except supplies	±10 m A 2/
Junction temperature range (T_J)	150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature, soldering reflow (10 seconds to 30 seconds)	235°C
Lead (Pb) free temperature, soldering reflow	255°C
Electrostatic discharge (ESD)	3.5 kV
Thermal resistance, junction to ambient (θ_{JC})	92°C/W
Thermal resistance, junction to ambient (θ_{JA})	230°C/W

1.4 Recommended operating conditions. 3/ 4/

Supply voltage (V_{DD}) range	+2.35 V to +5.25 V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ All ratings and specifications, please refer to the relevant EP datasheet.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Load circuit for digital output timing specifications. The load circuit for digital output timing specifications shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance section.		f_{IN} = 100 kHz sine wave					
Signal to (noise + distortion)	SINAD		+25°C	01	70		dB
			-55°C to +125°C		69		
Signal to noise ratio	SNR		-55°C to +125°C	01	70		dB
Total harmonic distortion	THD		-55°C to +125°C	01	-78 typical		dB
Peak harmonic or spurious noise	SFDR		-55°C to +125°C	01	-80 typical		dB
Intermodulation distortion, second order terms	IMD	fa = 103.5 kHz, fb = 113.5 kHz	-55°C to +125°C	01	-78 typical		dB
Intermodulation distortion, third order terms	IMD	fa = 103.5 kHz, fb = 113.5 kHz	-55°C to +125°C	01	-78 typical		dB
Aperture delay			-55°C to +125°C	01	10 typical		ns
Aperture jitter			-55°C to +125°C	01	30 typical		ps
Full power bandwidth	FPBW	At 3 dB	-55°C to +125°C	01	6.5 typical		MHz
DC accuracy section.		V_{DD} = 2.35 V to 3.6 V 3/					
Resolution			-55°C to +125°C	01	12		Bits
Integral nonlinearity	INL		+25°C	01	±0.6 typical		LSB
			-55°C to +125°C			±1.5	
Differential nonlinearity	DNL	Guaranteed in missed codes to 12 bits	+25°C	01	±0.75 typical		LSB
			-55°C to +125°C		-0.9	+1.5	
Offset error	OE		-55°C to +125°C	01		±2	LSB
Gain error	GE		-55°C to +125°C	01		±2	LSB
Analog input section.							
Input voltage ranges	V_{IN}		-55°C to +125°C	01	0 to V_{DD}		V
DC leakage current			-55°C to +125°C	01		±1	µA
Input capacitance	C_{IN}		-55°C to +125°C	01	30 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic input section.							
Input high voltage	V_{INH}		-55°C to +125°C	01	2.4		V
		V_{DD} = 2.35 V			1.8		
Input low voltage	V_{INL}	V_{DD} = 3 V	-55°C to +125°C	01		0.4	V
		V_{DD} = 5 V				0.8	
Input current, SCLK pin	I_{IN}	Typically 10 nA, V_{IN} = 0 V or V_{DD}	-55°C to +125°C	01		±1	µA
Input current, $\overline{CS}$ pin	I_{IN}		-55°C to +125°C	01	±1 typical		µA
Input capacitance	C_{IN}	4/	-55°C to +125°C	01		10	pF
Logic output section.							
Output high voltage	V_{OH}	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 5.25 V	-55°C to +125°C	01	V_{DD} – 0.2		V
Output low voltage	V_{OL}	I_{SINK} = 200 µA	-55°C to +125°C	01		0.4	V
Floating state leakage current			-55°C to +125°C	01		±10	µA
Floating state output capacitance		4/	-55°C to +125°C	01		10	pF
Output coding		Straight (natural) binary	-55°C to +125°C	01			
Conversion rate section.							
Conversion time		16 SCLK	-55°C to +125°C	01		1.33	µs
Track and hold acquisition time		Full scale step input	-55°C to +125°C	01		500	ns
		Sine wave input ≤ 100 kHz				400	
Throughput rate			-55°C to +125°C	01		600	kSPS

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power requirements section.							
Supply voltage	V_{DD}		-55°C to +125°C	01	2.35	5.25	V
Supply current, normal mode (static)	I_{DD}	Digital I/Ps = 0 V or V_{DD}, V_{DD} = 4.75 V to 5.25 V, SCLK on or off	-55°C to +125°C	01	2 typical		mA
		Digital I/Ps = 0 V or V_{DD}, V_{DD} = 2.35 V to 3.6 V, SCLK on or off			1 typical		
Supply current, normal mode (operational)	I_{DD}	Digital I/Ps = 0 V or V_{DD}, V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = f_{SAMPLE} max 5/	-55°C to +125°C	01		3	mA
		Digital I/Ps = 0 V or V_{DD}, V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = f_{SAMPLE} max 5/				1.4	
Full power down mode	FPDM	SCLK off	-55°C to +125°C	01		1	µA
		SCLK on				80	
Power dissipation, normal mode (operational)	P_D	V_{DD} = 5 V, f_{SAMPLE} = f_{SAMPLE} max 5/	-55°C to +125°C	01		15	mW
		V_{DD} = 3 V, f_{SAMPLE} = f_{SAMPLE} max 5/				4.2	
Power dissipation, full power down	P_D	V_{DD} = 5 V, SCLK off	-55°C to +125°C	01		5	µW
		V_{DD} = 3 V, SCLK off				3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions 6/ 7/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications section.							
Serial clock frequency 8/	f_{SCLK}	At 3 V	-55°C to +125°C	01	10		kHz
		At 5 V			10		
		At 3 V				12	MHz
		At 5 V				12	
Conversion time	$t_{CONVERT}$	At 3 V	-55°C to +125°C	01	16 x t_{SCLK}		
		At 5 V			16 x t_{SCLK}		
Minimum quite time required between bus relinquish and start of next conversion	t_{QUIET}	At 3 V	-55°C to +125°C	01	50		ns
		At 5 V			50		
Minimum $\overline{CS}$ pulse width	t_1	At 3 V	-55°C to +125°C	01	10		ns
		At 5 V			10		
$\overline{CS}$ to SCLK setup time	t_2	At 3 V	-55°C to +125°C	01	10		ns
		At 5 V			10		
Delay from $\overline{CS}$ 9/ until SDATA three state disabled	t_3	At 3 V	-55°C to +125°C	01		20	ns
		At 5 V				20	
Data access time 9/ after SCLK falling edge, A version	t_4	At 3 V	-55°C to +125°C	01		40	ns
		At 5 V				20	
Data access time 9/ after SCLK falling edge, B version	t_4	At 3 V	-55°C to +125°C	01		70	ns
		At 5 V				20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions 6/ 7/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specifications section - continued.							
SCLK low pulse width	t_5	At 3 V	-55°C to +125°C	01	0.4 x t_{SCLK}		ns
		At 5 V			0.4 x t_{SCLK}		
SCLK high pulse width	t_6	At 3 V	-55°C to +125°C	01	0.4 x t_{SCLK}		ns
		At 5 V			0.4 x t_{SCLK}		
SCLK to data valid hold time	t_7	At 3 V	-55°C to +125°C	01	10		ns
		At 5 V			10		
SCLK falling edge 10/ to SDATA high impedance	t_8	At 3 V	-55°C to +125°C	01	10	25	ns
		At 5 V			10	25	
Power up time from full power down	$t_{POWER-UP}$	At 3 V	-55°C to +125°C	01	1 typical		µs
		At 5 V			1 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 12 MHz, and f_{SAMPLE} = 600 kSPS

3/ Specifications apply as typical figures when V_{DD} = 5.25 V.

4/ Guaranteed by characterization.

5/ f_{SAMPLE} max = 600 kSPS.

6/ 3 V specifications apply from V_{DD} = 2.35 V to 3.6 V and 5 V specifications apply from V_{DD} = 4.75 V to 5.25 V.

7/ Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

8/ Mark/space ratio for the SCLK input is 40/60 to 60/40.

9/ Measured with the load circuit of figure 3 and defined as the time required for the output to cross 0.8 V to 2.0 V.

10/ t_8 is derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit in figure 3. The measured number is then extrapolated to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, is the true bus relinquish time of the part and is independent of the bus loading.

Case X

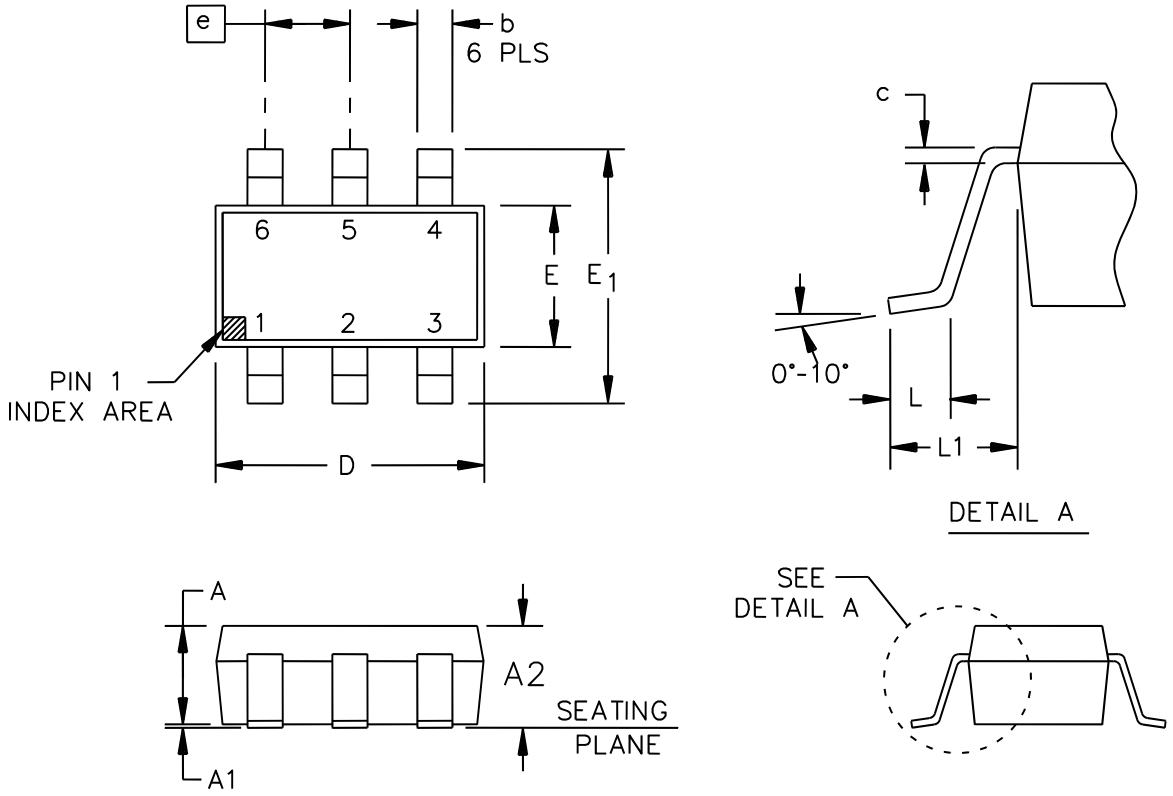

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/11611
		REV A	PAGE 10

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.035	0.051	0.90	1.30
A1	0.001	0.005	0.05	0.15
A2	0.037	0.057	0.95	1.45
b	0.011	0.019	0.30	0.50
c	0.003	0.007	0.08	0.20
D	0.110	0.118	2.80	3.00
E	0.059	0.069	1.50	1.70
E1	0.102	0.118	2.60	3.00
e	0.037 BSC		0.95 BSC	
L	0.013	0.021	0.35	0.55
L1	0.023 BSC		0.60 BSC	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-178-AB.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V_{DD}	Power supply input. The V_{DD} range for the device is from 2.35 V to 5.25 V.
2	GND	Analog ground. Ground reference point for all circuitry on the part. All analog input signals should be referred to this GND voltage.
3	V_{IN}	Analog input. Single ended analog input channel. The input range is 0 V to V_{DD}.
4	SCLK	Serial clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the device conversion process.
5	SDATA	Data out. Logic output. The conversion result is provided on this output as serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the device consists of four leading zeros followed by the 12 bits of conversion data; this is provided MSB first.
6	$\overline{CS}$	Chip select. Active low logic input. This input provides the dual function of initiating conversions on the device and framing the serial data transfer.

FIGURE 2. Terminal connections.

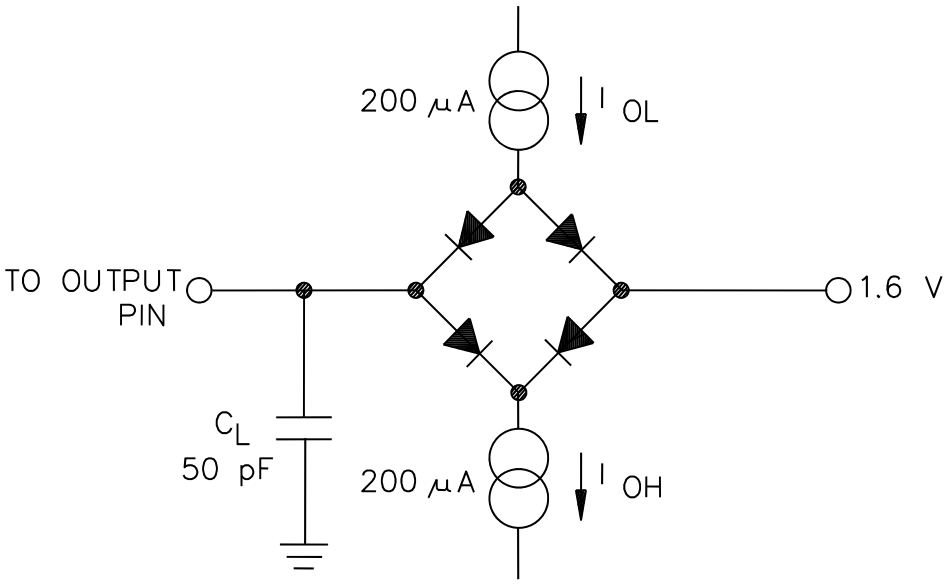

FIGURE 3. Load circuit for digital output timing specifications.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Linearity error (LSB) 2/	Vendor part number
V62/11611-01XE	24355	±1.5 maximum	AD7476SRTZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Linearity error refers to integral linearity error.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland