



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS operational amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/11610</u>   Drawing number	-	<u>01</u>   Device type (See 1.2.1)	<u>X</u>   Case outline (See 1.2.2)	<u>E</u>   Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	OPA365-EP	CMOS 50 MHz gain bandwidth operational amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	MO-178-AA	Plastic small outline surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage (V <sub>S</sub> ) .....	5.5 V
Signal input terminals, voltage .....	(-V) – 0.5 V to (+V) + 0.5 V 2/
Signal input terminals, current .....	±10 mA 2/
Output short circuit duration .....	Continuous 3/ 4/
Power dissipation (P <sub>D</sub> ) .....	56.25 mW
Junction temperature range (T <sub>J</sub> ) .....	+150°C
Storage temperature range (T <sub>STG</sub> ) .....	-65°C to +150°C
Electrostatic discharge (ESD) rating:	
Human body model (HBM) .....	4000 V
Charged device model (CDM) .....	1000 V
Machine model (MM) .....	200 V
Thermal resistance, junction to case (θ <sub>JC</sub> ) .....	69.4°C/W
Thermal resistance, junction to ambient (θ <sub>JA</sub> ) .....	200°C/W typical

1.4 Recommended operating conditions. 5/

Supply voltage range (V <sub>S</sub> ) .....	2.2 V to 5.5 V
Operating free-air temperature range (T <sub>A</sub> ) .....	-55°C to +125°C

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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Input terminals are diode clamped to the power supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- 3/ Short circuit to ground, one amplifier per package.
- 4/ Continuous output current greater than 20 mA for extended periods may affect product reliability.
- 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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## 2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107 or online at <http://www.jedec.org>)

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Offset voltage							
Input offset voltage	V <sub>OS</sub>		+25°C	01		200	μV
			-55°C to +125°C			450	
Input offset voltage drift	dV <sub>OS</sub> / dT		-55°C to +125°C	01	3 typical		μV / °C
Input offset voltage versus power supply	PSRR	V <sub>S</sub> = +2.2 V to +5.5 V	-55°C to +125°C	01		100	μV/V
Input bias current							
Input bias current	I <sub>B</sub>		+25°C	01		±10	pA
			-55°C		0.5 typical		
			+125°C		60 typical		
Input offset current	I <sub>OS</sub>		+25°C	01		±10	pA
Noise							
Input voltage noise	e <sub>n</sub>	f = 0.1 Hz to 10 Hz	+25°C	01	5 typical		μV <sub>PP</sub>
Input voltage noise density	e <sub>n</sub>	f = 100 kHz	+25°C	01	4.5 typical		nV / √Hz
Input current noise density	i <sub>n</sub>	f = 10 kHz	+25°C	01	4 typical		fA / √Hz
Input voltage range							
Common mode voltage range	V <sub>CM</sub>		-55°C to +125°C	01	(-V) - 0.1	(+V) + 0.1	V
Common mode rejection ratio	CMRR	(-V) - 0.1 V ≤ V <sub>CM</sub> ≤ (+V) + 0.1 V	-55°C to +125°C	01	96.5		dB
Input capacitance							
Differential			+25°C	01	6 typical		pF
Common mode			+25°C	01	2 typical		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Open loop gain							
Open loop voltage gain	A <sub>OL</sub>	100 mV < V <sub>O</sub> < (+V) – 100 mV, R <sub>L</sub> = 10 kΩ	-55°C to +125°C	01	96.5		dB
		200 mV < V <sub>O</sub> < (+V) – 200 mV, R <sub>L</sub> = 600 Ω	+25°C		100		
		200 mV < V <sub>O</sub> < (+V) – 200 mV, R <sub>L</sub> = 600 Ω	-55°C to +125°C		91		
Frequency response							
Gain bandwidth product	GBW		+25°C	01	50 typical		MHz
Slew rate	SR	V <sub>S</sub> = 5 V, G = +1	+25°C	01	25 typical		V/μs
Settling time	t <sub>S</sub>	0.1%, V <sub>S</sub> = 5 V, 4 V step, G = +1	+25°C	01	200 typical		ns
		0.01%, V <sub>S</sub> = 5 V, 4 V step, G = +1			300 typical		
Overload recovery time		V <sub>S</sub> = 5 V, V <sub>IN</sub> x gain > V <sub>S</sub>	+25°C	01	< 0.1 typical		μs
Total harmonic <u>3/</u> distortion + noise	THD + N	V <sub>S</sub> = 5 V, R <sub>L</sub> = 600 Ω, V <sub>O</sub> = 4 VPP, G = +1, f = 1 kHz	+25°C	01	0.0004 typical		%
Output							
Voltage output swing from rail		V <sub>S</sub> = 5.5 V, R <sub>L</sub> = 10 kΩ,	-55°C to +125°C	01		20	mV
Short circuit current <u>4/</u>	I <sub>SC</sub>		+25°C	01	±65 typical		mA
Capacitive load drive	C <sub>L</sub>		+25°C	01	100 typical		pF
Open loop output impedance		f = 1 MHz, I <sub>O</sub> = 0	+25°C	01	30 typical		Ω

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Power supply							
Specified voltage range	V <sub>S</sub>		-55°C to +125°C	01	2.2	5.5	V
Quiescent current per amplifier	I <sub>Q</sub>	I <sub>O</sub> = 0	+25°C	01		5	mA
			-55°C to +125°C			5.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V<sub>S</sub> = 2.2 V to 5.5 V, R<sub>L</sub> = 10 kΩ connected to V<sub>S</sub>/2, V<sub>CM</sub> = V<sub>S</sub>/2, and V<sub>OUT</sub> = V<sub>S</sub>/2.

3/ Third order filter, bandwidth 80 kHz at -3 dB.

4/ Continuous output current greater than 20 mA for extended periods may affect product reliability.

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Case X

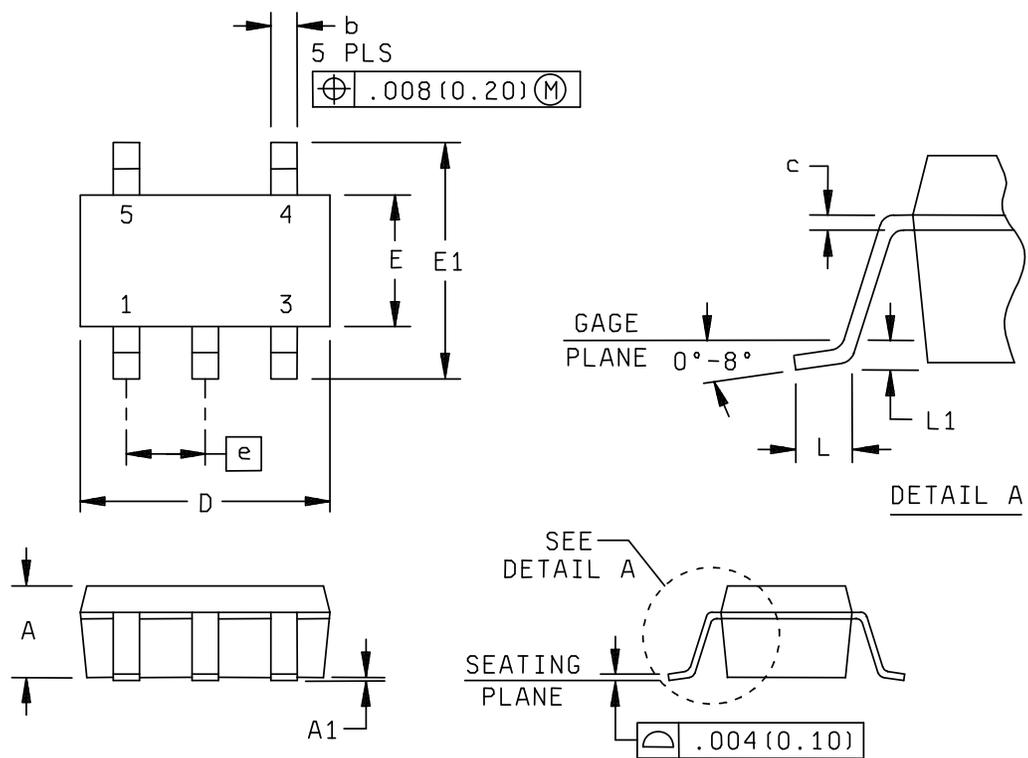


FIGURE 1. Case outline.

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Case X

Symbol	Dimensions			
	Inch		Millimeters	
	Min	Max	Min	Max
A	---	.057	---	1.45
A1	.000	.006	0.00	0.15
b	.011	.019	0.30	0.50
c	.003	.008	0.08	0.22
D	.108	.120	2.75	3.05
E	.057	.068	1.45	1.75
E1	.102	.118	2.60	3.00
e	.037 BSC		0.95 BSC	
L	.011	.022	0.30	0.55
L1	.009	---	0.25	---
n	5 leads		5 leads	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (.006 inch) per side.
3. Falls with JEDEC MO-178-AA.

FIGURE 1. Case outline – Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	V <sub>OUT</sub>
2	-V <sub>S</sub>
3	+INPUT
4	-INPUT
5	+V <sub>S</sub>

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/ 2/ 3/</u>	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/11610-01XE	01295	OUNM	OPA365AMDBVTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet , or use website [www.ti.com](http://www.ti.com).

3/ Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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