REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add lead finish “E” to the devices. - PHN	18-02-15	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					
REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A									
	PAGE		1	2	3	4	5	6	7	8	9	10									

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 11-01-19	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, PHASE DETECTOR/ FREQUENCY SYNTHESIZER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/11607**
	REV **A**	**PAGE** 1 **OF** 10

AMSC N/A

5962-V030-18

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Phase detector/ Frequency synthesizer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11607	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADF4002-EP	Phase detector/ Frequency synthesizer

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153	Lead Thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage referenced :
- AV_{DD} to GND 2/ ..... -0.3 V to +3.6 V
- AV_{DD} to DV_{DD} ..... -0.3 V to +0.3 V
- V_P to GND 2/ ..... -0.3 V to +5.8 V
- V_P to AV_{DD} ..... -0.3 V to +5.8 V

Digital I/O voltage to GND 2/ ..... -0.3 V to DV_{DD} + 0.3 V
Analog I/O voltage to GND 2/ ..... -0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $REF_{IN}B$ to GND 2/ ..... -0.3 V to AV_{DD} + 0.3 V
Ambient operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... 150°C
Lead temperature, soldering:
- Vapor phase (60 sec) ..... 215°C
- Infrared (15 sec) ..... 220°C

Transistor count:
- CMOS 6425
- Bipolar 303

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at https://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ GND = AGND = DGND = 0 V.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing diagrams. The timing diagrams shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
RF characteristics					
RF input sensitivity			-10	0	dBm
RF Input frequency	RF_{IN}	For RF_{IN} < 5 MHz, ensure slew rate (SR) > 4V/µs	5	400	MHz
REF_{IN} characteristics					
REF_{IN} input frequency		For REF_{IN} < 20 MHz, ensure SR > 50 V/µs	20	300	MHz
REF_{IN} input sensitivity 3/		Biased at $AV_{DD}/2$ (ac coupling ensures $AV_{DD}/2$ bias)	0.8	AV_{DD}	Vp-p
REF_{IN} input capacitance				10	pF
REF_{IN} input current				±100	µA
Phase Frequency detector					
Phase detector frequency 4/		ABP[2:1] = 00 (2.9 ns antibacklash pulse width)		104	MHz
Charge pump					
Sink/Source	I_{CP}				
High value		R_{SET} = 5.1 kΩ	5 TYP		mA
Low value			625 TYP		µA
Absolute accuracy		R_{SET} = 5.1 kΩ	2.5 TYP		%
R_{SET} range			3.0	11	kΩ
Three stage leakage	I_{CP}	T_A = 25°C	1 TYP		nA
I_{CP} vs V_{CP}		0.5 ≤ V_{CP} ≤ (V_P – 0.5 V)	1.5 TYP		%
Sink and source current matching		0.5 ≤ V_{CP} ≤ (V_P – 0.5 V)	2 TYP		%
I_{CP} vs temperature		V_{CP} = V_P/2	2 TYP		%
Logic inputs					
Input high voltage	V_{IH}		1.4		V
Input low voltage	V_{IL}			0.6	
Input current	I_{INH}, I_{INL}			±1	µA
Input capacitance	C_{IN}			10	pF
Logic outputs					
Output high voltage	V_{OH}	Open-drain output, 1 kΩ pull up resistor to 1.8 V CMOS output chosen	1.4		V
			V_{DD} – 0.4		
Output high current	I_{OH}			100	µA
Output low voltage	V_{OL}	I_{OL} = 500 µA		0.4	V
Power supplies					
AV_{DD}			2.7	3.3	V
DV_{DD}			AV_{DD}		V
V_P		AV_{DD} ≤ V_P ≤ 5.5 V	AV_{DD}	5.5	V
I_{DD} (AI_{DD} +DI_{DD}) 5/				6.0	mA
I_P		T_A = 25°C		0.4	
Power down mode		AI_{DD} + DI_{DD}	1 TYP		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Noise characteristics					
Normalized phase noise floor (PN_{SYNTH}) 6/ 7/		PLL loop BW = 500 kHz	-222 TYP		dBc/Hz
Normalized 1/f Noise (PN_{1_f}) 6/ 8/		Measured at 10 kHz offset, normalized to 1 GHz	-122 TYP		
Timing characteristics 9/ 10/					
Data to clock setup time	t_1		10		ns
Data to clock hold time	t_2		10		
Clock high duration	t_3		25		
Clock low duration	t_4		25		
Clock to LE setup time	t_5		10		
LE pulse width	t_6		20		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $AV_{DD} = DV_{DD} = 3$ V ±10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $-55°C \le T_A \le +125°C$, unless otherwise noted.

3/ $AV_{DD} = DV_{DD} = 3.0$ V.

4/ Guaranteed by design. Sample tested to ensure compliance.

5/ $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; $RF_{IN} = 350$ MHz. The current for any other setup (25°C, 3.0 V) in mA is given by 2.35 + 0.0046 (REF_{IN}) + 0.0062 (RF); RF frequency and REF_{IN} frequency in MHz.

6/ All phase noise measurements were performed with a Rohde&Schwarz FSU26 phase noise test system using the EVAL-ADF4002EBZ1 evaluation board and the ultralow noise, 100 MHz OCXO from Wenzel(Part No. 501-16843) as the PLL reference.

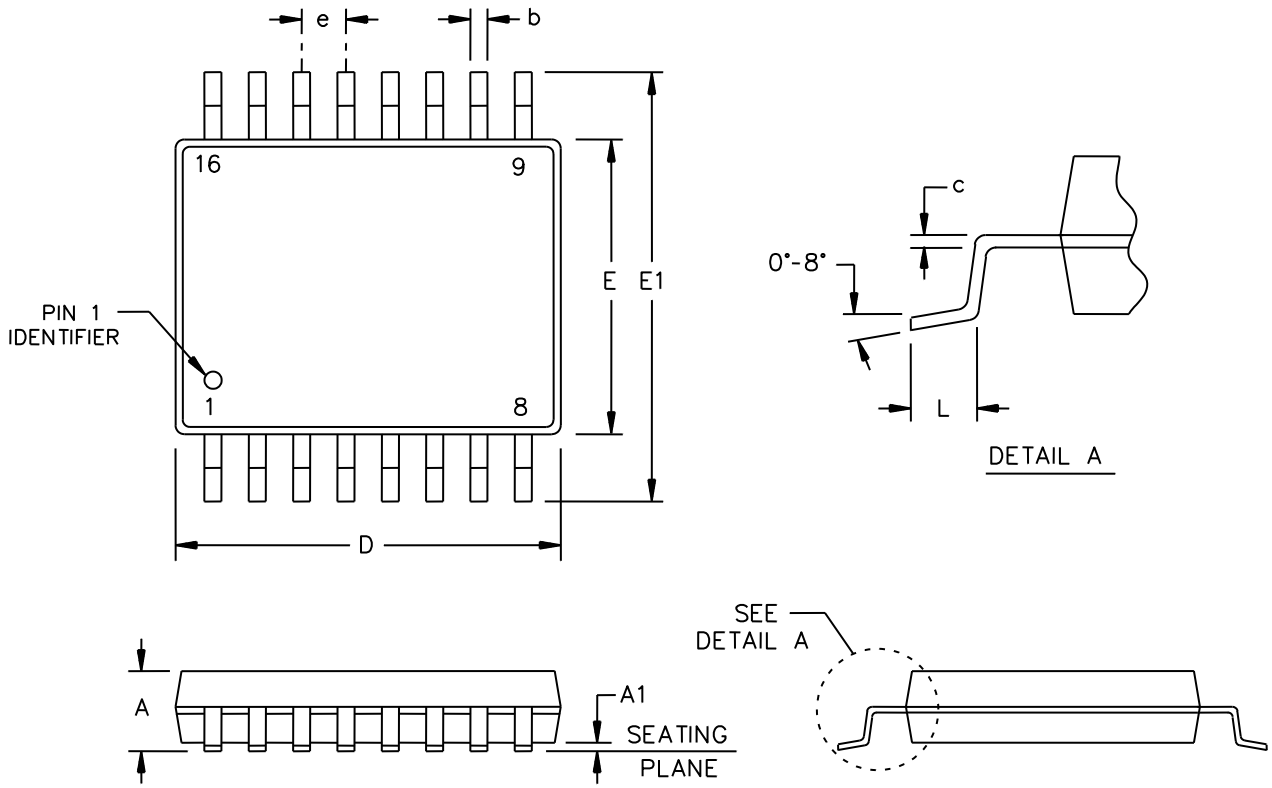
7/ The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. $PN_{SYTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.

8/ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by $PN = P_{1\_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$.

9/ $AV_{DD} = DV_{DD} = 3$ V ±10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $-40°C \le T_A \le +85°C$, unless otherwise noted.

10/ Guaranteed by design, but not production tested.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 TYP	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

FIGURE 1. Case outline.

Case X			
Pin No.	Pin Name	Pin No.	Pin Name
1	R_{SET}	9	DGND
2	CP	10	CE
3	CPGND	11	CLK
4	AGND	12	DATA
5	$RF_{IN}B$	13	LE
6	$RF_{IN}A$	14	MUXOUT
7	AV_{DD}	15	DV_{DD}
8	REF_{IN}	16	V_P

FIGURE 2. Terminal connections.

Case X PinNo.	**Pin Name**	**Description**
1	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is: $I_{CP\ MAX} = \frac{25.5}{R_{SET}}$ So, with R_{SET} = 5.1 kΩ, $I_{CP\ MAX}$ = 5 mA.
2	CP	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
3	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	AGND	Analog Ground. This is the ground return path of the RF input.
5	$RF_{IN}B$	Complementary Input to the RF Input. This pin must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	$RF_{IN}A$	Input to the RF Input. This small-signal input is ac-coupled to the external VCO.
7	AV_{DD}	Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to the AV_{DD} pin. AV_{DD} must be the same value as DV_{DD}.
8	REF_{IN}	Reference Input. This CMOS input has a nominal threshold of $AV_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	DGND	Digital Ground.
10	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking this pin high powers up the device, depending on the status of the Power-Down Bit PD1.
11	CLK	Serial Clock Input. The serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first; the two LSBs are the control bits. This input is a high impedance CMOS input.
13	LE	Load Enable. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits. This input is a high impedance CMOS input.
14	MUXOUT	Multiplexer Output. This output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	DV_{DD}	Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to the DV_{DD} pin. DV_{DD} must be the same value as AV_{DD}.
16	V_P	Charge Pump Power Supply. This should be greater than or equal to AV_{DD}. In systems where AV_{DD} is 3 V, V_P can be set to 5.5 V and used to drive a VCO with a tuning voltage of up to 5 V.

FIGURE 3. Pin Function Descriptions.

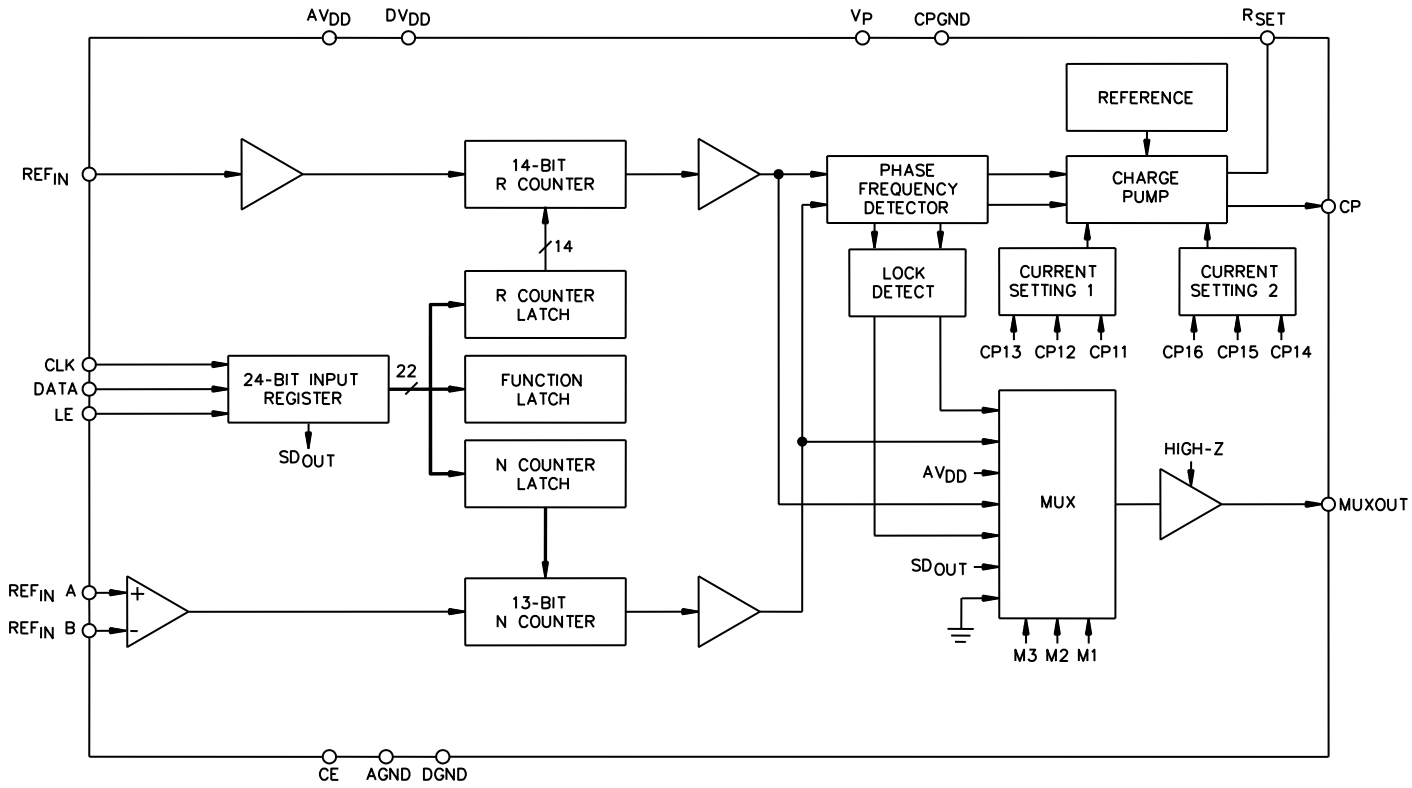


FIGURE 3. Functional block diagram.

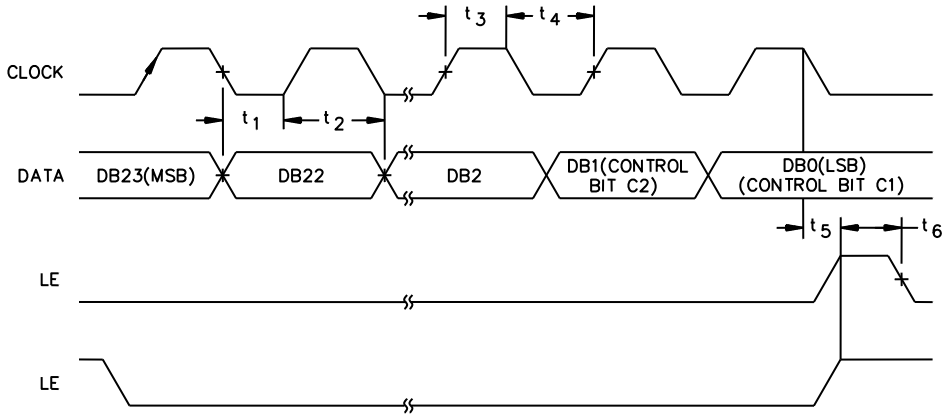


FIGURE 4. Timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11607-01XB	24355	ADF4002SRU-EP
V62/11607-01XE	24355	ADF4002SRUZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605