

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add lead finish "E" to the devices. - PHN	18-02-15	Thomas M. Hess



Prepared in accordance with ASME Y14.24

Vendor item drawing

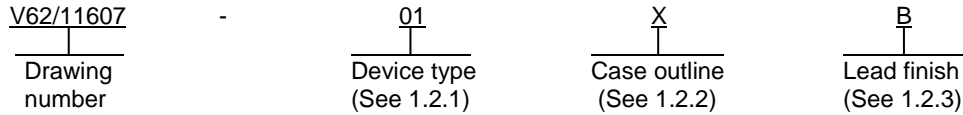
REV																				
PAGE																				
REV																				
PAGE																				
REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A								
	PAGE	1	2	3	4	5	6	7	8	9	10									

PMIC N/A	<b>PREPARED BY</b> Phu H. Nguyen	<b>DLA LAND AND MARITIME</b> <b>COLUMBUS, OHIO 43218-3990</b> <a href="http://www.landandmaritime.dla.mil/">http://www.landandmaritime.dla.mil/</a>	
Original date of drawing YY MM DD 11-01-19	<b>CHECKED BY</b> Phu H. Nguyen	<b>TITLE</b> MICROCIRCUIT, DIGITAL, PHASE DETECTOR/ FREQUENCY SYNTHESIZER, MONOLITHIC SILICON	
	<b>APPROVED BY</b> Thomas M. Hess		
	<b>SIZE</b> A	<b>CODE IDENT. NO.</b> 16236	<b>DWG NO.</b> <h1>V62/11607</h1>
	<b>REV</b>	A	<b>PAGE 1 OF 10</b>

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Phase detector/ Frequency synthesizer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADF4002-EP	Phase detector/ Frequency synthesizer

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MO-153	Lead Thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		REV    A	PAGE    2

1.3 Absolute maximum ratings. 1/

Voltage referenced :

AV <sub>DD</sub> to GND 2/	.....	-0.3 V to +3.6 V
AV <sub>DD</sub> to DV <sub>DD</sub>	.....	-0.3 V to +0.3 V
V <sub>P</sub> to GND 2/	.....	-0.3 V to +5.8 V
V <sub>P</sub> to AV <sub>DD</sub>	.....	-0.3 V to +5.8 V
Digital I/O voltage to GND 2/	.....	-0.3 V to DV <sub>DD</sub> + 0.3 V
Analog I/O voltage to GND 2/	.....	-0.3 V to V <sub>P</sub> + 0.3 V
REF <sub>IN</sub> , RF <sub>INA</sub> , REF <sub>INB</sub> to GND 2/	.....	-0.3 V to AV <sub>DD</sub> + 0.3 V
Ambient operating temperature range	.....	-55°C to +125°C
Storage temperature range	.....	-65°C to +150°C
Maximum junction temperature (T <sub>J</sub> )	.....	150°C
Lead temperature, soldering:		
Vapor phase (60 sec)	.....	215°C
Infrared (15 sec)	.....	220°C
Transistor count:		
CMOS	.....	6425
Bipolar	.....	303

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.  
 2/ GND = AGND = DGND = 0 V.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		REV    A	PAGE    3

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing diagrams. The timing diagrams shall be as shown in figure 4.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		REV    A	PAGE    4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
<b>RF characteristics</b>					
RF input sensitivity			-10	0	dBm
RF Input frequency	RF <sub>IN</sub>	For RF <sub>IN</sub> < 5 MHz, ensure slew rate (SR) > 4V/μs	5	400	MHz
<b>REF<sub>IN</sub> characteristics</b>					
REF <sub>IN</sub> input frequency		For REF <sub>IN</sub> < 20 MHz, ensure SR > 50 V/μs	20	300	MHz
REF <sub>IN</sub> input sensitivity 3/		Biased at AV <sub>DD</sub> /2 (ac coupling ensures AV <sub>DD</sub> /2 bias)	0.8	AV <sub>DD</sub>	Vp-p
REF <sub>IN</sub> input capacitance				10	pF
REF <sub>IN</sub> input current				±100	μA
<b>Phase Frequency detector</b>					
Phase detector frequency 4/		ABP[2:1] = 00 (2.9 ns antibacklash pulse width)		104	MHz
<b>Charge pump</b>					
Sink/Source	I <sub>CP</sub>				
High value		R <sub>SET</sub> = 5.1 kΩ		5 TYP	mA
Low value				625 TYP	μA
Absolute accuracy		R <sub>SET</sub> = 5.1 kΩ		2.5 TYP	%
R <sub>SET</sub> range			3.0	11	kΩ
Three stage leakage	I <sub>CP</sub>	T <sub>A</sub> = 25°C		1 TYP	nA
I <sub>CP</sub> vs V <sub>CP</sub>		0.5 ≤ V <sub>CP</sub> ≤ (V <sub>P</sub> - 0.5 V)		1.5 TYP	%
Sink and source current matching		0.5 ≤ V <sub>CP</sub> ≤ (V <sub>P</sub> - 0.5 V)		2 TYP	%
I <sub>CP</sub> vs temperature		V <sub>CP</sub> = V <sub>P</sub> /2		2 TYP	%
<b>Logic inputs</b>					
Input high voltage	V <sub>IH</sub>		1.4		V
Input low voltage	V <sub>IL</sub>			0.6	
Input current	I <sub>INH</sub> , I <sub>INL</sub>			±1	μA
Input capacitance	C <sub>IN</sub>			10	pF
<b>Logic outputs</b>					
Output high voltage	V <sub>OH</sub>	Open-drain output, 1 kΩ pull up resistor to 1.8 V CMOS output chosen	1.4		V
			V <sub>DD</sub> - 0.4		
Output high current	I <sub>OH</sub>			100	μA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 500 μA		0.4	V
<b>Power supplies</b>					
AV <sub>DD</sub>			2.7	3.3	V
DV <sub>DD</sub>			AV <sub>DD</sub>		V
V <sub>P</sub>		AV <sub>DD</sub> ≤ V <sub>P</sub> ≤ 5.5 V	AV <sub>DD</sub>	5.5	V
I <sub>DD</sub> (AI <sub>DD</sub> + DI <sub>DD</sub> ) 5/				6.0	mA
I <sub>P</sub>		T <sub>A</sub> = 25°C		0.4	
Power down mode		AI <sub>DD</sub> + DI <sub>DD</sub>		1 TYP	μA

See footnotes at end of table.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/11607
		REV A	PAGE 5

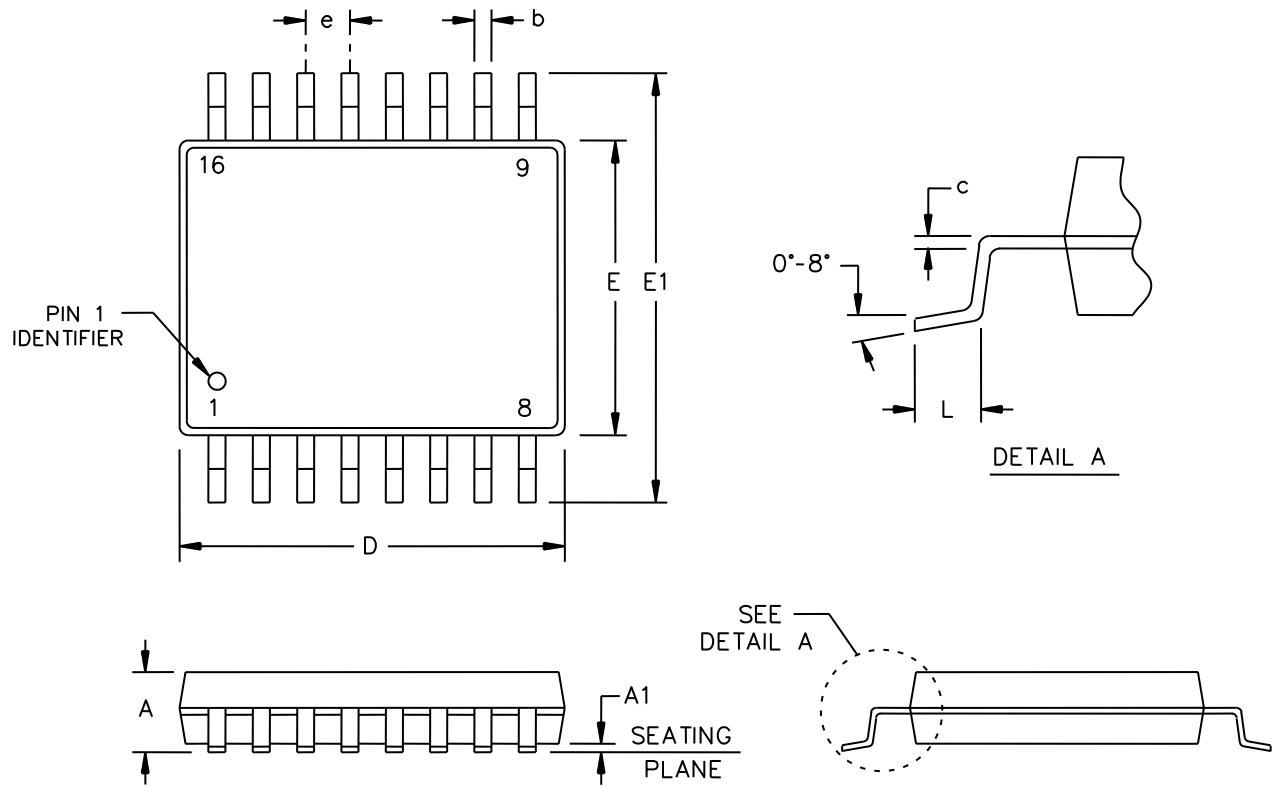
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
<b>Noise characteristics</b>					
Normalized phase noise floor (PN <sub>SYNTH</sub> ) 6/ 7/		PLL loop BW = 500 kHz	-222 TYP		dBc/Hz
Normalized 1/f Noise (PN <sub>1/f</sub> ) 6/ 8/		Measured at 10 kHz offset, normalized to 1 GHz	-122 TYP		
<b>Timing characteristics</b> 9/ 10/					
Data to clock setup time	t <sub>1</sub>		10		ns
Data to clock hold time	t <sub>2</sub>		10		
Clock high duration	t <sub>3</sub>		25		
Clock low duration	t <sub>4</sub>		25		
Clock to LE setup time	t <sub>5</sub>		10		
LE pulse width	t <sub>6</sub>		20		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/  $AV_{DD} = DV_{DD} = 3 V \pm 10\%$ ,  $AV_{DD} \leq V_P \leq 5.5 V$ ,  $AGND = DGND = CPGND = 0 V$ ,  $R_{SET} = 5.1 k\Omega$ , dBm referred to 50  $\Omega$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted.
- 3/  $AV_{DD} = DV_{DD} = 3.0 V$ .
- 4/ Guaranteed by design. Sample tested to ensure compliance.
- 5/  $T_A = 25^\circ C$ ;  $AV_{DD} = DV_{DD} = 3 V$ ;  $RF_{IN} = 350 MHz$ . The current for any other setup (25°C, 3.0 V) in mA is given by  $2.35 + 0.0046 (RF_{IN}) + 0.0062 (RF)$ ; RF frequency and  $RF_{IN}$  frequency in MHz.
- 6/ All phase noise measurements were performed with a Rohde&Schwarz FSU26 phase noise test system using the EVAL-ADF4002EBZ1 evaluation board and the ultralow noise, 100 MHz OCXO from Wenzel (Part No. 501-16843) as the PLL reference.
- 7/ The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting  $20 \log N$  (where N is the N divider value) and  $10 \log F_{PPFD}$ .  $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PPFD} - 20 \log N$ .
- 8/ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency,  $f_{RF}$ , and at a frequency offset, f, is given by  $PN = P_{1/f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{RF}/1 \text{ GHz})$ .
- 9/  $AV_{DD} = DV_{DD} = 3 V \pm 10\%$ ,  $AV_{DD} \leq V_P \leq 5.5 V$ ,  $AGND = DGND = CPGND = 0 V$ ,  $R_{SET} = 5.1 k\Omega$ , dBm referred to 50  $\Omega$ ,  $-40^\circ C \leq T_A \leq +85^\circ C$ , unless otherwise noted.
- 10/ Guaranteed by design, but not production tested.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/11607
		REV A	PAGE 6

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 TYP	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

FIGURE 1. Case outline.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		REV    A	PAGE    7

Case X			
Pin No.	Pin Name	Pin No.	Pin Name
1	R <sub>SET</sub>	9	DGND
2	CP	10	CE
3	CPGND	11	CLK
4	AGND	12	DATA
5	RF <sub>INB</sub>	13	LE
6	RF <sub>INA</sub>	14	MUXOUT
7	AV <sub>DD</sub>	15	DV <sub>DD</sub>
8	REF <sub>IN</sub>	16	V <sub>P</sub>

FIGURE 2. Terminal connections.

Case X PinNo.	Pin Name	Description
1	R <sub>SET</sub>	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R <sub>SET</sub> pin is 0.66 V. The relationship between I <sub>CP</sub> and R <sub>SET</sub> is: $I_{CP\ MAX} = \frac{25.5}{R_{SET}}$ So, with R <sub>SET</sub> = 5.1 kΩ, I <sub>CP</sub> MAX = 5 mA.
2	CP	Charge Pump Output. When enabled, this provides ±I <sub>CP</sub> to the external loop filter, which in turn drives the external VCO.
3	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	AGND	Analog Ground. This is the ground return path of the RF input.
5	RF <sub>INB</sub>	Complementary Input to the RF Input. This pin must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	RF <sub>INA</sub>	Input to the RF Input. This small-signal input is ac-coupled to the external VCO.
7	AV <sub>DD</sub>	Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to the AV <sub>DD</sub> pin. AV <sub>DD</sub> must be the same value as DV <sub>DD</sub> .
8	REF <sub>IN</sub>	Reference Input. This CMOS input has a nominal threshold of AV <sub>DD</sub> /2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	DGND	Digital Ground.
10	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking this pin high powers up the device, depending on the status of the Power-Down Bit PD1.
11	CLK	Serial Clock Input. The serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first; the two LSBs are the control bits. This input is a high impedance CMOS input.
13	LE	Load Enable. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits. This input is a high impedance CMOS input.
14	MUXOUT	Multiplexer Output. This output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	DV <sub>DD</sub>	Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to the DV <sub>DD</sub> pin. DV <sub>DD</sub> must be the same value as AV <sub>DD</sub> .
16	V <sub>P</sub>	Charge Pump Power Supply. This should be greater than or equal to AV <sub>DD</sub> . In systems where AV <sub>DD</sub> is 3 V, V <sub>P</sub> can be set to 5.5 V and used to drive a VCO with a tuning voltage of up to 5 V.

FIGURE 3. Pin Function Descriptions.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		REV    A	PAGE    8



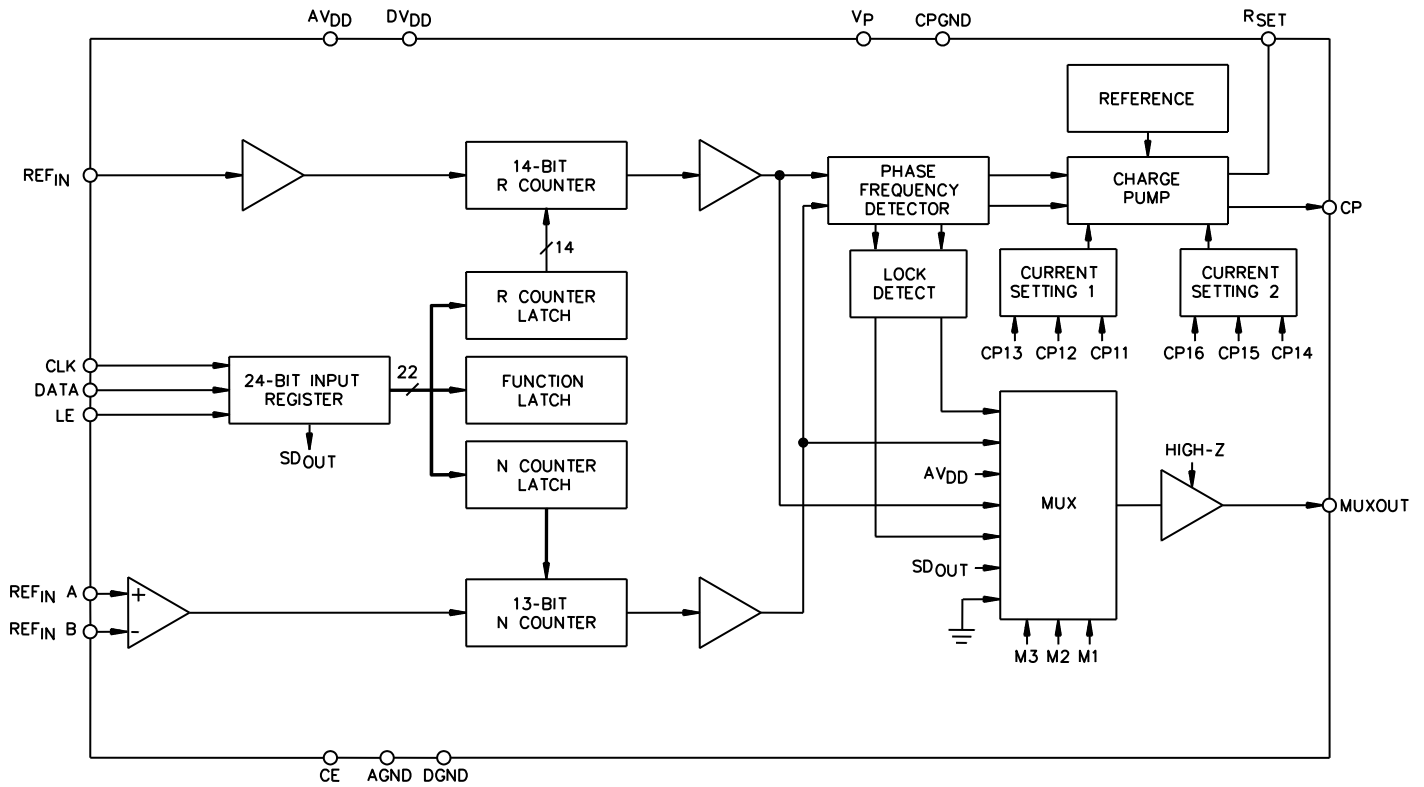


FIGURE 3. Functional block diagram.

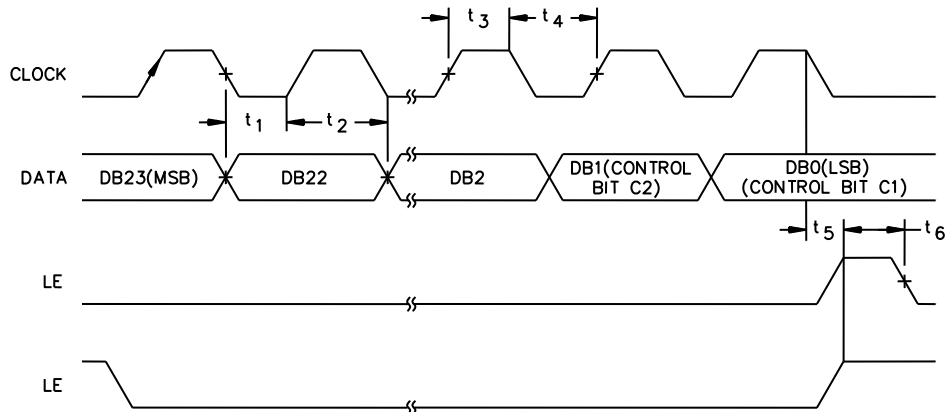


FIGURE 4. Timing diagram.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		<b>REV    A</b>	<b>PAGE    9</b>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <sup>1/</sup>	Device manufacturer CAGE code	Vendor part number
V62/11607-01XB	24355	ADF4002SRU-EP
V62/11607-01XE	24355	ADF4002SRUZ-EP-RL7

<sup>1/</sup> The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices  
 Rt 1 Industrial Park  
 PO Box 9106  
 Norwood, MA 02062  
 Point of contact: 7910 Triad Center Drive  
 Greensboro, NC 27409-9605

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11607</b>
		<b>REV     A</b>	<b>PAGE    10</b>