

| REVISIONS | | | |
|-----------|---|----------|----------------|
| LTR | DESCRIPTION | DATE | APPROVED |
| A | Add lead finish "E" to the devices. - PHN | 18-02-15 | Thomas M. Hess |
| | | | |
| | | | |



Prepared in accordance with ASME Y14.24

Vendor item drawing

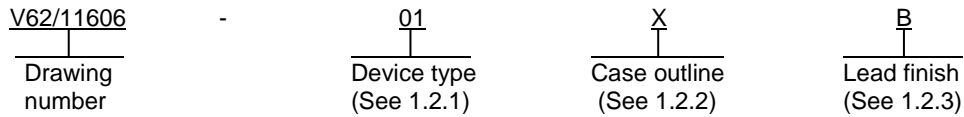
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| REV STATUS OF PAGES | REV | A | A | A | A | A | A | A | A | A | A | A | A | A | | | | | | |
| | PAGE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | |

| | | | |
|--|--------------------------------------|---|------------------------------------|
| PMIC N/A | PREPARED BY Phu H. Nguyen | DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/ | |
| Original date of drawing YY MM DD 11-01-19 | CHECKED BY Phu H. Nguyen | TITLE MICROCIRCUIT, DIGITAL, PLL FREQUENCY SYNTHESIZER, MONOLITHIC SILICON | |
| | APPROVED BY Thomas M. Hess | | |
| | SIZE A | CODE IDENT. NO. 16236 | DWG NO. V62/11606 |
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance PLL frequency synthesizer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

| <u>Device type</u> | <u>Generic</u> | <u>Circuit function</u> |
|--------------------|----------------|---------------------------|
| 01 | ADF4106-EP | PLL frequency synthesizer |

1.2.2 Case outline(s). The case outlines are as specified herein.

| <u>Outline letter</u> | <u>Number of pins</u> | <u>JEDEC PUB 95</u> | <u>Package style</u> |
|-----------------------|-----------------------|---------------------|--|
| X | 16 | JEDEC MO-153 | Lead Thin Shrink Small Outline Package |
| Y | 20 | JEDEC MO-220 | Lead Lead Frame Chip Scale Package |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| <u>Finish designator</u> | <u>Material</u> |
|--------------------------|----------------------|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| F | Tin-lead alloy |
| Z | Other |

| | | | |
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1.3 Absolute maximum ratings. 1/

Voltage referenced :

| | |
|---|-----------------------------------|
| AV _{DD} to GND 2/ | -0.3 V to +7.0 V |
| AV _{DD} to DV _{DD} | -0.3 V to +0.3 V |
| V _P to GND | -0.3 V to +5.8 V |
| V _P to AV _{DD} | -0.3 V to +5.8 V |
| Digital I/O voltage to GND | -0.3 V to V _{DD} + 0.3 V |
| Analog I/O voltage to GND | -0.3 V to V _P + 0.3 V |
| REF _{IN} , RF _{INA} , REF _{INB} to GND | -0.3 V to V _{DD} + 0.3 V |
| Ambient operating temperature range | -55°C to +125°C |
| Storage temperature range | -65°C to +150°C |
| Maximum junction temperature (T _J) | 150°C |
| Thermal impedance,(θ _{JA}): | |
| Case outline X | 112°C /W |
| Case outline Y (Paddle soldered) | 30.4°C /W |
| Reflow soldering: | |
| Peak temperature | 260°C |
| Time at peak temperature | 40 sec |
| Transistor count: | |
| CMOS | 6425 |
| Bipolar | 303 |

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
 2/ GND = AGND = DGND = 0 V.

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3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing diagrams. The timing diagrams shall be as shown in figure 4.

| | | | |
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TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Test conditions 2/ unless otherwise specified | Limits | | Unit |
|--|-------------------------------------|---|-----------------------|-----------------|------|
| | | | Min | Max | |
| RF characteristics | | | | | |
| RF Input frequency | RF _{IN} | For lower frequency, ensure slew rate (SR) > 320/μs | 0.5 | 6.0 | GHz |
| RF input sensitivity | | | -10 | 0 | dBm |
| Maximum allowable prescaler output frequency 3/ | | P = 8 | | 300 | MHz |
| | | P = 10 | | 325 | MHz |
| REF_{IN} characteristics | | | | | |
| REF _{IN} input frequency | | For f < 20 MHz, ensure SR > 50 V/μs | 20 | 300 | MHz |
| REF _{IN} input sensitivity 4/ | | Biased at AV _{DD} /2 ⁴ | 0.8 | V _{DD} | Vp-p |
| REF _{IN} input capacitance | | | | 10 | pF |
| REF _{IN} input current | | | | ±100 | μA |
| Phase detector | | | | | |
| Phase detector frequency 6/ | | ABP = 0, 0 (2.9 ns antibacklash pulse width) | | 104 | MHz |
| Charge pump | | | | | |
| Sink/Source | I _{CP} | | | | |
| High value | | With R _{SET} = 5.1 kΩ | 5 TYP | | mA |
| Low value | | | 625 TYP | | μA |
| Absolute accuracy | | With R _{SET} = 5.1 kΩ | 2.5 TYP | | % |
| R _{SET} range | | | 3.0 | 11 | kΩ |
| Three stage leakage | I _{CP} | 1 nA typical; T _A = 25°C | | 2 | nA |
| Sink and source current matching | | 0.5 ≤ V _{CP} ≤ V _P - 0.5 V | 2 TYP | | % |
| I _{CP} vs V _{CP} | | 0.5 ≤ V _{CP} ≤ V _P - 0.5 V | 1.5 TYP | | % |
| I _{CP} vs temperature | | V _{CP} = V _P /2 | 2 TYP | | % |
| Logic inputs | | | | | |
| Input high voltage | V _{IH} | | 1.4 | | V |
| Input low voltage | V _{IL} | | | 0.6 | |
| Input current | I _{INH} , I _{INL} | | | ±1 | μA |
| Input capacitance | C _{IN} | | | 10 | pF |
| Logic outputs | | | | | |
| Output high voltage | V _{OH} | Open-drain output chosen, 1 kΩ pull up resistor to 1.8 V CMOS output chosen | 1.4 | | V |
| | | | V _{DD} - 0.4 | | |
| Output high current | I _{OH} | | | 100 | μA |
| Output low voltage | V _{OL} | I _{OL} = 500 μA | | 0.4 | V |
| Power supplies | | | | | |
| AV _{DD} | | | 2.7 | 3.3 | V |
| DV _{DD} | | | AV _{DD} | | V |
| V _P | | AV _{DD} ≤ V _P ≤ 5.5 V | AV _{DD} | 5.5 | V |
| I _{DD} (A _{IDD} + D _{IDD}) 7/ | | 9.0 mA TYP | | 11 | mA |
| I _{DD} (A _{IDD} + D _{IDD}) 8/ | | 9.5 mA TYP | | 11.5 | |
| I _{DD} (A _{IDD} + D _{IDD}) 9/ | | 10.5 mA TYP | | 13 | |
| I _P | | T _A = 25°C | | 0.4 | |
| Power down mode (A _{IDD} + D _{IDD}) 10/ | | | 10 TYP | | μA |

See footnotes at end of table.

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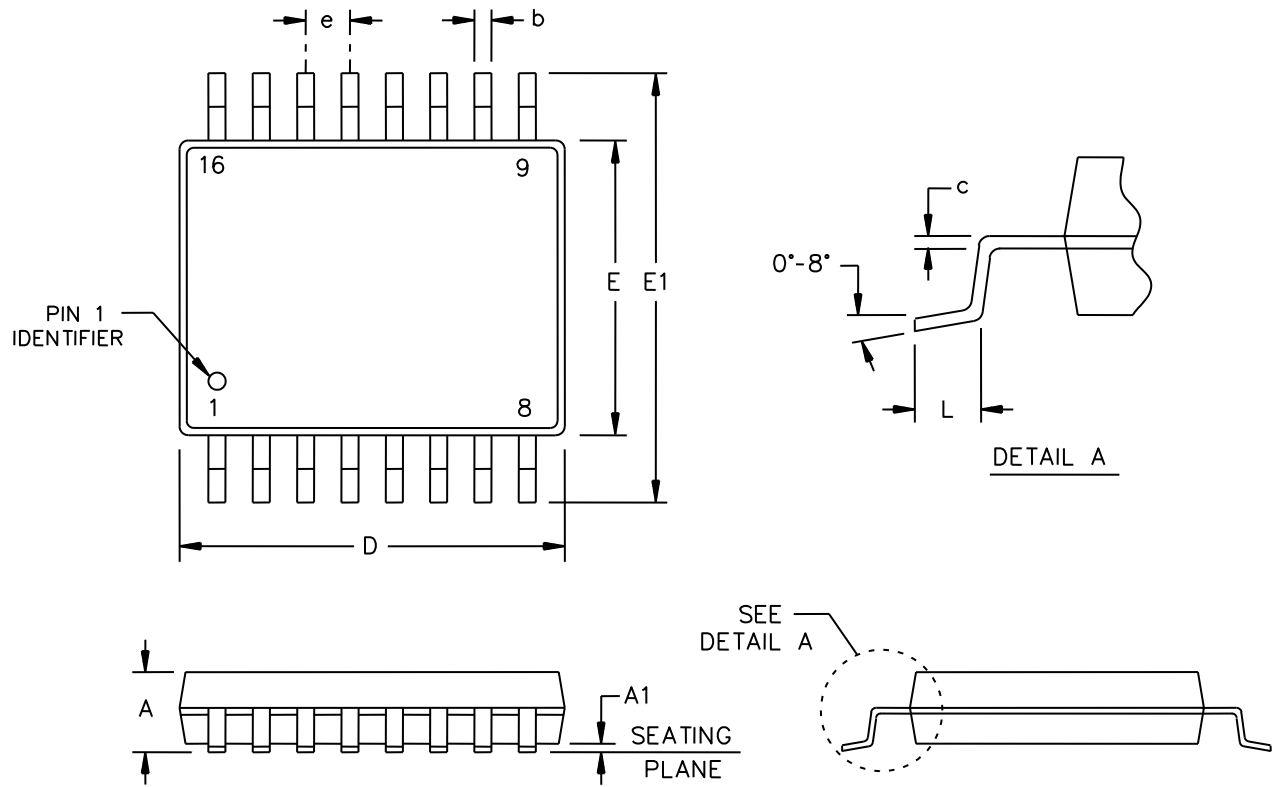
TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Test conditions 2/ unless otherwise specified | Limits | | Unit |
|---|----------------|---|-----------|-----|--------|
| | | | Min | Max | |
| Noise characteristics | | | | | |
| Normalized phase noise floor (PN _{SYNTH}) 11/ | | PLL loop BW = 500 kHz | -223 TYP | | dBc/Hz |
| Normalized 1/f Noise (PN _{1/f}) 12/ | | Measured at 10 kHz offset, normalized to 1 GHz VCO output | -122 TYP | | |
| Phase noise performance 13/ | | | | | dBc |
| 900 MHz 14/ | | 1 kHz offset and 200 kHz PFD frequency | -92.5 TYP | | |
| 5800 MHz 15/ | | 1 kHz offset and 200 kHz PFD frequency | -76.5 TYP | | |
| 5800 MHz 16/ | | 1 kHz offset and 1 MHz PFD frequency | -83.5 TYP | | |
| Spurious signals | | | | | dBc |
| 900 MHz 14/ | | 200 kHz/400 kHz and 200 kHz PDF frequency | -90 | -92 | |
| 5800 MHz 15/ | | 200 kHz/400 kHz and 200 kHz PDF frequency | -65 | -70 | |
| 5800 MHz 16/ | | 1 MHz/2 MHz and 1 MHz PDF frequency | -70 | -75 | |
| Timing characteristics 17/ | | | | | |
| Data to clock setup time | t ₁ | | 10 | | ns |
| Data to clock hold time | t ₂ | | 10 | | |
| Clock high duration | t ₃ | | 25 | | |
| Clock low duration | t ₄ | | 25 | | |
| Clock to LE setup time | t ₅ | | 10 | | |
| LE pulse width | t ₆ | | 20 | | |

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ AV_{DD} = DV_{DD} = 3 V ±10%, AV_{DD} ≤ V_P ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.
- 3/ This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
- 4/ AV_{DD} = DV_{DD} = 3.0 V.
- 5/ AC coupling ensures AV_{DD}/2 bias.
- 6/ Guaranteed by design. Sample tested to ensure compliance.
- 7/ T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; P = 16; RF_{IN} = 900 MHz.
- 8/ T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; P = 16; RF_{IN} = 2.0 GHz.
- 9/ T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; P = 32; RF_{IN} = 6.0 GHz.
- 10/ T_A = 25°C; AV_{DD} = DV_{DD} = 3.3 V; R = 16383; A = 63; B = 891; P = 32; RF_{IN} = 6.0 GHz.
- 11/ The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. PN_{SYNTH} = PN_{TOT} - 10 log F_{PFD} - 20 log N.
- 12/ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by PN = P_{1/f} + 10log(10 kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
- 13/ The phase noise is measured with the EVAL-ADF4106-EB1 evaluation board and the Agilent E4440A spectrum analyzer. The spectrum analyzer provides the REF_{IN} for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).
- 14/ f_{REFIN} = 10 MHz, f_{PFD} = 200 kHz; offset frequency = 1 kHz, f_{RF} = 900 MHz; N = 4500; loop B/W = 20 kHz.
- 15/ f_{REFIN} = 10 MHz, f_{PFD} = 200 kHz; offset frequency = 1 kHz, f_{RF} = 5800 MHz; N = 29,000; loop B/W = 20 kHz.
- 16/ f_{REFIN} = 10 MHz, f_{PFD} = 1 MHz; offset frequency = 1 kHz, f_{RF} = 5800 MHz; N = 5800; loop B/W = 100 kHz.
- 17/ AV_{DD} = DV_{DD} = 3 V ±10%, AV_{DD} ≤ V_P ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, -40°C ≤ T_A ≤ +85°C, unless otherwise noted.

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Case X

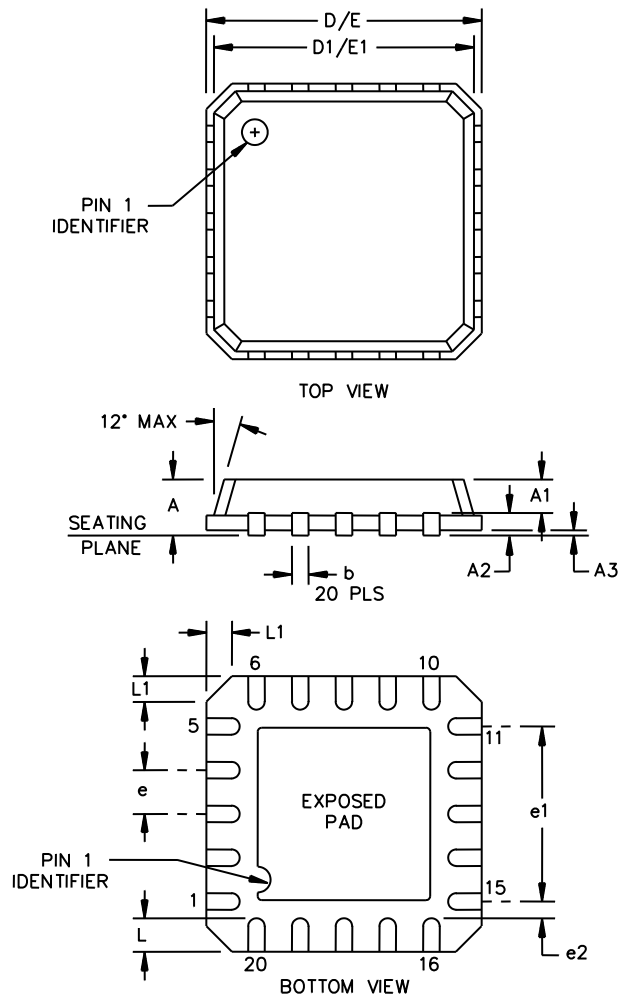


| Dimensions | | | | | |
|------------|-------------|------|--------|-------------|------|
| Symbol | Millimeters | | Symbol | Millimeters | |
| | Min | Max | | Min | Max |
| A | | 1.20 | E | 4.30 | 4.50 |
| A1 | 0.05 | 0.15 | E1 | 6.40 TYP | |
| b | 0.19 | 0.30 | e | 0.65 BSC | |
| c | 0.09 | 0.20 | L | 0.45 | 0.75 |
| D | 4.90 | 5.10 | | | |

FIGURE 1. Case outline.

| | | | |
|---|-------------------|---------------------------------|------------------------------|
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Case Y



| Dimensions | | | | | |
|------------|-------------|------|--------|-------------|------|
| Symbol | Millimeters | | Symbol | Millimeters | |
| | Min | Max | | Min | Max |
| A | 0.80 | 1.00 | D1/E1 | 3.75 BSC | |
| A1 | | 0.80 | e | 0.50 BSC | |
| A2 | 0.20 REF | | e1 | 1.95 | 2.25 |
| A3 | | 0.05 | e2 | 0.25 | |
| b | 0.18 | 0.30 | L | 0.50 | 0.75 |
| D/E | 4.00 BSC | | L1 | | 0.60 |

FIGURE 1. Case outline - Continued.

| | | | |
|---|-------------------|---------------------------------|------------------------------|
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| Case X | | | | Case Y | | | |
|---------|-------------------|---------|------------------|---------|-------------------|---------|------------------|
| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
| 1 | R _{SET} | 9 | DGND | 1 | CPGND | 11 | CE |
| 2 | CP | 10 | CE | 2 | AGND | 12 | CLK |
| 3 | CPGND | 11 | CLK | 3 | AGND | 13 | DATA |
| 4 | AGND | 12 | DATA | 4 | RF _{INB} | 14 | LE |
| 5 | RF _{INB} | 13 | LE | 5 | RF _{INA} | 15 | MUXOUT |
| 6 | RF _{INA} | 14 | MUXOUT | 6 | AV _{DD} | 16 | DV _{DD} |
| 7 | AV _{DD} | 15 | DV _{DD} | 7 | AV _{DD} | 17 | DV _{DD} |
| 8 | REF _{IN} | 16 | V _P | 8 | REF _{IN} | 18 | V _P |
| | | | | 9 | DGND | 19 | R _{SET} |
| | | | | 10 | DGND | 20 | CP |

FIGURE 2. Terminal connections.

| Case X PinNo. | Case Y Pin No. | Pin Name | Description |
|------------------|-------------------|-------------------|--|
| 1 | 19 | R _{SET} | Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R _{SET} pin is 0.66 V. The relationship between I _{CP} and R _{SET} is: $I_{CP\ MAX} = \frac{25.5}{R_{SET}}$ So, with R _{SET} = 5.1 kΩ, I _{CP} MAX = 5 mA. |
| 2 | 20 | CP | Charge Pump Output. When enabled, this provides ±I _{CP} to the external loop filter, which in turn drives the external VCO. |
| 3 | 1 | CPGND | Charge Pump Ground. This is the ground return path for the charge pump. |
| 4 | 2, 3 | AGND | Analog Ground. This is the ground return path of the prescaler. |
| 5 | 4 | RF _{INB} | Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. |
| 6 | 5 | RF _{INA} | Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO. |
| 7 | 6, 7 | AV _{DD} | Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV _{DD} must be the same value as DV _{DD} . |
| 8 | 8 | REF _{IN} | Reference Input. This is a CMOS input with a nominal threshold of V _{DD} /2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled. |
| 9 | 9, 10 | DGND | Digital Ground. |
| 10 | 11 | CE | Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2. |
| 11 | 12 | CLK | Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input. |
| 12 | 13 | DATA | Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input. |
| 13 | 14 | LE | Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches with the latch being selected using the control bits. |
| 14 | 15 | MUXOUT | The multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally. |
| 15 | 16, 17 | DV _{DD} | Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV _{DD} must be the same value as AV _{DD} . |
| 16 | 18 | V _P | Charge Pump Power Supply. This should be greater than or equal to V _{DD} . In systems where V _{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5 V. |
| | | EP | Exposed Pad. The exposed pad must be connected to AGND. |

FIGURE 3. Pin Function Descriptions.

| | | | |
|---|-------------------|---------------------------------|------------------------------|
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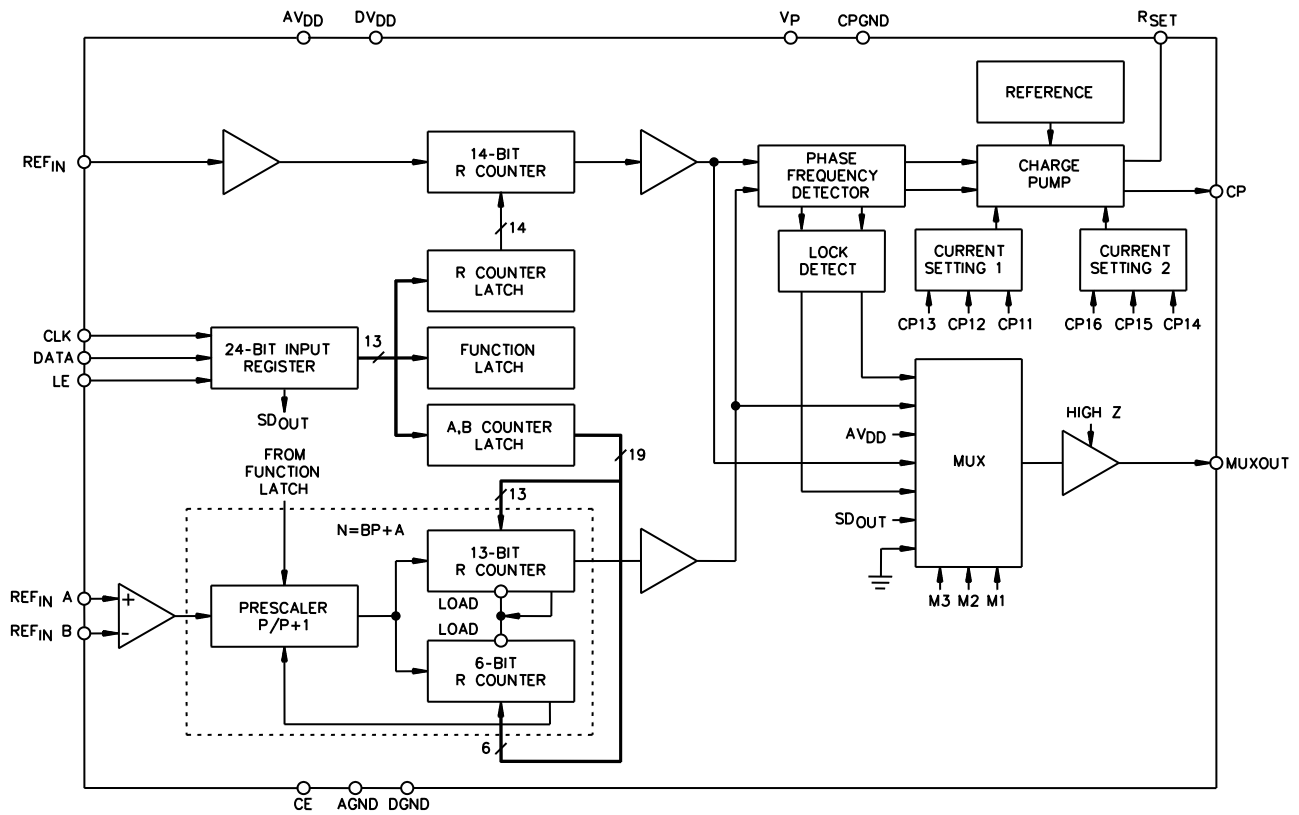


FIGURE 3. Functional block diagram.

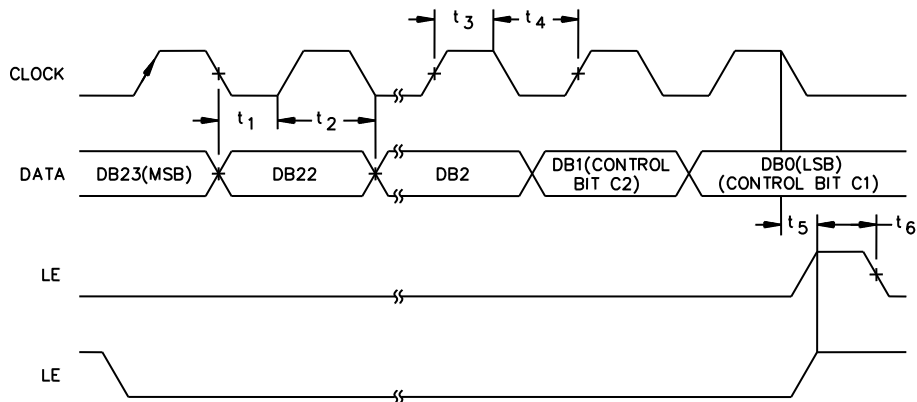


FIGURE 4. Timing diagram.

| | | | |
|---|-------------------|---------------------------------|------------------------------|
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

| Vendor item drawing administrative control number ^{1/} | Device manufacturer CAGE code | Vendor part number |
|---|-------------------------------|--------------------|
| V62/11606-01XB | 24355 | ADF4106-SRU-EP-R7 |
| V62/11606-01XE | 24355 | ADF4106-SRUZ-EP |
| | | ADF4106-SRUZ-EP-R7 |
| V62/11606-01YB | 24355 | ADF4106-SCPZ-EP-R7 |

^{1/} The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Rt 1 Industrial Park
 PO Box 9106
 Norwood, MA 02062
 Point of contact: 7910 Triad Center Drive
 Greensboro, NC 27409-9605

| | | | |
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