

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Change in Table I for new re-design. - PHN	13-03-12	Thomas M. Hess
B	Add lead finish E device. Under paragraph 6.3, add transportation mode and quantity column. Under paragraph 6.3, make correction to Source of supply Point of contact address to state Limerick Ireland. - ro	18-05-07	Charles F. Saffle



Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
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PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="http://www.dla.mil/landandmaritime">http://www.dla.mil/landandmaritime</a>
Original date of drawing YY-MM-DD  10-12-14	CHECKED BY Phu H. Nguyen	TITLE
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, DIGITAL, NONVOLATILE MEMORY, DUAL 1024-POSITION DIGITAL POTENTIOMETER, MONOLITHIC SILICON
	SIZE <b>A</b>	CODE IDENT. NO. <b>16236</b>
	REV <b>B</b>	DWG NO. <b>V62/11605</b>
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance non volatile memory, dual 1024-position digital potentiometer microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/11605</u>	-	<u>01</u>	<u>X</u>	<u>B</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	AD5235-EP	Nonvolatile memory, dual 1024-position digital potentiometer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MO-153	Small outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Voltage referenced :	
V <sub>DD</sub> to GND .....	-0.3 V to +7.0 V
V <sub>SS</sub> to GND .....	+0.3 V to -7.0 V
V <sub>DD</sub> to V <sub>SS</sub> .....	7.0 V
V <sub>A</sub> , V <sub>B</sub> , V <sub>W</sub> to GND .....	V <sub>SS</sub> – 0.3 V to V <sub>DD</sub> + 0.3 V
Current referenced, I <sub>A</sub> , I <sub>B</sub> , I <sub>W</sub> :	
Pulsed 2/ .....	±2.5 mA
Continuous .....	±1.1 mA
Digital input and output voltage to GND .....	-0.3 V to V <sub>DD</sub> + 0.3 V
Ambient operating temperature range 3/ .....	-40°C to +125°C
Storage temperature range .....	-65°C to +150°C
Maximum junction temperature (T <sub>J</sub> ) .....	150°C
Lead temperature, soldering:	
Vapor phase (60 seconds) .....	215°C
Infrared (15 seconds) .....	220°C
Thermal resistance, junction to ambient (θ <sub>JA</sub> ) .....	150°C /W
Thermal resistance, junction to case (θ <sub>JC</sub> ) .....	28°C /W
Package power dissipation .....	(T <sub>J max</sub> – T <sub>A</sub> ) / θ <sub>JA</sub>

- 
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B and W terminals at a given resistance.
- 3/ Includes programming of nonvolatile memory.

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## 2. APPLICABLE DOCUMENTS

### JEDEC Solid State Technology Association

- JESD51-2a – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JESD22a117 – Electrical Erasable programmable ROM (EEPROM) Program/Erase endurance and data retention test.

(Applications for copies should be addressed to the JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.or online at <https://www.jedec.org>).

## 3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal functions. The terminal functions shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Timing diagrams. The timing diagrams shall be as shown in figures 5 and 6.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits			Unit
			Min	Typ 3/	Max	
<b>DC characteristic-RHEOSTAT mode (All RDACs)</b>						
Resistor differential nonlinearity 4/	R-DNL	R <sub>WB</sub>	-1		+1	LSB
Resistor integral nonlinearity 4/	R-INL	R <sub>WB</sub>	-2		+2	LSB
Nominal resistor tolerance	$\Delta R_{AB}/R_{AB}$	Code = full scale	-8		+8	%
Resistance temperature coefficient	$(\Delta R_{AB}/R_{AB})\Delta T \times 10^6$			35		ppm/°C
Wipe resistance	R <sub>W</sub>	I <sub>W</sub> = 1 V/R <sub>WB</sub> , V <sub>DD</sub> = 5 V, code = half scale		30	65	Ω
		I <sub>W</sub> = 1 V/R <sub>WB</sub> , V <sub>DD</sub> = 3 V, code = half scale		50		
Nominal resistance match	R <sub>AB1</sub> /R <sub>AB2</sub>	Code = full scale, T <sub>A</sub> = 25°C		±0.1		%
<b>DC characteristics – Potentiometer divider mode (All RDACs)</b>						
Resolution	N				10	Bits
Differential nonlinearity 5/	DNL		-1		+1	LSB
Integral nonlinearity 5/	INL		-1		+1	LSB
Voltage divider temperature coefficient	$(\Delta V_W/V_W)\Delta T \times 10^6$	Code = half scale		15		ppm/°C
Full scale error	V <sub>WFSE</sub>	Code = full scale	-7		0	LSB
Zero scale error	V <sub>WZSE</sub>	Code = zero scale	0		5	LSB
<b>Resistor terminals</b>						
Terminal voltage range 6/	V <sub>A</sub> , V <sub>B</sub> , V <sub>W</sub>		V <sub>SS</sub>		V <sub>DD</sub>	V
Capacitance Ax, Bx 7/	C <sub>A</sub> , C <sub>B</sub>	f = 1 MHz, measured to GND, code = half scale		11		pF
Capacitance Wx 7/	C <sub>W</sub>			80		
Common mode leakage current 7/ 8/	I <sub>CM</sub>	V <sub>W</sub> = V <sub>DD</sub> /2		0.01	±1	μA
<b>Digital inputs and outputs</b>						
Input logic high	V <sub>IH</sub>	With respect to GND, V <sub>DD</sub> = 5 V	2.4			V
Input logic low	V <sub>IL</sub>	With respect to GND, V <sub>DD</sub> = 5 V			0.8	
Input logic high	V <sub>IH</sub>	With respect to GND, V <sub>DD</sub> = 3 V	2.1			
Input logic low	V <sub>IL</sub>	With respect to GND, V <sub>DD</sub> = 3 V			0.6	
Input logic high	V <sub>IH</sub>	With respect to GND, V <sub>DD</sub> = +2.5 V, V <sub>SS</sub> = -2.5 V	2.0			
Input logic low	V <sub>IL</sub>	With respect to GND, V <sub>DD</sub> = +2.5 V, V <sub>SS</sub> = -2.5 V			0.5	
Output logic high (SDO, RDY)	V <sub>OH</sub>	R <sub>PULL-UP</sub> = 2.2 kΩ to 5 V	4.9			
Output logic low	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA, V <sub>LOGIC</sub> = 5 V			0.4	
Input current	I <sub>IL</sub>				±2.25	μA
Input capacitance 7/	C <sub>IL</sub>			5		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions <u>2/</u> unless otherwise specified	Limits			Unit
			Min	Typ <u>3/</u>	Max	
<b>Power supplies</b>						
Single supply power range	V <sub>DD</sub>	V <sub>SS</sub> = 0 V	2.7		5.5	V
Dual supply power range	V <sub>DD</sub> /V <sub>SS</sub>		±2.25		±2.75	V
Positive supply current	I <sub>DD</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND		2	7	µA
Negative supply current	I <sub>SS</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND, V <sub>DD</sub> = +2.5 V, V <sub>SS</sub> = -2.5 V	-6	-2		µA
EEMEM store mode current	I <sub>DD(store)</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND, V <sub>SS</sub> = GND, I <sub>SS</sub> ≈ 0		2		mA
	I <sub>SS(store)</sub>	V <sub>DD</sub> = +2.5 V, V <sub>SS</sub> = -2.5 V		-2		mA
EEMEM restore mode current <u>9/</u>	I <sub>DD(restore)</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND, V <sub>SS</sub> = GND, I <sub>SS</sub> ≈ 0		320		µA
	I <sub>SS(restore)</sub>	V <sub>DD</sub> = +2.5 V, V <sub>SS</sub> = -2.5 V		-320		µA
Power dissipation <u>10/</u>	P <sub>DISS</sub>	V <sub>IH</sub> = V <sub>DD</sub> or V <sub>IL</sub> = GND		10	40	µW
Power supply sensitivity <u>7/</u>	P <sub>SS</sub>	ΔV <sub>DD</sub> = 5 V ± 10%		0.006	0.01	%/%
<b>Dynamic characteristics</b> <u>7/ 11/</u>						
Bandwidth	BW	-3 dB, V <sub>DD</sub> /V <sub>SS</sub> = ±2.5 V		125		kHz
Total harmonic distortion	THD <sub>W</sub>	V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0 V, f = 1 kHz		0.009		%
V <sub>W</sub> settling time	t <sub>s</sub>	V <sub>A</sub> = V <sub>DD</sub> , V <sub>B</sub> = 0 V, V <sub>W</sub> = 0.50% error band, Code 0x000 to code 0x200		4		µs
Resistor noise density	e <sub>N_WB</sub>	T <sub>A</sub> = 25°C		20		nV/√Hz
Crosstalk (C <sub>W1</sub> /C <sub>W2</sub> )	C <sub>T</sub>	V <sub>A</sub> = V <sub>DD</sub> , V <sub>B</sub> = 0 V, measured V <sub>W1</sub> with V <sub>W2</sub> making full scale change		30		nV-s
Analog crosstalk	C <sub>TA</sub>	V <sub>DD</sub> = V <sub>A1</sub> = +2.5 V, V <sub>SS</sub> = V <sub>B1</sub> = -2.5 V, measured V <sub>W1</sub> with V <sub>W2</sub> = 5 Vp-p@f = 1 kHz, Code 1 = 0x200, code 2 = 0x3FF		-110		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions <u>2/</u> unless otherwise specified	Limits			Unit	
			Min	Max			
<b>Interface timing and EEMEM reliability characteristics</b> <u>12/</u>							
Clock cycle time ( $t_{CYC}$ )	$t_1$		20			ns	
$\overline{CS}$ setup time	$t_2$		10			ns	
CLK shut down time for $\overline{CS}$ rise	$t_3$		1			$t_{CYC}$	
Input clock pulse width	$t_4, t_5$	Clock level high or low	10			ns	
Data setup time	$t_6$	From positive CLK transition	5				
Data hold time	$t_7$	From positive CLK transition	5				
$\overline{CS}$ to SDO-SPI line acquire	$t_8$				40		
$\overline{CS}$ to SDO-SPI line release	$t_9$				50		
CLK to SDO propagation delay <u>13/</u>	$t_{10}$	$R_P = 2.2\text{ k}\Omega, C_L < 20\text{ pF}$			50		
CLK to SDO data hold time	$t_{11}$	$R_P = 2.2\text{ k}\Omega, C_L < 20\text{ pF}$	0				
$\overline{CS}$ high pulse width <u>14/</u>	$t_{12}$		10				
$\overline{CS}$ high to $\overline{CS}$ high <u>14/</u>	$t_{13}$		4				$t_{CYC}$
RDY rise to $\overline{CS}$ fall	$t_{14}$		0				ns
$\overline{CS}$ rise to RDY fall time	$t_{15}$			0.15	0.3	ms	
Store EEMEM time <u>15/ 16/</u>	$t_{16}$	Applies to instruction 0x2, 0x3		15	50	ms	
Read EEMEM time <u>15/</u>	$t_{16}$	Applies to instruction 0x8, 0x9, and 0x10		7	30	$\mu\text{s}$	
$\overline{CS}$ rise to clock rise/Fall setup	$t_{17}$		15			ns	
Preset pulse width (Asynchronous) <u>17/</u>	$t_{PRW}$		50			ns	
Preset response time to wiper setting <u>17/</u>	$t_{PRESP}$	$\overline{PR}$ pulsed low to refresh wiper positions		30		$\mu\text{s}$	
Power ON EEMEM restore time <u>17/</u>	$t_{EEMEM}$			30		$\mu\text{s}$	
<b>Flash/EE memory reliability</b>							
Endurance <u>18/</u>		$T_A = 25^\circ\text{C}$		1		MCycles	
			100			kCycles	
Data retention <u>19/</u>				100		Years	

See footnotes at end of table.

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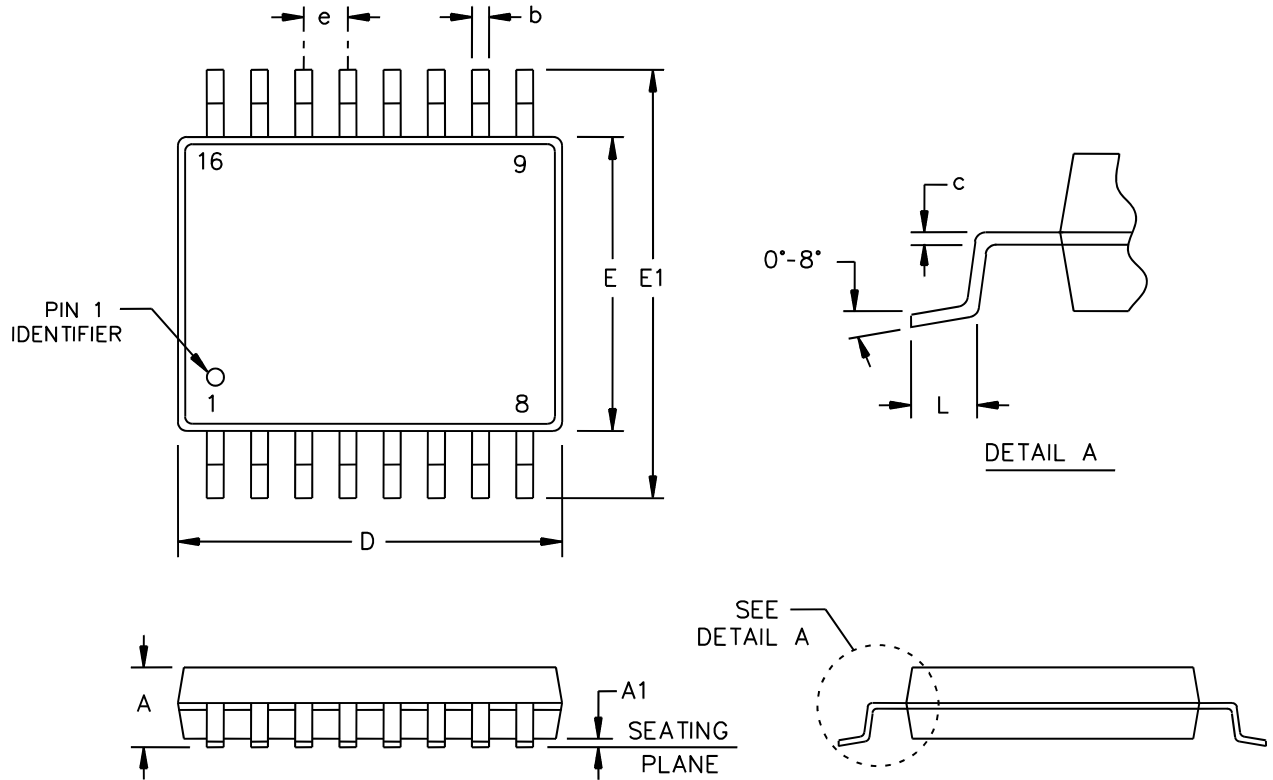
TABLE I. Electrical performance characteristics - Continued.

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/  $V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0$ ;  $V_{DD} = 2.5\text{ V}$ ,  $V_{SS} = -2.5\text{ V}$ ,  $V_A = V_{DD}$ ,  $V_B = V_{SS}$ ,  $-40^\circ\text{C} < T_A < 125^\circ\text{C}$  (unless otherwise noted). The part can be operated at 2.7 V single supply, except from  $0^\circ\text{C}$  to  $-40^\circ\text{C}$ , where a minimum of 3 V is needed.
- 3/ Typicals (TYP) represent average readings at  $25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ .
- 4/ Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.  $I_W \sim 50\ \mu\text{A}$  for  $V_{DD} = 2.7\text{ V}$  and  $I_W \sim 400\ \mu\text{A}$  for  $V_{DD} = 5\text{ V}$ .
- 5/ INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output DAC.  $V_A = V_{DD}$  and  $V_B = V_{SS}$ . DNL specification limits of  $\pm 1\text{ LSB}$  maximum guaranteed monotonic operating conditions.
- 6/ Resistor terminal A, Resistor terminal B, and resistor terminal W has no limitations on polarity with respect to each other. Dual supply operation enables ground-referenced bipolar signal adjustment.
- 7/ Guaranteed by design and not subject to production test.
- 8/ Common mode leakage current is a measure of the dc leakage from any terminal A, terminal B, or terminal W to a common mode bias level of  $V_{DD}/2$ .
- 9/ EEMEM response mode current is not continuous. Current is consumed while EEMEM locations are read and transferred to the RDAC register. To minimize power dissipation, on a NOP, instruction 0 (0x0) should be issued immediately after instruction 1 (0x1).
- 10/  $P_{DISS}$  is calculated from  $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$ .
- 11/ All dynamic characteristics use  $V_{DD} = +2.5\text{ V}$  and  $V_{SS} = -2.5\text{ V}$ .
- 12/ Guaranteed by design and not subject to production test. See the timing diagrams section for the location of measured values. All input control voltages are specified with  $t_R = t_F = 2.5\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both  $V_{DD} = 3\text{ V}$  and  $V_{DD} = 5\text{ V}$ .
- 13/ Propagation delay depends on the value of  $V_{DD}$ ,  $R_{PULL-UP}$ , and  $C_L$ .
- 14/ Valid for commands that do not activate the RDY pin.
- 15/ RDY pin low only for Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and the  $\overline{PR}$  hardware pulse;  $CMD\_8 \sim 20\ \mu\text{s}$ ;  $CMD\_9$ ,  $CMD\_10 \sim 7\ \mu\text{s}$ ;  $CMD\_2$ ,  $CMD\_3 \sim 15\text{ ms}$ ;  $\overline{PR}$  hardware pulse  $\sim 30\ \mu\text{s}$ .
- 16/ Store EEMEM time depends on the temperature and EEMEJM writes cycles. Higher timing is expected at a lower temperature and higher write cycles.
- 17/ Not shown in FIGURE 5 and FIGURE 6.
- 18/ Endurance is qualified to 100,000 cycles per JEDEC standard 22, method A117 and measured at  $-40^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+125^\circ\text{C}$ .
- 19/ Retention life time equivalent at junction temperature ( $T_J$ ) =  $85^\circ\text{C}$  per JEDEC standard 22, method A117. Retention lifetime based on an activation energy of 1 eV derates with junction temperature in the Flash/EE memory.

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Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 TYP	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

FIGURE 1. Case outline.

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Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CLK	16	RDY
2	SDI	15	$\overline{CS}$
3	SDO	14	$\overline{PR}$
4	GND	13	$\overline{WP}$
5	V <sub>SS</sub>	12	V <sub>DD</sub>
6	A1	11	A2
7	W1	10	W2
8	B1	9	B2

FIGURE 2. Terminal connections.

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
3	SDO	Serial Data Output. Serves readback and daisy-chain functions. Command 9 and Command 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 5 and Figure 6). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 5 and Figure 6). This previously shifted out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 k $\Omega$ to 10 k $\Omega$ is needed.
4	GND	Ground Pin, Logic Ground Reference.
5	V <sub>SS</sub>	Negative Supply. Connect to 0 V for single-supply applications. If V <sub>SS</sub> is used in dual supply, it must be able to sink 35 mA for 30 ms when storing data to EEMEM.
6	A1	Terminal A of RDAC1.
7	W1	Wiper terminal of RDAC1.ADDR(RDAC1)=0x0.
8	B1	Terminal B of RDAC1.
9	B2	Terminal B of RDAC2.
10	W2	Wiper terminal of RDAC2.ADDR(RDAC2)=0x1.
11	A2	Terminal A of RDAC2.
12	V <sub>DD</sub>	Positive Power Supply.
13	$\overline{WP}$	Optional Write Protect. When active low, $\overline{WP}$ prevents any changes to the present contents, except $\overline{PR}$ strobe. CMD_1 and COMD_8 refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to $\overline{WP}$ high. Tie $\overline{WP}$ to V <sub>DD</sub> , if not used.
14	$\overline{PR}$	Optional Hardware Override Preset. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 512 <sub>10</sub> until EEMEM is loaded with a new value by the user. $\overline{PR}$ is activated at the logic high transition. Tie $\overline{PR}$ to V <sub>DD</sub> , if not used.
15	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active high open-drain output. Identifies completion of Instruction 2, Instruction 3, Instruction 8, Instruction 9, Instruction 10, and $\overline{PR}$ .

FIGURE 3. Terminal functions.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/11605</b>
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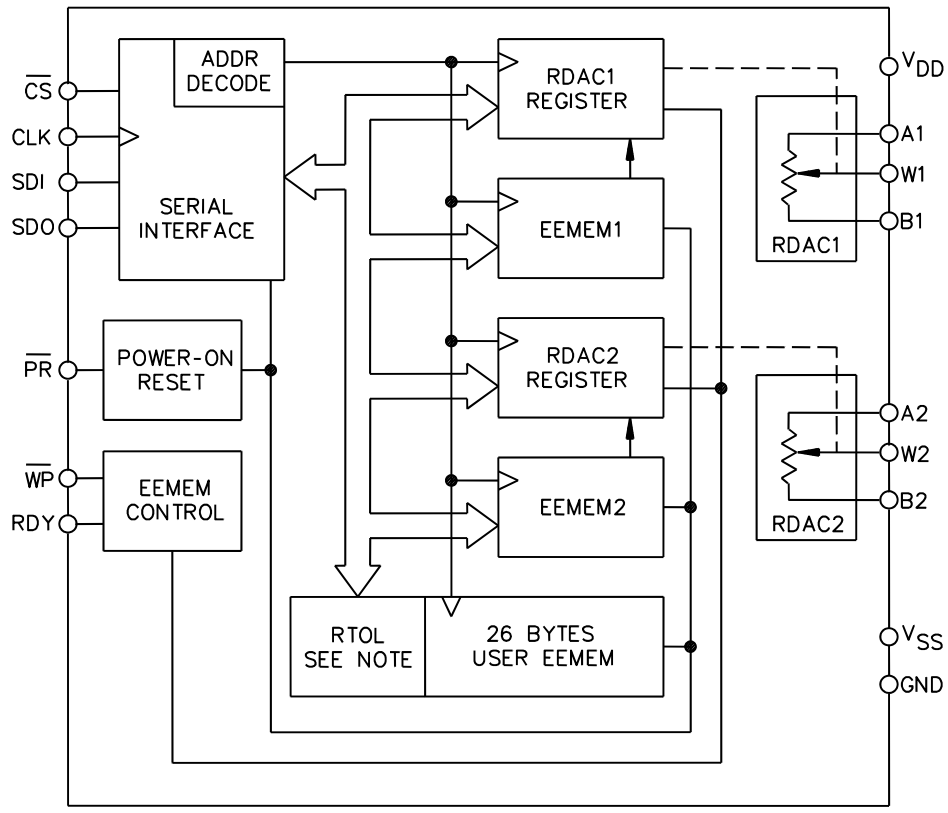
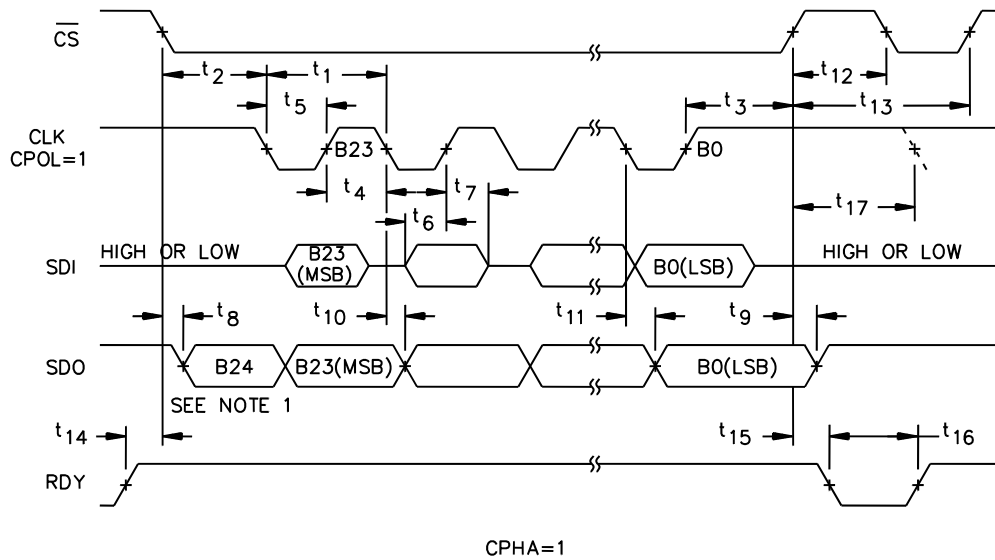


FIGURE 4. Functional block diagram.

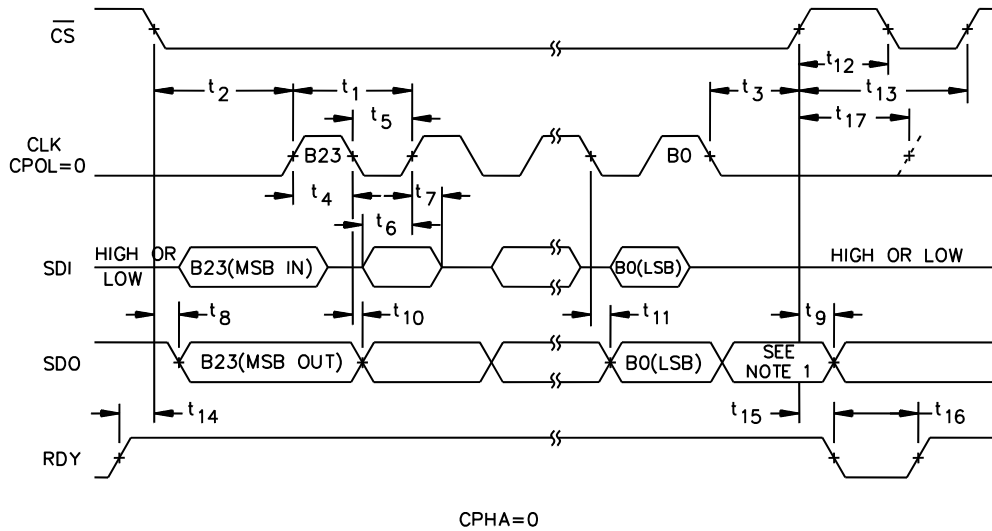
<p><b>DLA LAND AND MARITIME COLUMBUS, OHIO</b></p>	<p><b>SIZE A</b></p>	<p><b>CODE IDENT NO. 16236</b></p>	<p><b>DWG NO. V62/11605</b></p>
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NOTES:

1. The extra bit that is not defined is normally the LSB of the character previously transmitted. The CPOL = 1 microcontroller command aligns the incoming data to the positive edge of the clock.

FIGURE 5. Timing diagram.



NOTES:

1. The extra bit that is not defined is normally the MSB of the character just received. The CPOL = 0 microcontroller command aligns the incoming data to the positive edge of the clock.

FIGURE 6. Timing diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Mode of transportation and quantity	Vendor part number
V62/11605-01XB	24355	Reel, 1,000 units	AD5235BRU25-EP-RL7
V62/11605-01XE	24355	Reel, 1,000 units	AD5235BRUZ25-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices  
 Route 1 Industrial Park  
 P.O. Box 9106  
 Norwood, MA 02062  
 Point of contact: Raheen Business Park  
 Limerick, Ireland

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