

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Updated document paragraphs to current requirements. - ro	19-08-21	J. ESCHMEYER



Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
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PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime
Original date of drawing YY-MM-DD 10-09-08	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, CMOS SPDT SWITCH, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE A	CODE IDENT. NO. 16236
	REV A	DWG NO. V62/10615
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS single pole double throw (SPDT) switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/10615</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADG419-EP	CMOS SPDT switch

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MO-187-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Positive power supply (VDD) to negative power supply (VSS)	44 V
VDD to ground (GND)	-0.3 V to +25 V
VSS to GND	+0.3 V to -25 V
Logic power supply (VL) to GND	-0.3 V to VDD + 0.3 V
Analog, digital inputs 2/	VSS - 2 V to VDD + 2 V or 30 mA, whichever comes first
Continuous current, source terminal (S) or drain terminal (D)	30 mA
Peak current, S or D (pulsed at 1 ms, 10% duty cycle maximum)	100 mA
Power dissipation (PD)	315 mW
Junction temperature range (TJ)	150°C
Storage temperature range (TSTG)	-65°C to +150°C
Electrostatic discharge (ESD) rating	3/
Thermal resistance, junction to case (θ_{JC}):	44°C/W
Thermal impedance, junction to ambient (θ_{JA})	205°C/W

1.4 Recommended operating conditions. 4/

Operating free-air temperature range (TA)	-55°C to +125°C
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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Overvoltages at IN, S or D is clamped by internal diodes. Limit current to the maximum ratings given.

3/ The electrostatic discharge limit will be specified when available from the manufacturer.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuits shall be as shown in figures 4 through 10.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Dual supply							
Analog switch							
Analog signal range			-55°C to +125°C	01		V _{SS} to V _{DD}	V
On resistance	R _{ON}	V _D = ±12.5 V, I _S = -10 mA, V _{DD} = +13.5 V, V _{SS} = -13.5, see figure 4	+25°C	01		35	Ω
			-55°C to +125°C			45	
Leakage currents V _{DD} = +16.5 V, V _{SS} = -16.5 V							
Source off leakage current	I _S (off)	V _D = ±15.5 V, V _S = ∓ 15.5 V, see figure 5	+25°C	01		±0.25	nA
			-55°C to +125°C			±15	
Drain off leakage current	I _D (off)	V _D = ±15.5 V, V _S = ∓ 15.5 V, see figure 5	+25°C	01		±0.75	nA
			-55°C to +125°C			±30	
Channel on leakage current	I _D , I _S (on)	V _S = V _D = ±15.5 V, see figure 6	+25°C	01		±0.75	nA
			-55°C to +125°C			±30	
Digital inputs							
Input high voltage	V _{INH}		-55°C to +125°C	01	2.4		V
Input low voltage	V _{INL}		-55°C to +125°C	01		0.8	V
Input current	I _{INL} or I _{INH}	V _{IN} = V _{INL} or V _{INH}	-55°C to +125°C	01		±0.5	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Dual supply - continued.							
Dynamic characteristics <u>3/</u>							
Transition timing	t _T	R _L = 300 Ω, C _L = 35 pF, V _{S1} = ±10 V, V _{S2} = ∓ 10 V, see figure 7	+25°C	01		145	ns
			-55°C to +125°C			200	
Break-before-make time delay	t _D	R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = ±10 V, see figure 8	+25°C	01	5		ns
Off isolation		R _L = 50 Ω, f = 1 MHz, see figure 9	+25°C	01	80 typical		dB
Channel-to-channel crosstalk		R _L = 50 Ω, f = 1 MHz, see figure 10	+25°C	01	90 typical		dB
Source capacitance	C _S (off)	f = 1 MHz	+25°C	01	6 typical		pF
Drain capacitance	C _D , C _S (on)	f = 1 MHz	+25°C	01	55 typical		pF
Power requirements		V _{DD} = +16.5 V, V _{SS} = -16.5 V					
Drain current	I _{DD}	V _{IN} = 0 V to 5 V	+25°C	01		1	μA
			-55°C to +125°C			2.5	
Source current	I _{SS}		+25°C	01		1	μA
			-55°C to +125°C			2.5	
Load current	I _L	V _L = 5.5 V	+25°C	01		1	μA
			-55°C to +125°C			2.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 4/	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Single supply							
Analog switch							
Analog signal range			-55°C to +125°C	01		0 to VDD	V
On resistance	RON	VD = 3 V, 8.5 V, IS = -10 mA, VDD = 10.8 V, see figure 4	-55°C to +125°C	01		70	Ω
Leakage currents VDD = +13.2 V							
Source off leakage current	IS (off)	VD = 12.2 V/1 V, VS = 1 V/12.2 V, see figure 5	+25°C	01		±0.25	nA
			-55°C to +125°C			±15	
Drain off leakage current	ID (off)	VD = 12.2 V/1 V, VS = 1 V/12.2 V, see figure 5	+25°C	01		±0.75	nA
			-55°C to +125°C			±30	
Channel on leakage current	ID, IS (on)	VS = VD = 12.2 V/1 V, see figure 6	+25°C	01		±0.75	nA
			-55°C to +125°C			±30	
Digital inputs							
Input high voltage	VINH		-55°C to +125°C	01	2.4		V
Input low voltage	VINL		-55°C to +125°C	01		0.8	V
Input current	IINL or IINH	VIN = VINL or VINH	-55°C to +125°C	01		±0.5	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>4/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Single supply - continued.							
Dynamic characteristics <u>3/</u>							
Transition timing	t _T	R _L = 300 Ω, C _L = 35 pF, V _{S1} = 0 V/8 V, V _{S2} = 8 V/0 V, see figure 7	+25°C	01		170	ns
			-55°C to +125°C			250	
Break-before-make time delay	t _D	R _L = 300 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 8 V, see figure 8	+25°C	01	60 typical		ns
Off isolation		R _L = 50 Ω, f = 1 MHz, see figure 9	+25°C	01	80 typical		dB
Channel-to-channel crosstalk		R _L = 50 Ω, f = 1 MHz, see figure 10	+25°C	01	70 typical		dB
Source capacitance	C _S (off)	f = 1 MHz	+25°C	01	13 typical		pF
Drain capacitance	C _D , C _S (on)	f = 1 MHz	+25°C	01	65 typical		pF
Power requirements		V _{DD} = +13.2 V					
Drain current	I _{DD}	V _{IN} = 0 V to 5 V	+25°C	01		1	μA
			-55°C to +125°C			2.5	
Load current	I _L	V _L = 5.5 V	+25°C	01		1	μA
			-55°C to +125°C			2.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 15 V ±10%, V_{SS} = -15V ±10%, V_L = 5 V ±10%, and GND = 0 V.

3/ Guaranteed by design, not subject to production test.

4/ Unless otherwise specified, V_{DD} = 12 V ±10%, V_{SS} = 0 V, V_L = 5 V ±10%, and GND = 0 V.

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Case X

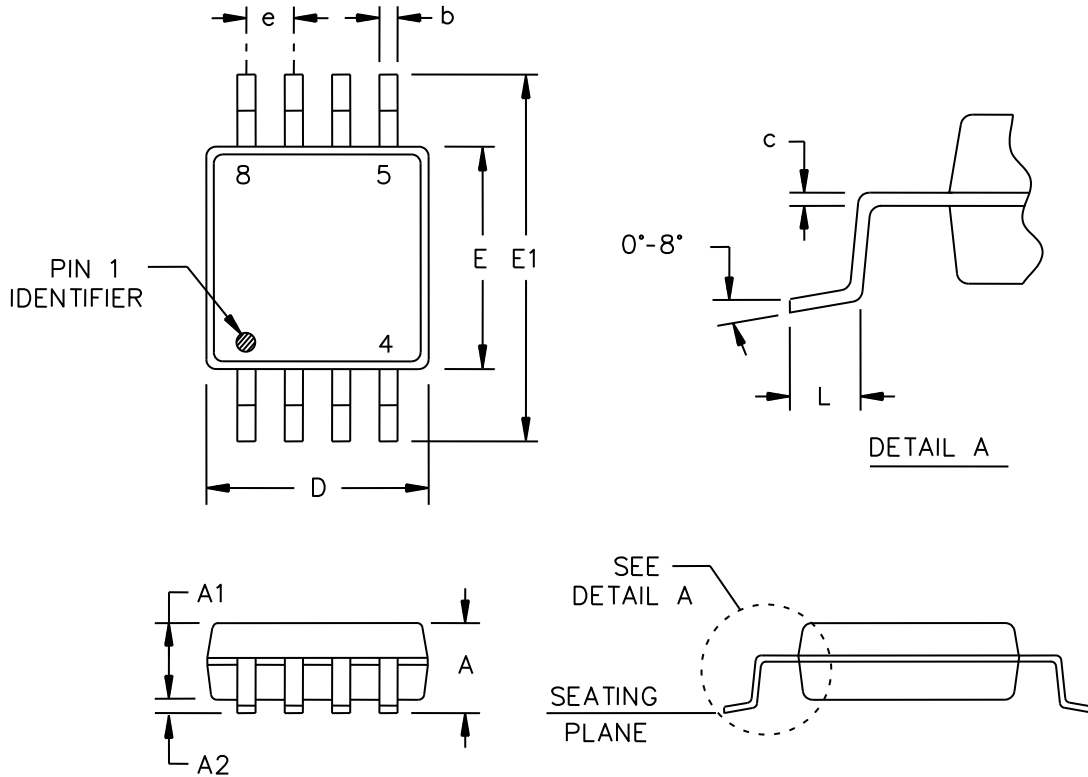


FIGURE 1. Case outline.

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Case X - continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.043	---	1.10
A1	0.029	0.037	0.75	0.95
A2	0.000	0.005	0.00	0.15
b	0.009	0.015	0.25	0.40
c	0.003	0.009	0.09	0.23
D	0.110	0.125	2.80	3.20
E	0.110	0.125	2.80	3.20
E1	0.183	0.202	4.65	5.15
e	0.025 BSC		0.65 BSC	
L	0.015	0.031	0.40	0.80

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls with JEDEC MO-187-AA.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	D	Drain terminal. May be an input or an output.
2	S1	Source terminal. May be an input or an output.
3	GND	Ground (0 V) reference.
4	VDD	Most positive power supply potential.
5	VL	Logic power supply (5 V).
6	IN	Logic control input.
7	VSS	Most negative power supply potential in dual-supply applications. In single-supply applications, it may be connected to GND.
8	S2	Source terminal. May be an input or an output.

FIGURE 2. Terminal connections.

Logic	Switch 1	Switch 2
0	On	Off
1	Off	On

FIGURE 3. Truth table.

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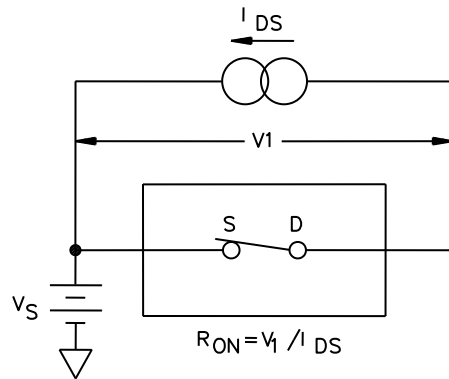


FIGURE 4. On resistance test circuit.

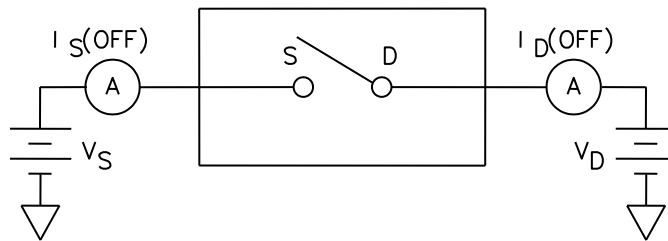


FIGURE 5. Off leakage test circuit.

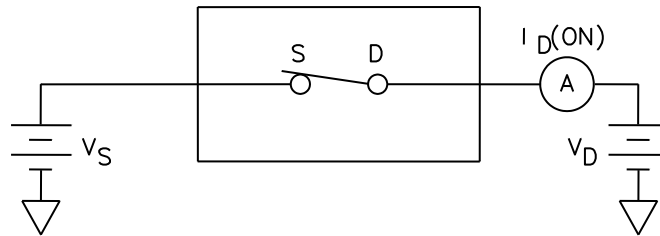


FIGURE 6. On leakage test circuit.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/10615</p>
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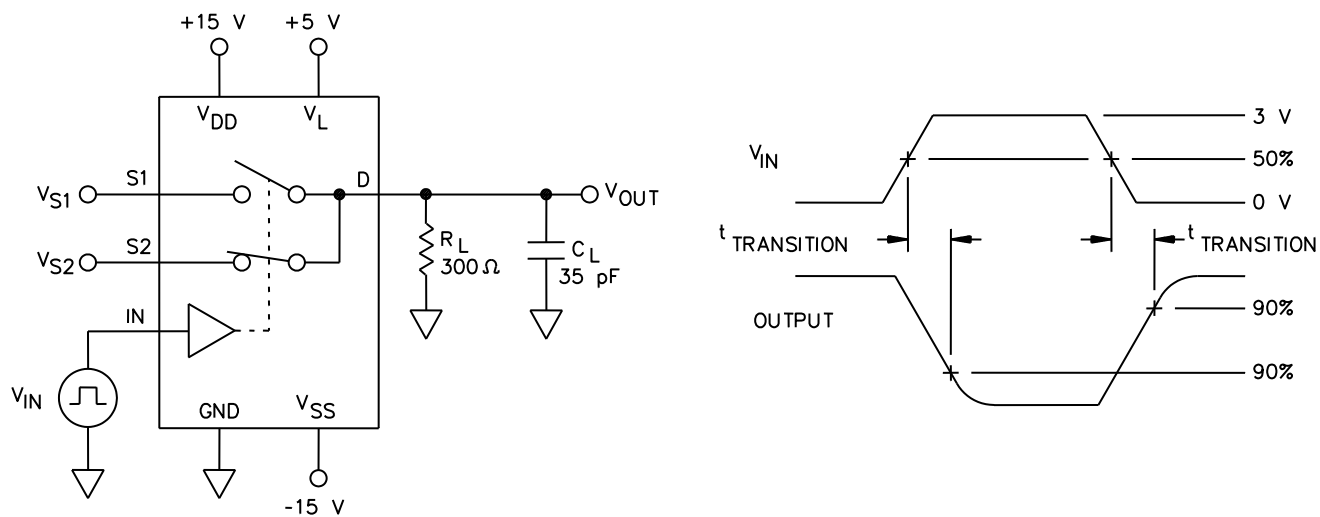


FIGURE 7. Transition time test circuit and waveforms.

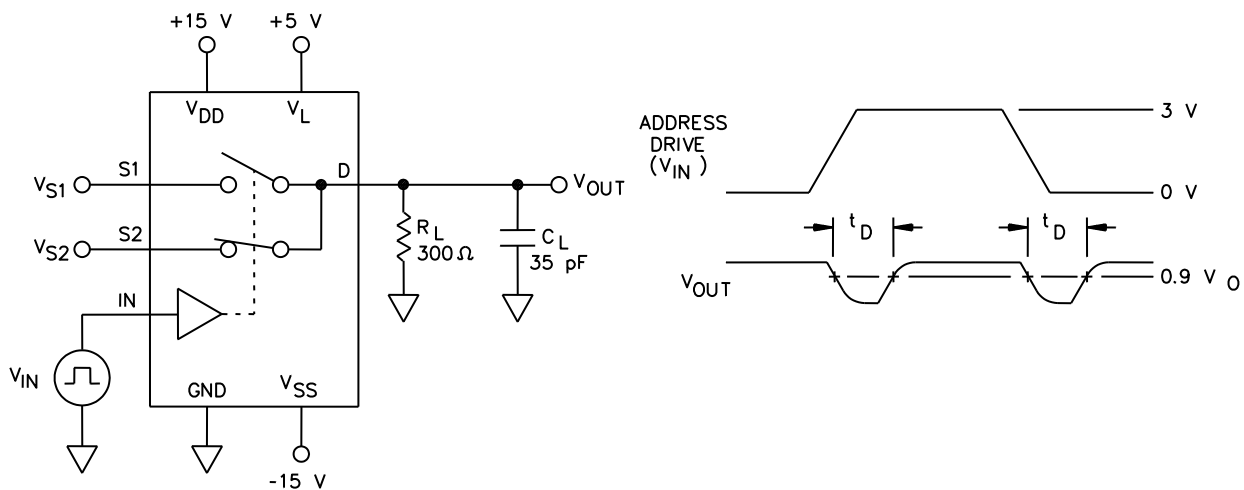


FIGURE 8. Break-before-make time delay test circuit and waveforms.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/10615</p>
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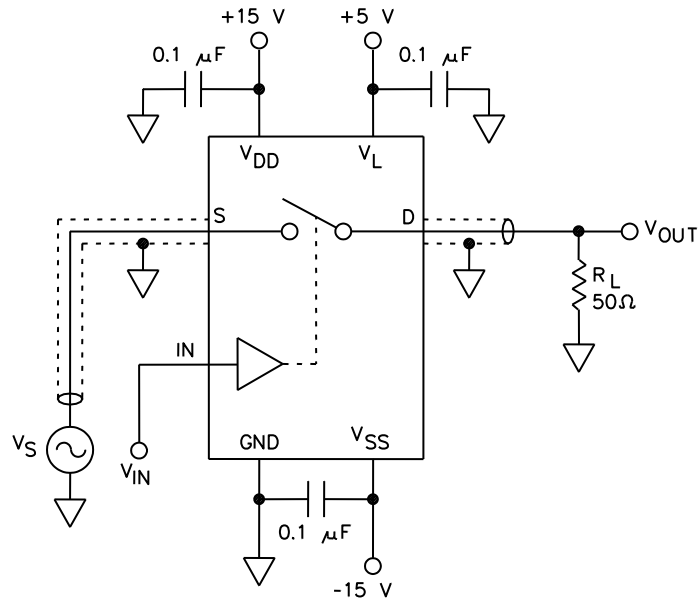
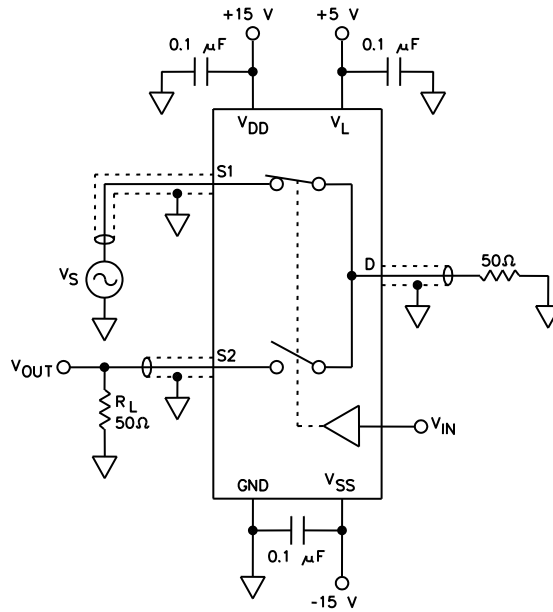


FIGURE 9. Off isolation test circuit.



$$\text{Channel-to-channel crosstalk} = 20 \times \log | V_S / V_{OUT} |$$

FIGURE 10. Crosstalk test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/10615-01XA	24355	ADG419SRMZ-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: 20 Alpha Road
 Chelmsford, MA 01824-4123

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