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				C	2	Add paragraph 1.5 and delete Thermal resistance, junction to ambient limit from Table I. Add min limits to the Input voltage and Output short circuit parameters under paragraph 1.3. Make change to Input voltage range, add Output current, and add footnotes to Electrostatic discharge parameters to paragraph 1.4. Make changes to Output voltage temperature drift, Line regulation, Load regulation, and Quiescent current tests as specified under Table I. Update document paragraphs to current requirements ro16-06-01C						C. SAFFLE										
					E)	Make parag parag accul Line curre dime Add desc	- 1ake changes to VIN and IOS limits under 21-09-02 J. ES aragraph 1.3. Add JEDEC references to aragraphs 1.3 and 2. Make changes to 21-09-02 J. ES aragraphs 1.4 and 1.5. Make changes to Initial ccuracy, Output voltage temperature drift, ine regulation, Load regulation, and Quiescent urrent tests under Table I. Make change to imension "c" min limit and note 3 under figure 1. add I/O column and make changes to lescriptions under figure 2 ro Image: column and make changes to Image: column and make changes to					ESCHI	MEYE	R							
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1. SCOPE

1.1 <u>Scope</u>. This drawing documents the general requirements of a low noise, low drift, precision voltage reference microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 <u>Vendor Item Drawing Administrative Control Number</u>. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/10613</u> Drawing number	-	01 Device type (See 1.2.1)	X Case outline (See 1.2.2)	Lead finish (See 1.2.3)
1.2.1 Device type(s).				
Device type	<u>Generic</u>	Output voltage		Circuit function
01 02 03 04	REF5020 REF5040 REF5050 REF5025	2.048 V 4.096 V 5.0 V 2.5 V	Low nois Low nois Low nois Low nois	se, low drift, precision voltage reference se, low drift, precision voltage reference se, low drift, precision voltage reference se, low drift, precision voltage reference

1.2.2 <u>Case outline(s)</u>. The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
х	8	MS-012-AA	Plastic surface mount with gullwing leads

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
А	Hot solder dip
В	Tin-lead plate
С	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage (VIN)	18 V
Output short circuit (IOS)	30 mA
Operating temperature range (TA)	-55°C to +125°C
Storage temperature range (TSTG)	-65°C to +150°C
Junction temperature range (TJ max)	150°C
Power dissipation (PD)	166.66 mW
Electrostatic discharge (ESD) rating:	
Human body model (HBM), per JEDEC JS-001	±3,000 V <u>2</u> /
Charged device model (CDM), per JEDEC JESD22-C101	±1,000 V <u>3</u> /

1.4 Recommended operating conditions. 4/

Input voltage range (VIN) per device :	
Device types 01, 02, 03, 04	(VOUT + 0.2 V) min, 18 V max
Output current (IOUT)	10 mA min, 10 mA max
Operating temperature range (TA)	55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θJΑ	123.8	°C/W
Thermal resistance, junction-to-case (top)	θ JC(TOP)	54.4	°C/W
Thermal resistance, junction-to-board	θЈΒ	69.3	°C/W
Characterization parameter, junction-to-top	ΨJT	10.2	°C/W
Characterization parameter, junction-to-board	ψJB	68.1	°C/W
Thermal resistance, junction-to-case (bottom)	θJC(BOTTOM)	Not applicable	°C/W

<u>2/</u> <u>3/</u> <u>4</u>/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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^{1/} Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

JEDEC document JEP157 states that 250 V HBM allows safe manufacturing with a standard ESD control process.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	-	Human Body Model Testing of Integrated Circuits
JESD22-C101	-	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand
		Thresholds of Microelectronics Components
JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	-	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	-	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 <u>Marking</u>. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 <u>Unit container</u>. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 <u>Electrical characteristics</u>. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 <u>Design, construction, and physical dimension</u>. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 <u>Case outline</u>. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 <u>Terminal connections</u>. The terminal connections shall be as shown in figure 2.

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Test	Symbol	Conditions <u>2</u> /	Temperature,	Device type	Lir	nits	Unit
					Min	Max	
Output voltage	Vout	2.7 V < VIN < 18 V <u>3</u> /	+25°C	01	2.048	typical	V
				02	4.096	typical	-
				03	5 ty	pical	
				04	2.5 t	ypical	
Initial accuracy			+25°C	All	-0.05	0.05	%
			55°C to +125°C	01, 02, 03	-0.08	0.08	
Output voltage noise		f = 0.1 Hz to 10 Hz	+25°C	01	6 ty	pical	μVpp
				02	12 ty	/pical	
				03	15 ty	/pical	
				04	7.5 t	ypical	
Output voltage	∆Vout /		-55°C to +125°C	01, 02		5	ppm /
	ΔT			03, 04		6.5	ۍ.
Line regulation	ΔVOUT / ΔVIN	VIN = 2.7 V to 18 V <u>3</u> /	+25°C	01		1	ppm/V
		VIN = VOUT + 0.2 V	+25°C	02, 03,		1	
			-55°C to +125°C	- 04		3	
Load regulation	∆Vout / ∆Iload	-10 mA < I _{LOAD} < +10 mA, VIN = 3 V	+25°C	01		30	ppm / mA
		-10 mA < ILOAD < +10 mA,	+25°C	02, 03,		30	
		VIN = VOUT + 0.75 V	-55°C to +125°C	- 04		60	
Short circuit current	Isc	VOUT = 0 V	+25°C	All	25 ty	/pical	mA
TEMP pin, voltage output			+25°C	All	575 t	ypical	mV
TEMP pin, temperature sensitivity			-55°C to +125°C	All	2.64	typical	mV/°C
Turn on settling time		To 0.1 % with CL = 1 μ F	+25°C	All	200 t	ypical	μs

TABLE I. <u>Electrical performance characteristics</u>. <u>1</u>/

See footnotes at end of table.

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Test	Symbol	Conditions <u>2</u> / Temperature, Device Limits TA type		nits	Unit		
					Min	Max	
Power supply							
Supply voltage	Vs	<u>3</u> /	+25°C	All	Vout + 0.2	18	V
Quiescent current			+25°C	All		1	mA
			-55°C to +125°C			1.25	
Specified temperature range				All	-55	+125	°C
Operating temperature range				All	-55	+125	°C

TABLE I. Electrical performance characteristics - Continued. 1/

<u>1</u>/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

<u>2</u>/ Unless otherwise specified, ILOAD = 0, CL = 1 μ F, and VIN = (VOUT + 0.2 V) to 18 V.

 $\underline{3}/$ $\,$ For VOUT ≤ 2.5 V, the minimum supply voltage is 2.7 V.

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FIGURE 1. Case outline.

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Case X

	Dimensions					
Symbol	Inches		Millim	neters		
	Min	Max	Min	Max		
A		.069		1.75		
A1	.004	.010	0.10	0.25		
b	.012	.020	0.31	0.51		
с	.005	.010	0.13	0.25		
D	.189	.197	4.80	5.00		
E	.150	.157	3.81	3.99		
E1	.228	.244	5.80	6.20		
е	.050 BSC		1.27	BSC		
L	.016	.050	0.41	1.27		
n	8		8			

NOTES:

- 1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
- 2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed .006 inch (0.15 mm) per side.
- 3. For dimension E, body width does not include interlead flash.
- 4. Falls with JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

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Device types	01, 02, 03, 04			
Case outline			X	
Terminal number	Terminal symbol	I/O	Description	
1	DNC		Do not connect.	
2	Vin	Power	Power supply voltage. Range from VOUT + 0.2 V up to 18 V. Recommended bypass capacitor from 1 μF to 10 μF.	
3	TEMP	0	Temperature monitoring pin provides a temperature dependent voltage output.	
4	GND	Power	System ground.	
5	TRIM / NR	I	Output adjustment and noise reduction input. Connecting 1 μ F to this pin will create low pass filter at the bandgap and reduce output noise.	
6	Vout	0	Very accurate, factory trimmed voltage output. Recommended bypass capacitor from 1 μ F up to 50 μ F with equivalent series resistance (ESR) between 1 Ω and 1.5 Ω .	
7	NC		No internal connection.	
8	DNC		Do not connect.	

FIGURE 2. Terminal connections.

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4. VERIFICATION

4.1 <u>Product assurance requirements</u>. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 <u>Packaging</u>. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 <u>ESDS</u>. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 <u>Configuration control</u>. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 <u>Suggested source(s) of supply</u>. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <u>https://landandmaritimeapps.dla.mil/Programs/Smcr/</u>.

Vendor item drawing administrative control number <u>1</u> / <u>2</u> / <u>3</u> /	Device manufacturer CAGE code	Output voltage	Top side marking	Vendor part number
V62/10613-01XE	01295	2.048 V	5020EP	REF5020MDREP
V62/10613-02XE	01295	4.096 V	5040EP	REF5040MDREP
V62/10613-03XE	01295	5 V	5050EP	REF5050MDREP
V62/10613-04XE	01295	2.5 V	5025EP	REF5025MDTEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.
- 3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243

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