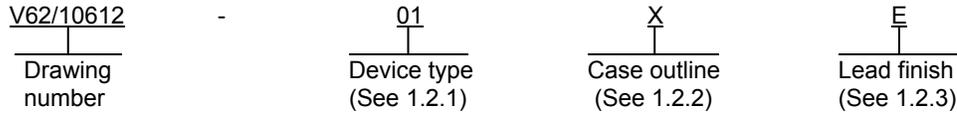


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8-bit shift registers with 3-state output registers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74HC595-EP	8-bit Shift Registers with 3-state output registers

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7 V
Input clamp current (I_{IK}) ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA <u>2/</u>
Output clamp current (I_{OK}) ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA <u>2/</u>
Continuous output current (I_O) ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance (θ_{JA})	108°C/W <u>3/</u>
Storage temperature range (T_{STG})	-65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 4/ 5/

Supply voltage range (V_{CC})	2.0 V to 6.0 V
Minimum high level input voltage (V_{IH}):	
$V_{CC} = 2\text{ V}$	1.5 V
$V_{CC} = 4.5\text{ V}$	3.15 V
$V_{CC} = 6.0\text{ V}$	4.2 V
Maximum low level input voltage (V_{IL}):	
$V_{CC} = 2\text{ V}$	0.5 V
$V_{CC} = 4.5\text{ V}$	1.35 V
$V_{CC} = 6.0\text{ V}$	1.8 V
Input voltage (V_I)	0 V to V_{CC}
Output voltage (V_O)	0 V to V_{CC}
Maximum input transition rise or fall rate ($\Delta t / \Delta v$): <u>6/</u>	
$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200 ns/V
$V_{CC} = 3\text{ V to }3.6\text{ V}$	100 ns/V
$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

-
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
 - 5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
 - 6/ If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to do into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000\text{ ns}$ and $V_{CC} = 2\text{ V}$ does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5 .

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions unless otherwise specified		V _{CC}	Limits				Unit
					T _A = 25°C		-55°C ≤ T _A ≤ 125°C		
					Min	Max	Min	Max	
High level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9		1.9		V
				4.5 V	4.4		4.4		
				6 V	5.9		5.9		
			Q _H , I _{OH} = - 4 mA	4.5 V	3.98		3.7		
				Q _A - Q _H , I _{OH} = - 6 mA		3.98		3.7	
				Q _H , I _{OH} = - 5.2 mA	6 V	5.48		5.2	
Q _A - Q _H , I _{OH} = - 7.8 mA		5.48		5.2					
Low level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.1		0.1	V
				4.5 V		0.1		0.1	
				6 V		0.1		0.1	
			Q _H , I _{OL} = 4 mA	4.5 V		0.26		0.4	
				Q _A - Q _H , I _{OL} = 6 mA		0.26		0.4	
				Q _H , I _{OL} = 5.2 mA	6 V		0.26		
Q _A - Q _H , I _{OL} = 7.8 mA		0.26		0.4					
Input current	I _I	V _I = V _{CC} or 0		6 V		±100		±1000	nA
Off state output current	I _{OZ}	V _O = V _{CC} or 0, Q _A - Q _H		6 V		±0.5		±10	μA
Supply current	I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V		8		160	μA
Input capacitance	C _i			2 V to 6V		10		10	pF
Power dissipation capacitance	C _{pd}	No load				400 TYP			pF

Timing requirements

Clock frequency	f _{clock}		2 V		6		4.2	MHz
			4.5 V		31		21	
			6 V		36		25	
Pulse duration	t _w	SRCL or RCLK high or low	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		SRCL low	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
Setup time	t _{su}	SER before SRCLK↑	2 V	100		150		
			4.5 V	20		30		
			6 V	17		25		
		SRCLK↑ before RCLK↑	2 V	75		113		
			4.5 V	15		23		
			6 V	13		19		
		SRCLR low before RCLK↑	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
		SRCLR high (inactive) before SRCLK↑	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		

See footnotes at end of table.

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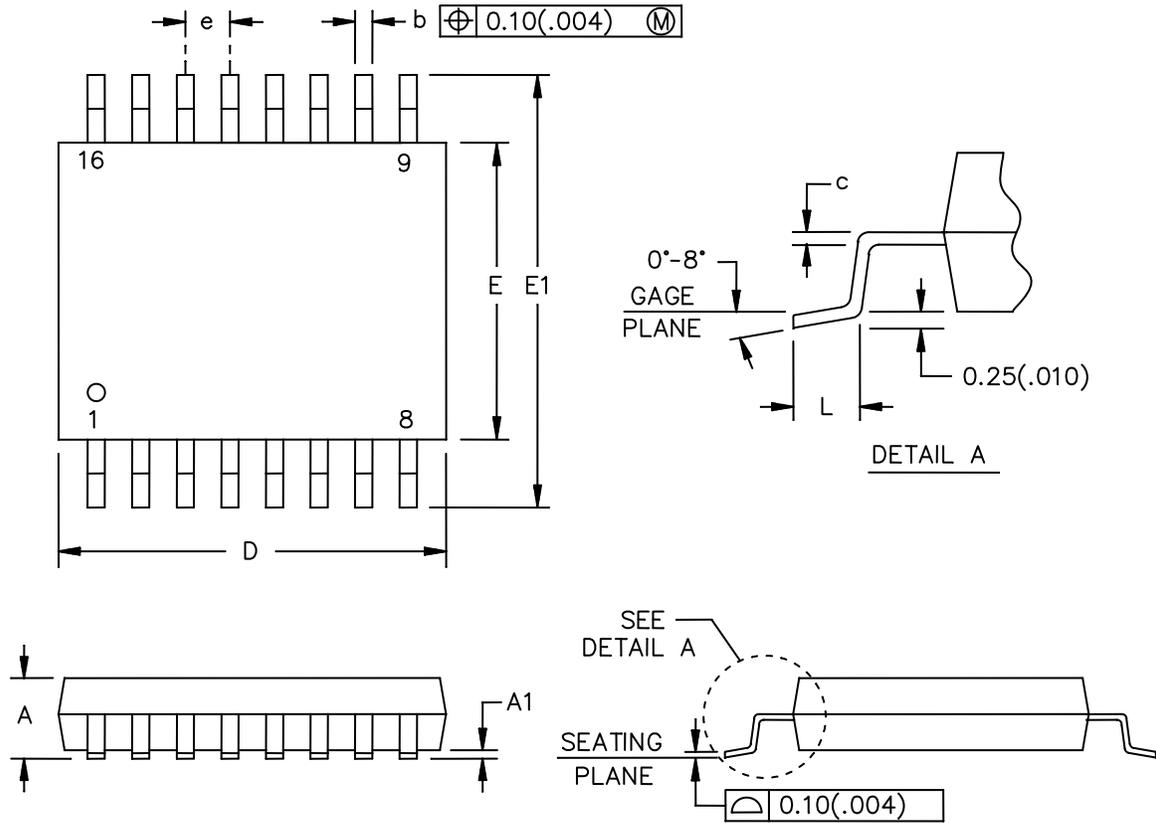
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions unless otherwise specified	V _{CC}	Limits				Unit
				T _A = 25°C		-55°C ≤ T _A ≤ 125°C		
				Min	Max	Min	Max	
Timing requirements - Continued								
Hold time, SER after SRCLK↑	t _h		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		
Switching characteristics								
Maximum frequency		C _L = 50 pF	2 V	6		4.2		MHz
			4.5 V	31		21		
			6 V	36		25		
Propagation delay from SRCLK to Q _H	t _{pd}		2 V		160		240	ns
			4.5 V		32		48	
			6 V		27		41	
Propagation delay from RCLK to Q _A -Q _H	t _{pd}		2 V		150		225	
			4.5 V		30		45	
			6 V		26		38	
Propagation delay, high to low, from SRCLR to Q _H	t _{PHL}		2 V		175		261	
			4.5 V		35		52	
			6 V		30		44	
Enable time from \overline{OE} to Q _A -Q _H	t _{en}		2 V		150		255	
			4.5 V		30		45	
			6 V		26		38	
Disable time from \overline{OE} to Q _A -Q _H	t _{dis}		2 V		200		300	
			4.5 V		40		60	
			6 V		34		51	
Transition time to Q _A -Q _H	t _t		2 V		60		90	
			4.5 V		12		18	
			6 V		10		15	
Transition time to Q _H	t _t		2 V		75		110	
			4.5 V		15		22	
			6 V		13		19	
Propagation delay from RCLK to Q _A -Q _H	t _{pd}	C _L = 150 pF	2 V		200		300	
			4.5 V		40		60	
			6 V		34		51	
Enable time from \overline{OE} to Q _A -Q _H	t _{en}		2 V		200		298	
			4.5 V		40		60	
			6 V		34		51	
Transition time to Q _A -Q _H	t _t		2 V		210		315	
			4.5 V		42		63	
			6 V		36		53	

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

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Case X



Dimension									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A		1.20		0.047	E	4.30	4.50	0.169	0.177
A1	0.05	0.15	0.002	0.006	E1	6.20	6.60	0.244	0.260
b	0.19	0.30	0.007	0.012	e	0.65 NOM		0.026 NOM	
c	0.15 NOM		0.006 NOM		L	0.50	0.75	0.020	0.030
D	4.90	5.10	0.193	0.201					

NOTES:

1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches).
3. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Q _B	9	Q _H '
2	Q _C	10	SRCLR
3	Q _D	11	SRCLK
4	Q _E	12	RCLK
5	Q _F	13	\overline{OE}
6	Q _G	14	SER
7	Q _H	15	Q _A
8	GND	16	V _{CC}

FIGURE 2. Terminal connections.

Inputs					Function
SER	SRCLK	\overline{SRCLR}	RCLK	\overline{OE}	
X	X	X	X	H	Outputs Q _A – Q _H are disable
X	X	X	X	L	Outputs Q _A – Q _H are enable
X	X	L	X	X	Shift register is clear
L	↑	H	X	X	First stage of the shift register goes low. Other stage store the data of previous stage, respectively
H	↑	H	X	X	First stage of the shift register goes high. Other stage store the data of previous stage, respectively
X	X	X	↑	X	Shift register data is stored in the storage register

FIGURE 3. Function table.

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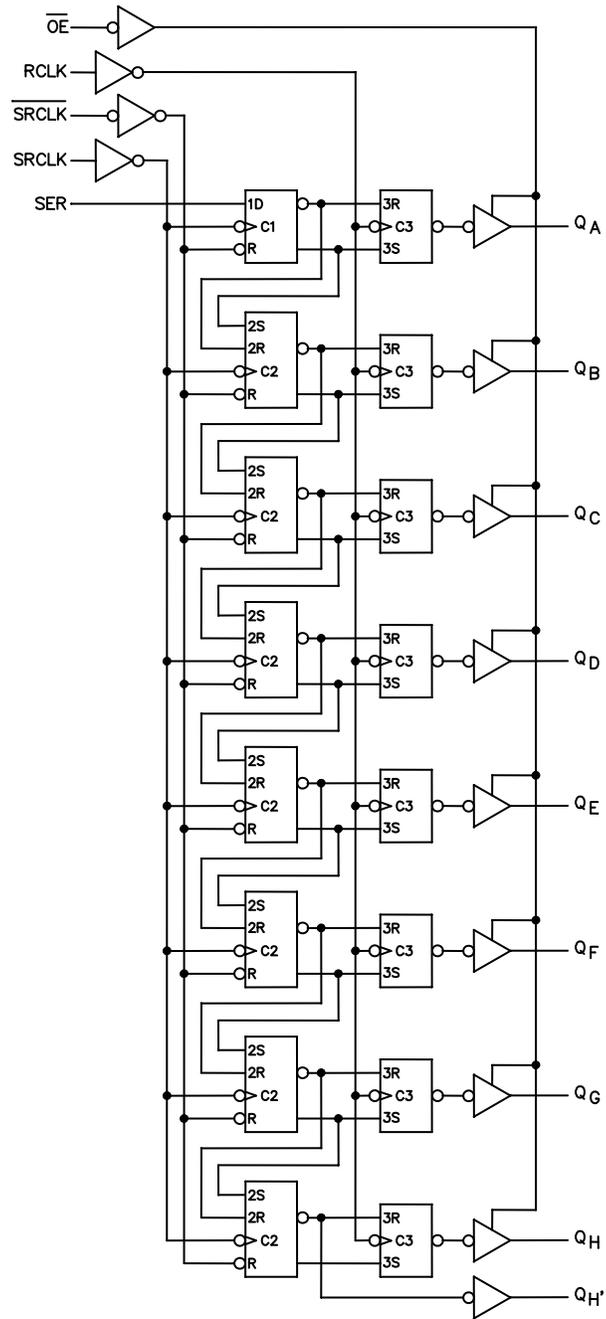
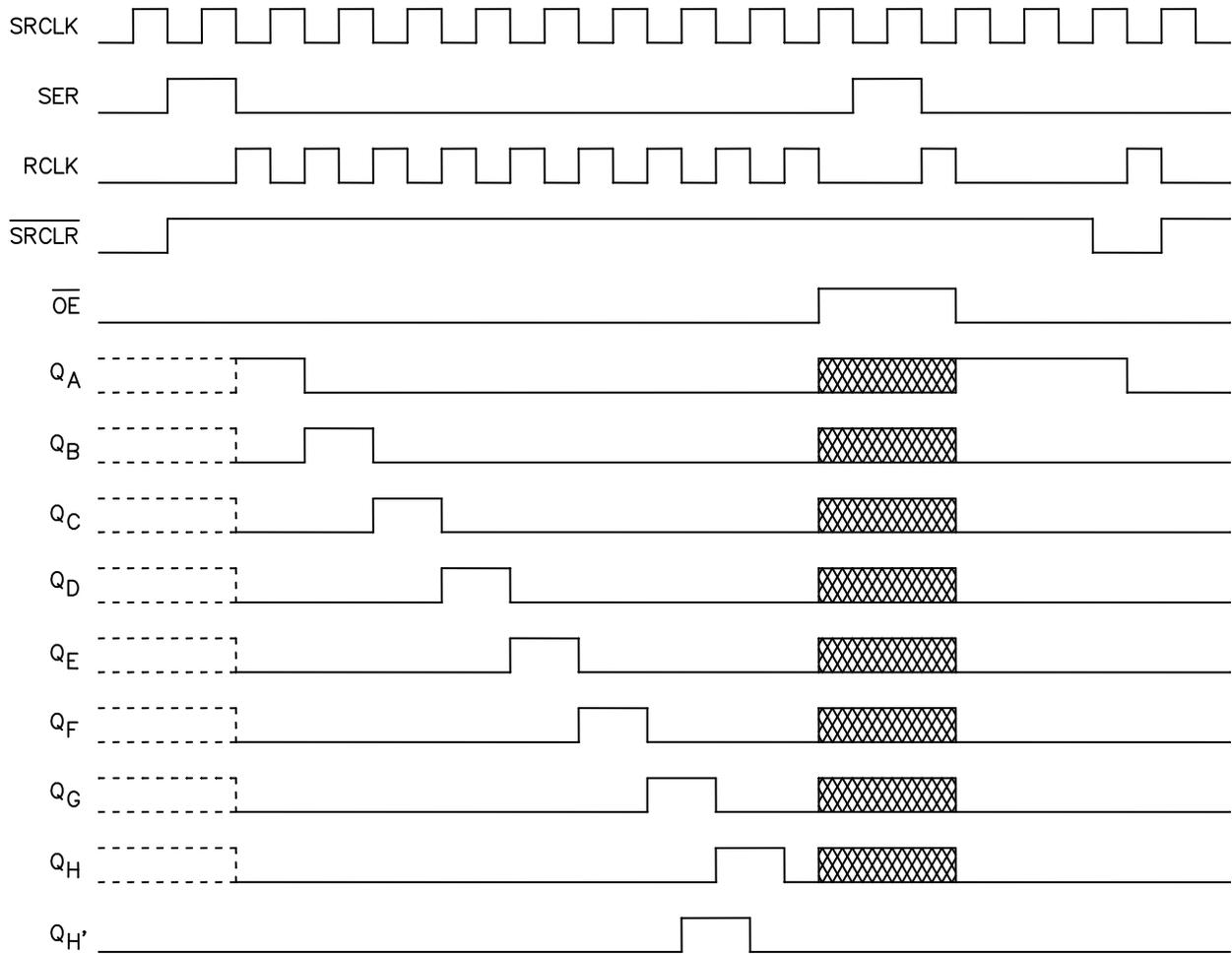


FIGURE 4. Logic diagram.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/10612</p>
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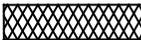
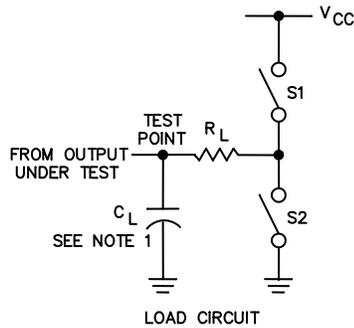
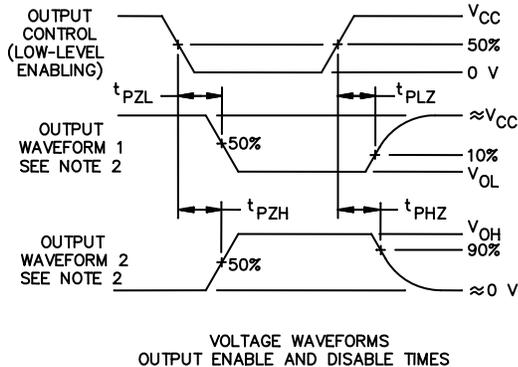
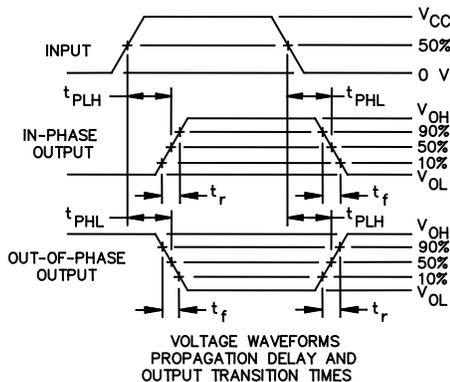
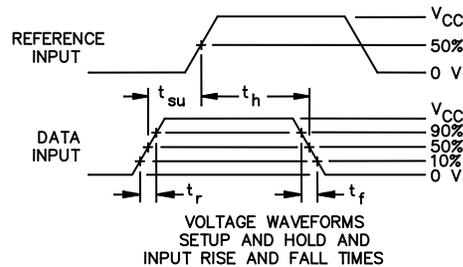
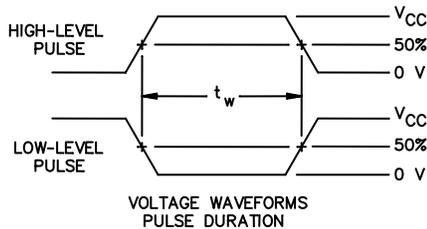
NOTE:  IMPLIES THAT THE OUTPUT IS IN 3-STATE MODE.

FIGURE 5. Load circuit and timing waveforms.

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PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	OPEN	CLOSED
			CLOSED	OPEN
t_{dis}	1 k Ω	50 pF	OPEN	CLOSED
			CLOSED	OPEN
t_{pd} or t_t	—	50 pF or 150 pF	OPEN	OPEN



NOTES:

- C_L includes probe and test fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, and $t_f = 6$ ns.
- For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PHL} and t_{PLH} are the same as t_{pd} .

FIGURE 5. Load circuit and timing waveforms – Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/10612-01XE	01295	SN74HC595MPWREP	HC595EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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