

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add paragraph 1.5, Thermal characteristics. Update document paragraphs to current requirements. - ro	16-02-09	C. SAFFLE
B	Update document paragraph to current requirements. - ro	21-08-25	J. ESCHMEYER



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990																		
Original date of drawing YY-MM-DD 10-06-22	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, 3.0 AMP LOW DROP OUT VOLTAGE REGULATOR WITH PROGRAMMABLE SOFT START, MONOLITHIC SILICON																		
	APPROVED BY CHARLES F. SAFFLE																			
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/10611																	
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a 3.0 amp low drop out voltage regulator with programmable soft start microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/10611</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS74401-EP	3.0 amp low drop out voltage regulator with programmable soft start

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-220	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/ 2/

Input voltage range (VIN, VBIAS)	-0.3 V to +6 V
Enable voltage range (VEN)	-0.3 V to +6 V
Power good (PG) voltage range (VPG)	-0.3 V to +6 V
PG sink current (IPG)	0 mA to +1.5 mA
Soft start (SS) pin voltage range (VSS)	-0.3 V to +6 V
Feedback (FB) pin voltage range (VFB)	-0.3 V to +6 V
Output voltage range (VOUT)	-0.3 V to VIN + 0.3 V
Power dissipation (PD)	3/
Maximum output current (IOUT)	Internally limited
Output short circuit duration	Indefinite
Storage junction temperature range (TSTG)	-65°C to +150°C
Operating junction temperature range (TJ)	-55°C to +125°C

1.4 Recommended operating conditions. 4/

Operating junction temperature range (TJ)	-55°C to +125°C
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1.5 Thermal characteristics.

Thermal metric 5/ 6/	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θJA	36.3	°C/W
Thermal resistance, junction-to-case (top)	θJC(TOP)	34.3	°C/W
Thermal resistance, junction-to-board	θJB	10.8	°C/W
Characterization parameter, junction-to-top	ψJT	0.3	°C/W
Characterization parameter, junction-to-board	ψJB	11.9	°C/W
Thermal resistance, junction-to-case (bottom)	θJC(BOTTOM)	2.4	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltages are respect to GND.

3/ Depending on input voltage and load conditions, power dissipation can be calculated by $PD = (V_{IN} - V_{OUT}) \times I_{OUT}$.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ For information about traditional and new thermal metrics, contact the manufacturer.

6/ For thermal estimates of this device based on printed circuit board (PCB) copper area, contact the manufacturer.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Input voltage range	V _{IN}		-55°C to +125°C	01	V _{OUT} + V _{D0}	5.5	V
Bias pin voltage range	V _{BIAS}		-55°C to +125°C	01	2.375	5.25	V
Internal reference (adjustment)	V _{REF}		-55°C to +125°C	01	0.792	0.808	V
Output voltage range	V _{OUT}	V _{IN} = 5 V, I _{OUT} = 1.5 A, V _{BIAS} = 5 V	-55°C to +125°C	01	V _{REF}	3.6	V
Accuracy 3/	V _{OUT}	2.97 V ≤ V _{BIAS} ≤ 5.25 V, 50 mA ≤ I _{OUT} ≤ 3.0 A	-55°C to +125°C	01	-1	+1	%
Line regulation	V _{OUT} / V _{IN}	V _{OUT} (NOM) + 0.3 ≤ V _{IN} ≤ 5.5 V	-55°C to +125°C	01		0.05	%/V
Load regulation	V _{OUT} / I _{OUT}	0 mA ≤ I _{OUT} ≤ 50 mA	+25°C	01	0.013 typical		%/mA
		50 mA ≤ I _{OUT} ≤ 3.0 A			0.03 typical		%/A
V _{IN} dropout voltage 4/	V _{D0}	I _{OUT} = 3.0 A, V _{BIAS} - V _{OUT} (NOM) ≥ 1.62 V	-55°C to +125°C	01		195	mV
V _{BIAS} dropout voltage 4/	V _{D0}	I _{OUT} = 3.0 A, V _{IN} = V _{BIAS}	-55°C to +125°C	01		1.62	V
Current limit	I _{CL}	V _{OUT} = 80% x V _{OUT} (NOM)	-55°C to +125°C	01	3.7	6.0	A
Bias pin current	I _{BIAS}	I _{OUT} = 0 mA to 3.0 A	-55°C to +125°C	01		4	mA
Shutdown supply current (V _{IN})	I _{SHDN}	V _{EN} ≤ 0.4 V	-55°C to +125°C	01		1	μA
Feedback pin current 5/	I _{FB}	I _{OUT} = 50 mA to 3.0 A	-55°C to +125°C	01	-250	250	nA
Power supply rejection ratio (V _{IN} to V _{OUT})	PSRR	1 kHz, I _{OUT} = 1.5 A, V _{IN} = 1.8 V, V _{OUT} = 1.5 V	+25°C	01	73 typical		dB
		800 kHz, I _{OUT} = 1.5 A, V _{IN} = 1.8 V, V _{OUT} = 1.5 V			42 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio (V _{BIAS} to V _{OUT})	PSRR	1 kHz, I _{OUT} = 1.5 A, V _{IN} = 1.8 V, V _{OUT} = 1.5 V	+25°C	01	62 typical		dB
		800 kHz, I _{OUT} = 1.5 A, V _{IN} = 1.8 V, V _{OUT} = 1.5 V			50 typical		
Output noise voltage	Noise	100 Hz to 100 kHz, I _{OUT} = 1.5 A, C _{SS} = 0.001 μF	+25°C	01	16 x V _{OUT} typical		μV _{RMS}
%V _{OUT} droop during load transient	V _{TRAN}	I _{OUT} = 100 mA to 3.0 A at 1 A/μs, C _{OUT} = 0 μF	+25°C	01	4 typical		%V _{OUT}
Minimum startup time	t _{STR}	I _{OUT} = 1.5 A, C _{SS} = open	+25°C	01	100 typical		μs
Soft-start charging current	I _{SS}	V _{SS} = 0.4 V	-55°C to +125°C	01	0.5	1	μA
Enable input high level	V _{EN, hi}		-55°C to +125°C	01	1.1	5.5	V
Enable input low level	V _{EN, lo}		-55°C to +125°C	01	0	0.4	V
Enable pin hysteresis	V _{EN, hys}		+25°C	01	50 typical		mV
Enable pin deglitch time	V _{EN, dg}		+25°C	01	20 typical		μs
Enable pin current	I _{EN}	V _{EN} = 5 V	-55°C to +125°C	01		1	μA
Power good (PG) trip threshold	V _{IT}	V _{OUT} decreasing	-55°C to +125°C	01	86	93.5	%V _{OUT}
PG trip hysteresis	V _{HYS}		+25°C	01	3 typical		%V _{OUT}
PG output low voltage	V _{PG, lo}	I _{PG} = 1 mA (sinking), V _{OUT} < V _{IT}	-55°C to +125°C	01		0.3	V
PG leakage current	I _{PG, lkg}	V _{PG} = 5.25 V, V _{OUT} > V _{IT}	-55°C to +125°C	01		1	μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Operating junction temperature	T _J			01	-55	+125	°C
Thermal shutdown temperature	T _{SD}	Shutdown, temperature increasing	+25°C	01	+155 typical		°C
		Reset, temperature decreasing			+140 typical		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{IN} = C_{BIAS} = 0.1 μF, C_{OUT} = 10 μF, I_{OUT} = 50 mA, and V_{BIAS} = 5.0 V.
- 3/ Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
- 4/ Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
- 5/ I_{FB} current flow is out of the device.

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Case X - continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.031	.039	0.80	1.00
A1	.00	.002	0.00	0.05
A2	0.007 REF		0.20 REF	
b	.009	.015	0.23	0.38
D	.191	.202	4.85	5.15
E	.191	.202	4.85	5.15
e	.025 BSC		0.65 BSC	
e1	.102 BSC		2.60 BSC	
L	.018	.025	0.45	0.65

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance.
3. Falls within reference to JEDEC MO-220.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	OUT
2	NC
3	NC
4	NC
5	IN
6	IN
7	IN
8	IN
9	PG
10	BIAS
11	EN
12	GND
13	NC
14	NC
15	SS
16	FB / SNS
17	NC
18	OUT
19	OUT
20	OUT

FIGURE 2. Terminal connections.

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Terminal symbol	Description
IN	Unregulated input to the device.
EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
SS	Soft start pin. A capacitor connected on this pin to ground sets the start up time. If this pin is left floating, the regulator output soft start ramp time is typically 100 μ s.
BIAS	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	Power good (PG) is an open drain, active high output that indicates the status of VOUT. When VOUT exceeds the PG trip threshold, the PG pin goes into a high impedance state. When VOUT is below this threshold, the pin is driven to a low impedance state. A pull up resistor from 10 k Ω to 1 M Ω should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
FB	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	Regulated output voltage. No capacitor is required on this pin for stability.
NC	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top side plane.
GND	Ground.
PAD / TAB	Should be soldered to the ground plane for increased thermal performance.

FIGURE 2. Terminal connections - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Packaging <u>2/ 3/</u>	Top side marking	Vendor part number
V62/10611-01XE	01295	Reel of 3,000	TPS74401EP	TPS74401MRGWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet or contact the manufacturer.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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