REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Under Table I, Switching specifications, ADC output section, Output clock to data propagation delay (t_{DC}), both LVDS and CMOS mode tests, delete condition “SDR rising edge” and replace with “SDR falling edge”. - ro	13-11-04	C. SAFFLE
B	Add a sentence to footnote 7/ and add new footnote 8/ to SNR test as specified under Table I. Add LVCMOS information to Figure 2 terminal connections. Update document paragraphs to current requirements. - ro	20-04-08	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B	B	B	B															
PAGE	18	19	20	21	22	23															

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 10-07-22	**CHECKED BY** JOSEPH RODENBECK	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 12 BIT, 250 MSPS, ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/10609**
	REV B	**PAGE** 1 **OF** 23

AMSC N/A

5962-V019-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12 bit 250 MSPS analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V6210609	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ISLA112P25MREP	12 bit, 250 MSPS analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	72	See figure 1	Quad flat leadless plastic package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

1.8 V analog supply (AVDD) to analog ground (AVSS)	-0.4 V to 2.1 V
1.8 V output supply (OVDD) to output ground (OVSS)	-0.4 V to 2.1 V
AVSS to OVSS	-0.3 V to 0.3 V
Analog inputs to AVSS	-0.4 V to AVDD + 0.3 V
Clock inputs to AVSS	-0.4 V to AVDD + 0.3 V
Logic inputs to AVSS	-0.4 V to OVDD + 0.3 V
Logic inputs to OVSS	-0.4 V to OVDD + 0.3 V
Junction temperature range (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to ambient (θ_{JA})	24°C/W 2/

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board in free air.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

IPC/JEDEC J STD-020	–	Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figures 4, 5, 6, 7, 8, 9, 10, and 11.

3.5.5 Application information. Detailed application information may be found in the manufacturer's datasheet.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
DC specifications.							
Analog input section.							
Full scale analog input range	V_{FS}	Differential	-55°C to +125°C	01	1.36	1.59	V_{PP}
Input resistance	R_{IN}	Differential	+25°C	01	1000 typical		Ω
Input capacitance	C_{IN}	Differential	+25°C	01	1.9 typical		pF
Full scale range temperature drift	A_{VTC}		+125°C	01	90 typical		ppm / °C
Input offset voltage	V_{OS}		-55°C to +125°C	01	-10	10	mV
Gain error	EG		+25°C	01	2 typical		%
Common mode output voltage	V_{CM}		+25°C	01	0.435	0.635	V
Clock input section.							
Inputs common mode voltage			+25°C	01	0.9 typical		V
CLKP, CLKN input swing			+25°C	01	1.8 typical		V
Power requirements section.							
1.8 V analog supply voltage	AVDD		-55°C to +125°C	01	1.7	1.9	V
1.8 V digital supply voltage	OVDD		-55°C to +125°C	01	1.7	1.9	V
1.8 V analog supply current	I_{AVDD}		-55°C to +125°C	01		96	mA
1.8 V digital supply 4/ current (SDR)	I_{OVDD}	3 mA low voltage differential signaling (LVDS)	-55°C to +125°C	01		76	mA
1.8 V digital supply 4/ current (DDR)	I_{OVDD}	3 mA LVDS	+25°C	01	39 typical		mA
Power supply rejection ratio	PSRR	30 MHz, 200 V_{PP} signal on AVDD	+25°C	01	-36 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 2/		Unit
					Min	Max	
DC specifications - continued.							
Total power dissipation section.							
Normal mode (SDR)	PD	3 mA LVDS	-55°C to +125°C	01		310	mW
Normal mode (DDR)	PD	3 mA LVDS	+25°C	01	234 typical		mW
Nap mode	PD		-55°C to +125°C	01		92	mW
Sleep mode	PD	CSB at logic high	-55°C to +125°C	01		18	mW
Nap mode wakeup time 5/		Sample clock running	+25°C	01	1 typical		µs
Sleep mode wakeup time 5/		Sample clock running	+25°C	01	1 typical		ms
AC specifications. 6/							
Differential nonlinearity	DNL		-55°C to +125°C	01	-0.9	+0.9	LSB
Integral nonlinearity	INL		-55°C to +125°C	01	-2.0	+2.0	LSB
Minimum conversion rate 7/	f_S MIN		-55°C to +125°C	01		40	MSPS
Maximum conversion rate	f_S MAX		-55°C to +125°C	01	250		MSPS
Signal to noise ratio 8/	SNR	f_{IN} = 10 MHz	+25°C	01	66.1 typical		dBFS
		f_{IN} = 105 MHz	-55°C to +125°C		62.7		
		f_{IN} = 190 MHz	+25°C		65.9 typical		
		f_{IN} = 364 MHz	+25°C		65.4 typical		
		f_{IN} = 695 MHz	+25°C		63.8 typical		
		f_{IN} = 995 MHz	+25°C		62.6 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
AC specifications - continued. 6/							
Signal to noise and distortion	SINAD	f_{IN} = 10 MHz	+25°C	01	65.3 typical		dBFS
		f_{IN} = 105 MHz	-55°C to +125°C		62.2		
		f_{IN} = 190 MHz	+25°C		64.6 typical		
		f_{IN} = 364 MHz	+25°C		63.9 typical		
		f_{IN} = 695 MHz	+25°C		56.9 typical		
		f_{IN} = 995 MHz	+25°C		49.6 typical		
Effective number of bits	ENOB	f_{IN} = 10 MHz	+25°C	01	10.6 typical		Bits
		f_{IN} = 105 MHz	-55°C to +125°C		10.1		
		f_{IN} = 190 MHz	+25°C		10.4 typical		
		f_{IN} = 364 MHz	+25°C		10.3 typical		
		f_{IN} = 695 MHz	+25°C		9.2 typical		
		f_{IN} = 995 MHz	+25°C		7.9 typical		
Spurious free dynamic range	SFDR	f_{IN} = 10 MHz	+25°C	01	83.0 typical		dBc
		f_{IN} = 105 MHz	-55°C to +125°C		67		
		f_{IN} = 190 MHz	+25°C		79 typical		
		f_{IN} = 364 MHz	+25°C		76 typical		
		f_{IN} = 695 MHz	+25°C		61 typical		
		f_{IN} = 995 MHz	+25°C		51 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
AC specifications - continued. 6/							
Intermodulation distortion	IMD	f_{IN} = 70 MHz	+25°C	01	-86 typical		dBFS
		f_{IN} = 170 MHz	+25°C		-97 typical		
Word error rate	WER		+25°C	01	10^{-12} typical		
Full power dissipation	FPBW		+25°C	01	1300 typical		MHz
Digital specifications.							
Inputs section.							
Input current high (SDIO, RESETN)	I_{IH}	V_{IN} = 1.8 V	-55°C to +125°C	01	-1	1	µA
Input current low (SDIO, RESETN)	I_{IL}	V_{IN} = 0 V	-55°C to +125°C	01	-25	-5	µA
Input voltage high (SDIO, RESETN)	V_{IH}		-55°C to +125°C	01	1.17		V
Input voltage low (SDIO, RESETN)	V_{IL}		-55°C to +125°C	01		0.63	V
Input current high 9/ (OUTMODE, NAPSLP, CLKDIV, OUTFMT)	I_{IH}		-55°C to +125°C	01	15	40	µA
Input current low (OUTMODE, NAPSLP, CLKDIV, OUTFMT)	I_{IL}		-55°C to +125°C	01	-40	-15	µA
Input capacitance	C_{DI}		+25°C	01	3 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
Digital specifications - continued.							
Low voltage differential signaling (LVDS) outputs section.							
Differential output voltage	V_T	3 mA mode	+25°C	01	620 typical		mV_{PP}
Output offset voltage	V_{OS}	3 mA mode	-55°C to +125°C	01	950	980	mV
Output rise time	t_R		+25°C	01	500 typical		ps
Output fall time	t_F		+25°C	01	500 typical		ps
CMOS output section.							
Voltage output high	V_{OH}	I_{OH} = -500 μA	-55°C to +125°C	01	OVDD - 0.3		V
Voltage output low	V_{OL}	I_{OL} = 1 mA	-55°C to +125°C	01		0.3	V
Output rise time	t_R		+25°C	01	1.8 typical		ns
Output fall time	t_F		+25°C	01	1.3 typical		ns
Switching specifications.		See figures 4 and 5.					
ADC output section							
Aperture delay	t_A		+25°C	01	375 typical		ps
RMS aperture jitter	j_A		+25°C	01	60 typical		fs
Output clock to 10/ 11/ data propagation delay, LVDS mode	t_{DC}	DDR rising edge	-55°C to +125°C	01	-260	120	ps
		DDR falling edge			-160	230	
		SDR falling edge			-260	230	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
Switching specifications.							
ADC output section - continued.		See figures 4 and 5.					
Output clock to data propagation delay, CMOS mode 10/	t_{DC}	DDR rising edge	-55°C to +125°C	01	-220	200	ps
		DDR falling edge			-310	110	
		SDR falling edge			-310	200	
Latency (pipeline delay)	L		+25°C	01	7.5 typical		cycles
Overvoltage recovery	t_{OVR}		+25°C	01	1 typical		cycles
SPI interface section.	11/ 12/ 13/	See figures 8 and 9.					
SCLK period	t_{CLK}	Write operation	-55°C to +125°C	01	16		cycles 8/
		Read operation			66		cycles
SCLK duty cycle	t_{HI} / t_{CLK} or t_{LO} / t_{CLK}	Read or write	-55°C to +125°C	01	25	75	%
CSB↓ to SCLK↑ setup time	t_S	Read or write	-55°C to +125°C	01	1		cycles
CSB↑ after SCLK↑ hold time	t_H	Read or write	-55°C to +125°C	01	3		cycles
Data valid to SCK↑ setup time	t_{DSW}	Write	-55°C to +125°C	01	1		cycles
Data valid after SCK↑ hold time	t_{DHW}	Write	-55°C to +125°C	01	3		cycles

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
Switching specifications.							
SPI interface section - continued. 11/ 12/ 13/ See figures 8 and 9.							
Data valid after SCK↓ time	t_{DVR}	Read	-55°C to +125°C	01		16.5	cycles
Data invalid after SCK↑ time	t_{DHR}	Read	-55°C to +125°C	01	3		cycles
Sleep mode 14/ CSB↓ to SCLK↑ setup time	t_S	Read or write in sleep mode	-55°C to +125°C	01	150		µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AVDD = 1.8 V, OVDD = 1.8 V, A_{IN} = -1 dBFS, f_{SAMPLE} = maximum conversion rate (per speed grade).

3/ Parameters with min and/or max limits are 100% production tested at their worst case temperature extreme (+125°C).

4/ Digital supply current is dependent upon the capacitive loading of the loading of the digital outputs. I_{OVDD} specifications apply for 10 pF load on each digital output.

5/ See nap / sleep mode description in the datasheet for more details

6/ AC specifications apply after internal calibration of the analog digital converter is invoked at the given sample rate and temperature. Refer to “power on calibration” and “user initiated reset” in the device datasheet for more details.

7/ The DLL range setting must be changed for low speed operation. See the “Serial Peripheral Interface” section in the manufacturer’s datasheet for more details.

8/ To ensure device accuracy the measurement temperature is to be within 60°C of the calibration temperature.

9/ The tri-level inputs internal switching thresholds are approximately 0.43 V and 1.34 V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.

10/ The input clock to output clock delay is a function of sample rate, using the output clock to latch the data simplifies data capture for most application.

11/ Parameter guaranteed by characterization and not 100% tested.

12/ Serial peripheral interface (SPI) interface timing is directly proportional to the ADC sample period (t_S). 4 ns at 250 MSPS. Minimum and maximum limits guaranteed by characterization, and not 100% tested.

13/ The SPI may operate asynchronously with respect to the ADC sample clock.

14/ The SPI chip select (CSB) setup time increases in sleep mode due to the reduced power state, CSB setup time in nap mode is equal to normal mode CSB setup time (4 ns minimum).

Case X

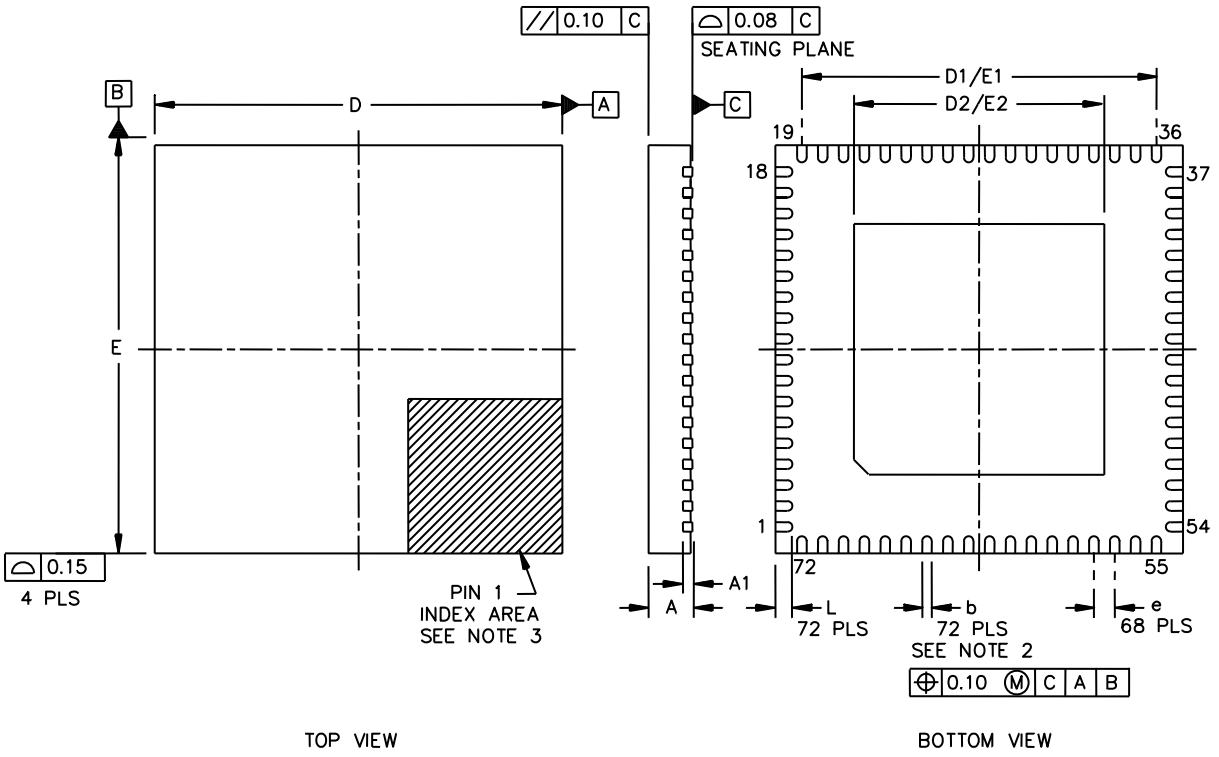

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV B	PAGE 12

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.035	---	0.90
A1	---	0.007	---	0.2
b	0.009	---	0.24	---
D/E	0.393 BSC		10.00 BSC	
D1/E1	0.334 BSC		8.50 BSC	
D2/E2	0.236 BSC		6.00 BSC	
e	0.019 BSC		0.50 BSC	
L	0.015	---	0.40	---
N		72		72

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension b applies to the metalized terminal and is measured between 0.15 mm (0.006 inch) and 0.30 mm (0.012 inch) from the terminal tip.
3. The configuration of the pin 1 identifier is optional, but must be located within the zone indicated. The pin 1 identifier may be either a mold or mark feature.

FIGURE 1. Case outline - continued.

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AVDD	25	RESETN	49	D6N
2	DNC	26	OVSS	50	D6P
3	DNC	27	OVDD	51	D7N
4	DNC	28	DNC	52	D7P
5	DNC	29	DNC	53	D8N
6	AVDD	30	DNC	54	D8P
7	AVSS	31	DNC	55	OVSS
8	AVSS	32	D0N	56	OVDD
9	VINN	33	D0P	57	D9N
10	VINP	34	D1N	58	D9P
11	AVSS	35	D1P	59	D10N
12	AVDD	36	OVDD	60	D10P
13	DNC	37	D2N	61	D11N
14	DNC	38	D2P	62	D11P
15	VCM	39	D3N	63	ORN
16	CLKDIV	40	D3P	64	ORP
17	DNC	41	D4N	65	OVSS
18	DNC	42	D4P	66	SDO
19	AVDD	43	D5N	67	CSB
20	CLKP	44	D5P	68	SCLK
21	CLKN	45	OVSS	69	SDIO
22	OUTMODE	46	RLVDS	70	OUTFMT
23	NAPSLP	47	CLKOUTN	71	AVDD
24	AVDD	48	CLKOUTP	72	AVSS

FIGURE 2. Terminal connections.

Terminal symbol	LVDS [LVCMOS] function SDR mode	DDR mode comments
AVDD	1.8 V analog supply.	
DNC	Do not connect.	
AVSS	Analog ground.	
VINN, VINP	Analog input negative, positive.	
VCM	Common mode output.	
CLKDIV	Clock divider control.	
CLKP, CLKN	Clock input true, complement.	
OUTMODE	Output mode (LVDS).	
NAPSLP	Power control, (nap, sleep modes).	
RESETN	Power on reset (active low).	
OVSS	Output ground.	
OVDD	1.8 V output supply.	
D0N [NC]	LVDS bit 0 (LSB) output complement. [NC IN LVCMOS]	DDR logical bits 1, 0 (LVDS)
D0P [D0]	LVDS bit 0 (LSB) output true. [LVCMOS bit 0]	DDR logical bits 1, 0 (LVDS or CMOS)
D1N [NC]	LVDS bit 1 output complement. [NC in LVCMOS]	NC in DDR
D1P [D1]	LVDS bit 1 output true. [LVCMOS bit 1]	NC in DDR
D2N [NC]	LVDS bit 2 output complement. [NC in LVCMOS]	DDR logical bits 3, 2 (LVDS)
D2P [D2]	LVDS bit 2 output true. [LVCMOS bit 2]	DDR logical bits 3, 2 (LVDS or CMOS)
D3N [NC]	LVDS bit 3 output complement. [NC in LVCMOS]	NC in DDR
D3P [D3]	LVDS bit 3 output true. [LVCMOS bit 3]	NC in DDR
D4N [NC]	LVDS bit 4 output complement. [NC in LVCMOS]	DDR logical bits 5, 4 (LVDS)
D4P [D4]	LVDS bit 4 output true. [LVCMOS bit 4]	DDR logical bits 5, 4 (LVDS or CMOS)
D5N [NC]	LVDS bit 5 output complement. [NC in LVCMOS]	NC in DDR
D5P [D5]	LVDS bit 5 output true. [LVCMOS bit 5]	NC in DDR

FIGURE 2. Terminal connections - continued.

Terminal symbol	LVDS [LVCMOS] function SDR mode	DDR mode comments
RLVDS	LVDS bias resistor (connect to OVSS with a 10 kΩ 1% resistor).	
CLKOUTN [NC]	LVDS clock output complement. [NC in LVCMOS]	
CLKOUTP [CLKOUT]	LVDS clock output true. [LVCMOS CLKOUT]	
D6N [NC]	LVDS bit 6 output complement. [NC in LVCMOS]	DDR logical bits 7, 6 (LVDS)
D6P [D6]	LVDS bit 6 output true. [LVCMOS bit 6]	DDR logical bits 7, 6 (LVDS or CMOS)
D7N [NC]	LVDS bit 7 output complement. [NC in LVCMOS]	NC in DDR
D7P [D7]	LVDS bit 7 output true. [LVCMOS bit 7]	NC in DDR
D8N [NC]	LVDS bit 8 output complement. [NC in LVCMOS]	DDR logical bits 9, 8 (LVDS)
D8P [D8]	LVDS bit 8 output true. [LVCMOS bit 8]	DDR logical bits 9, 8 (LVDS or CMOS)
D9N [NC]	LVDS bit 9 output complement. [NC in LVCMOS]	NC in DDR
D9P [D9]	LVDS bit 9 output true. [LVCMOS bit 9]	NC in DDR
D10N [NC]	LVDS bit 10 output complement. [NC in LVCMOS]	DDR logical bits 11, 10 (LVDS)
D10P [D10]	LVDS bit 10 output true. [LVCMOS bit 10]	DDR logical bits 11, 10 (LVDS or CMOS)
D11N [NC]	LVDS bit 11 output complement. [NC in LVCMOS]	NC in DDR
D11P [D11]	LVDS bit 11 output true. [LVCMOS bit 11]	NC in DDR
ORN [NC]	LVDS over range complement. [NC in LVCMOS]	
ORP [OR]	LVDS over range true. [LVCMOS over range]	
SDO	Serial peripheral interface (SPI) serial data output (4.7 kΩ pull-up to OVDD is required).	
CSB	SPI chip select (active low).	
SCLK	SPI clock.	
SDIO	SPI serial data input/output.	
OUTFMT	Output data format (two's complement, gray code, offset binary).	
AVSS	Analog ground.	

NOTE: SDR is the default state at power up the package.

FIGURE 2. Terminal connections - continued.

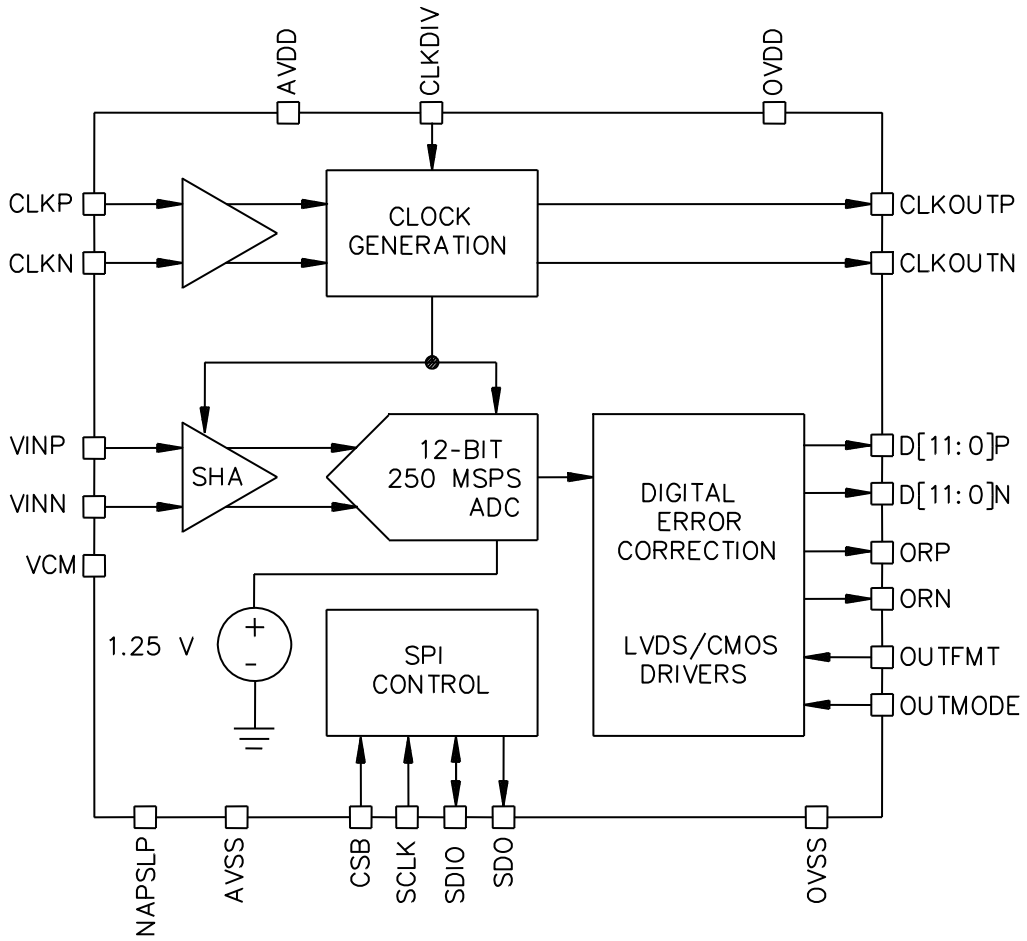

FIGURE 3. Block diagram.

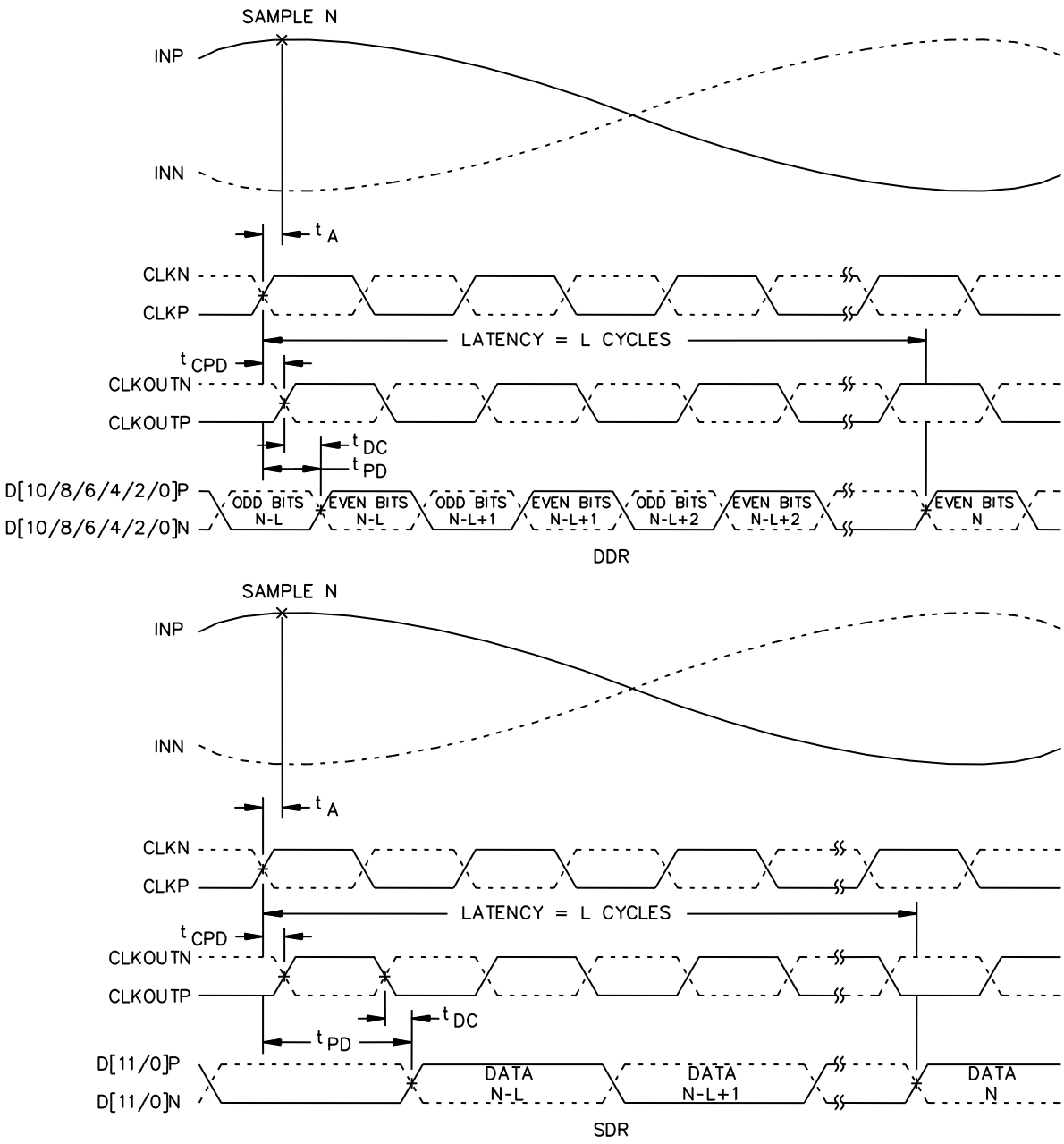

FIGURE 4. LVDS timing waveforms.

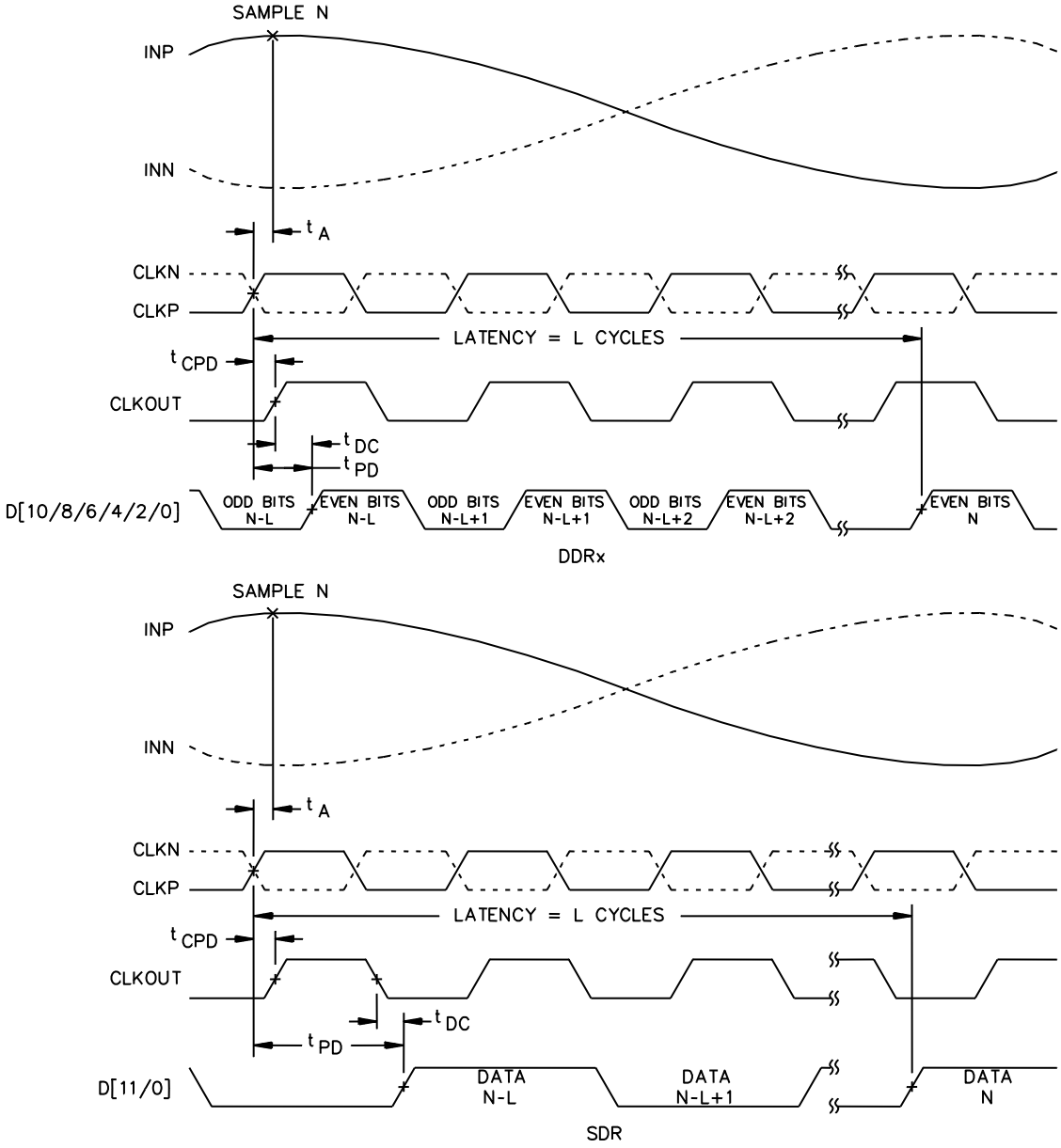

FIGURE 5. CMOS timing waveforms.

Input voltage	Offset binary	Two's complement	Gray code
-Full scale	000 00 000 00 00	100 00 000 00 00	000 00 000 00 00
-Full scale + 1 LSB	000 00 000 00 01	100 00 000 00 01	000 00 000 00 01
Mid-scale	100 00 000 00 00	000 00 000 00 00	110 00 000 00 00
+Full scale - 1 LSB	111 11 111 11 10	011 11 111 11 10	100 00 00 00 01
+Full scale	111 11 111 11 11	011 11 111 111 1	100 00 000 00 00

Input voltage to output code mapping

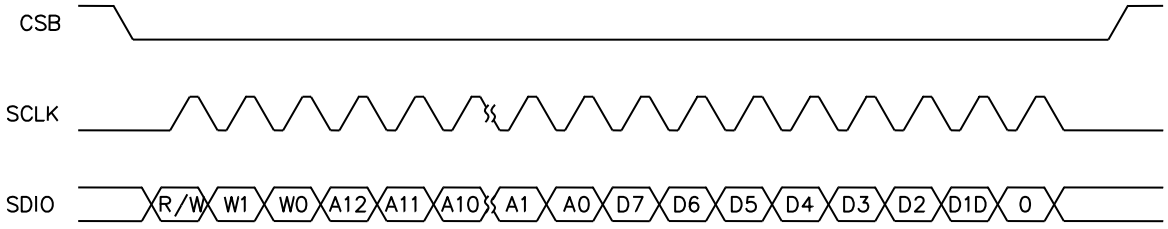

FIGURE 6. MSB first addressing waveforms.

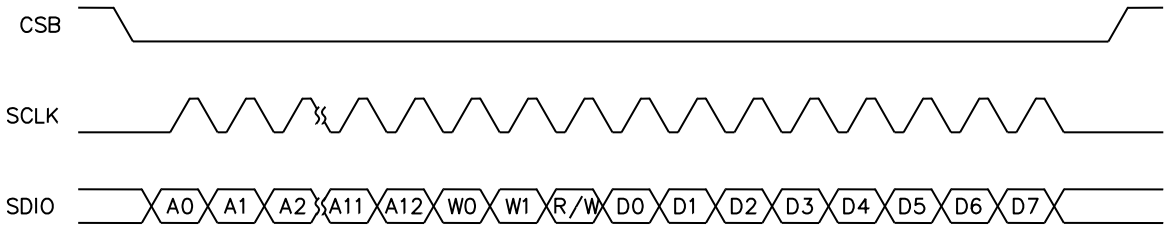

FIGURE 7. LSB first addressing waveforms.

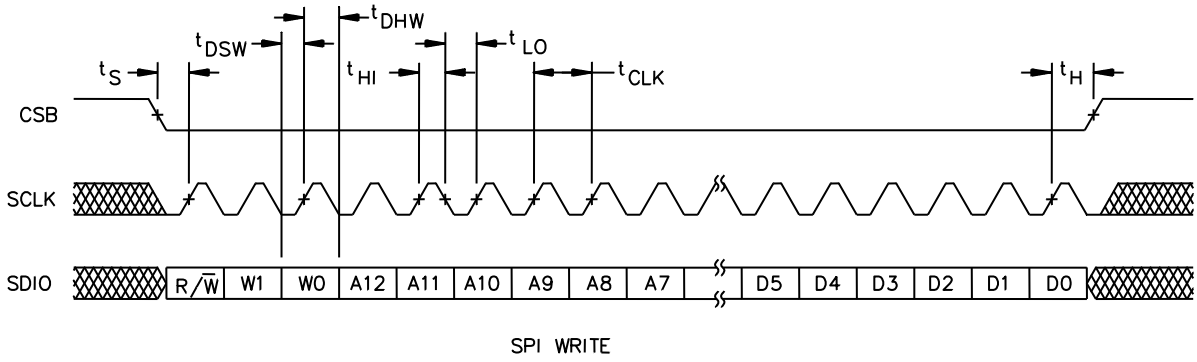

FIGURE 8. SPI write waveforms.

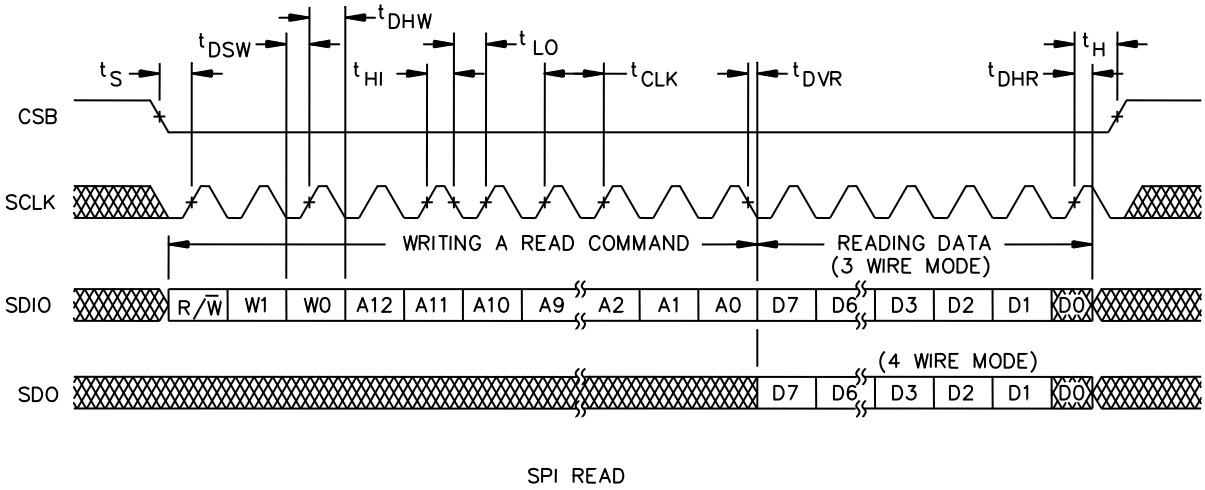

FIGURE 9. SPI read waveforms.

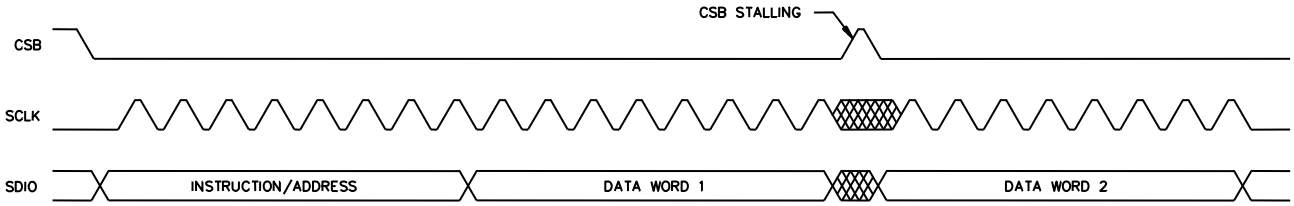

FIGURE 10. 2 byte transfer waveforms.

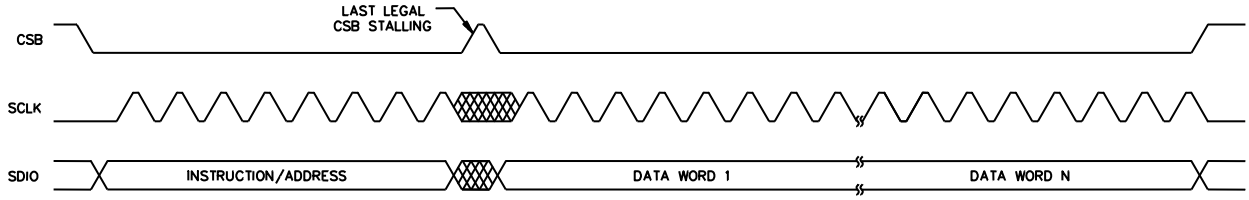

FIGURE 11. N byte transfer waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Part marking 2/	Vendor part number
V62/10609-01XE	34371	ISLA112P25MREP	ISLA112P25MREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ This lead (Pb) free plastic package employ special Pb free material sets; molding compounds/die attach materials and nickel (Ni), Pb, and gold (Au) plate - precious metals (e4) termination finish, which Restriction of Hazardous Substances Directive (RoHS) compliant and compatible with both tin lead (SnPb) and Pb free soldering operations. This Pb free device is moisture sensitivity level (MSL) classified at Pb free peak reflow temperatures that meet or exceed the Pb free requirements of IPC/JEDEC J STD-020.

CAGE code	Source of supply
34371	Renesas Electronics America, Inc. 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406