

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a ultralow power, 10 mA, low dropout voltage regulator microcircuit, with an operating temperature range of -55°C to +150°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| | | | | |
|--|---|--|--|---|
| <u>V62/10607</u> Drawing number | - | <u>01</u> Device type (See 1.2.1) | <u>X</u> Case outline (See 1.2.2) | <u>E</u> Lead finish (See 1.2.3) |
|--|---|--|--|---|

1.2.1 Device type(s).

| | | |
|--------------------|----------------|--|
| <u>Device type</u> | <u>Generic</u> | <u>Circuit function</u> |
| 01 | TPS76901-EP | Ultralow power, 10 mA, low dropout voltage regulator |

1.2.2 Case outline(s). The case outline(s) are as specified herein.

| | | | |
|-----------------------|-----------------------|---------------------|-----------------------|
| <u>Outline letter</u> | <u>Number of pins</u> | <u>JEDEC PUB 95</u> | <u>Package style</u> |
| X | 5 | MO-178-AA | Plastic surface mount |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

| | |
|--------------------------|----------------------|
| <u>Finish designator</u> | <u>Material</u> |
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

| | | | |
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1.3 Absolute maximum ratings. 1/

| | |
|--|----------------------------------|
| Input voltage range (V_{REF}) | -0.3 V to 13.5 V 2/ |
| Voltage range at \overline{EN} | -0.3 V to $V_{IN} + 0.3$ V |
| Voltage on OUT, FB | 7 V |
| Peak output current | Internally limited |
| Electrostatic discharge rating: | |
| Human body model (HBM) | 2 kV |
| Continuous total power dissipation | See 1.5 thermal characteristics. |
| Operating virtual junction temperature range (T_J) | -55°C to +150°C |

1.4 Recommended operating conditions. 3/

| | |
|--|-------------------|
| Input voltage range (V_{IN}) | 5 V to 10 V 4/ |
| Output voltage range (V_{OUT}) | 1.2 V to 4.5 V |
| Continuous output current (I_{OUT}) | 0 mA to 100 mA 5/ |
| Operating junction temperature range (T_J) | -55°C to +150°C |

1.5 Thermal characteristics.

| Board | θ_{JC} | θ_{JA} | Derating factor above $T_A = 25^\circ\text{C}$ |
|-----------|---------------|---------------|---|
| Low K 6/ | 65.8°C/W | 259°C/W | 3.9 mW/°C |
| High K 7/ | 65.8°C/W | 180°C/W | 5.6 mW/°C |

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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ All voltage limits are with respect to network ground terminal.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 4/ To calculate the minimum input voltage for maximum output current, use the following formula:
 $V_{IN}(\text{min}) = V_{OUT}(\text{max}) + V_{DO}(\text{max load})$.
- 5/ Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this paragraph for extended periods of time.
- 6/ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
- 7/ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Conditions | Temperature, T _J | Device type | Limits | | Unit |
|--|--------------------|---|-----------------------------|-------------|--------------------------|-------------------------|-------|
| | | | | | Min | Max | |
| Output voltage <u>2/</u> (10 μA to 100 mA load) | V _{OUT} | 12 V ≤ V _{OUT} ≤ 4.5 V | +25°C | 01 | V _{OUT} typical | | V |
| | | | -55°C to +150°C | | 0.97 x V _{OUT} | 1.03 x V _{OUT} | |
| Quiescent current <u>2/</u> (GND current) | I _Q | $\overline{EN} = 0 V,$ 0 mA < I _{OUT} < 100 mA | +25°C | 01 | 17 typical | | μA |
| | | $\overline{EN} = 4 V,$ I _{OUT} = 100 mA | -55°C to +150°C | | | 28 | |
| Load regulation | | $\overline{EN} = 0 V,$ I _{OUT} = 0 mA to 100 mA | +25°C | 01 | 12 typical | | mV |
| | | | +150°C | | 13.5 typical | | |
| Output voltage line <u>3/</u> regulation (ΔV _{OUT} / V _{OUT}) | | 5 V ≤ V _{IN} ≤ 10 V <u>2/</u> | +25°C | 01 | 0.04 typical | | % |
| | | | -55°C to +150°C | | | 0.1 | |
| Output noise voltage | V _N | BW = 300 Hz to 50 kHz, C _{OUT} = 10 μF | +25°C | 01 | 190 typical | | μVrms |
| Output current limit | | V _{OUT} = 0 V <u>2/</u> | +25°C | 01 | 350 typical | | mA |
| | | | -55°C to +150°C | | | 750 | |
| Standby current | I _{STDBY} | $\overline{EN} = V_{IN},$ 5 V ≤ V _{IN} ≤ 10 V | +25°C | 01 | 1 typical | | μA |
| | | | -55°C to +150°C | | | 2.4 | |
| Feedback (FB) input current | I _{FB} | FB = 1.18 V | -55°C to +150°C | 01 | -1 | 1 | μA |
| High level enable input voltage | V _{IH} | 5 V ≤ V _{IN} ≤ 10 V | +25°C | 01 | 1.7 | | V |
| Low level enable input voltage | V _{IL} | 5 V ≤ V _{IN} ≤ 10 V | +25°C | 01 | | 0.9 | V |
| | | | +150°C | | 0.75 typical | | |

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

| Test | Symbol | Conditions | Temperature, T _A | Device type | Limits | | Unit |
|-------------------------------|-----------------|---|--------------------------------|----------------|------------|-----|------|
| | | | | | Min | Max | |
| Power supply ripple rejection | PSRR | f = 1 kHz, C _{OUT} = 10 μF <u>2/</u> | +25°C | 01 | 60 typical | | dB |
| Input current | I _{IN} | $\overline{EN} = 0\text{ V}$ | -55°C to +150°C | 01 | -1 | 1 | μA |
| | | $\overline{EN} = V_{IN}$ | | | -1 | 1 | |

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Minimum INPUT operating voltage is 5 V. Maximum INPUT voltage 10 V, minimum output current 10 μA, maximum output current 100 mA.

3/ Line regulation (%) = (ΔV_{OUT}) / (ΔV_{IN}) x 100.

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Case X

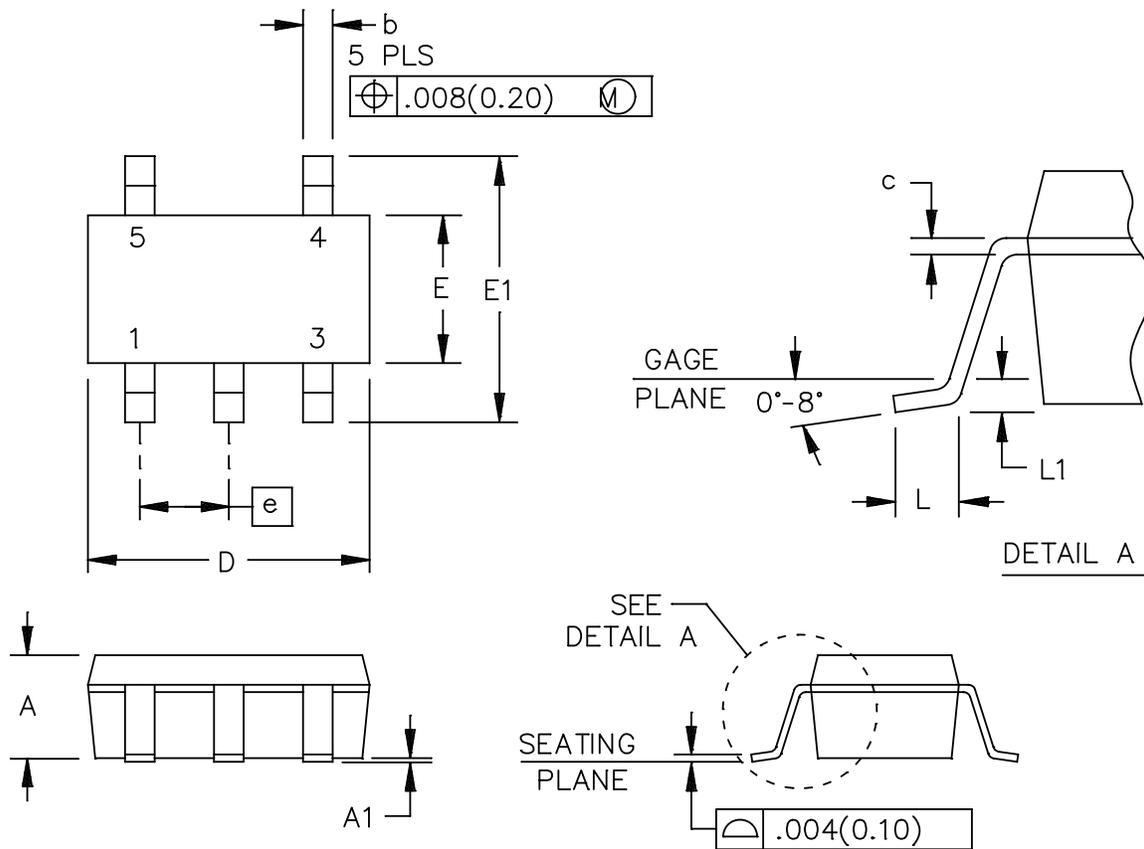


FIGURE 1. Case outline.

| | | | |
|--|--------------------------|--|-------------------------------------|
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Case X – continued.

| Symbol | Dimensions | | | |
|--------|------------|------|-------------|------|
| | Inch | | Millimeters | |
| | Min | Max | Min | Max |
| A | --- | .057 | --- | 1.45 |
| A1 | .000 | .006 | 0.00 | 0.15 |
| b | .011 | .019 | 0.30 | 0.50 |
| c | .003 | .008 | 0.08 | 0.22 |
| D | .108 | .120 | 2.75 | 3.05 |
| E | .057 | .068 | 1.45 | 1.75 |
| E1 | .102 | .118 | 2.60 | 3.00 |
| e | .037 BSC | | 0.95 BSC | |
| L | .011 | .023 | 0.30 | 0.60 |
| L1 | .009 BSC | | 0.25 BSC | |
| n | 5 leads | | 5 leads | |

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.006 inch) per end.
3. Falls within JEDEC MO-178 variation AA.

FIGURE 1. Case outline – Continued.

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| Device type | 01 | | |
|-----------------|------------------------|-------|-------------|
| Case outline | X | | |
| Terminal number | Terminal symbol | I / O | Description |
| 1 | INPUT | I | Input |
| 2 | GND | --- | Ground |
| 3 | $\overline{\text{EN}}$ | I | Enable |
| 4 | FB | I | Feedback |
| 5 | OUTPUT | O | Output |

FIGURE 2. Terminal connections.

| | | | |
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

| Vendor item drawing administrative control number <u>1/ 2/ 3/</u> | Device manufacturer CAGE code | Top side marking | Vendor part number |
|---|-------------------------------|------------------|--------------------|
| V62/10607-01XE | 01295 | PCFS | TPS76901SDBVTEP |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet , or use website www.ti.com.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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