REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current VID description requirements. - PHN	22-03-22	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

PMIC N/A

Original date of drawing

YY MM DD

14-04-07

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TITLE
MICROCIRCUIT, LINEAR, 1-Mbps QUAD DIGITAL ISOLATORS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/10606
REV A		PAGE 1 OF 16

AMSC N/A

5962-V024-22

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1-Mbps quad digital isolators microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/10606	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ISO7241A-EP	1-Mbps quad digital isolators

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MS-013-AA	Plastic Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage, (V_{CC}, V_{CC1}, V_{CC2}) ..... -0.5 V to 6.0 V 2/
Voltage at IN, OUT, EN (V_I) ..... -0.5 V to 6.0 V
Output current, (I_O) ..... ±15 mA
Electrostatic discharge, (ESD), All pins
Human body Model (JEDEC Standard 22, Test Method A114C-01) ..... ±4 kV
Field Induced Charged Device (JEDEC Standard 22, Test method C101) ..... ±1 kV
Machine Model (ANSI/ESDS5.2-1996) ..... ±200 V
Maximum junction temperature ..... 170°C

1.4 Recommended operating conditions. 3/

Supply voltage range, (V_{CC}, V_{CC1}, V_{CC2}) ..... 3.15 V to 5.5 V 4/
Maximum high level output current, (I_{OH}) ..... 4 mA
Minimum low level output current, (I_{OL}) ..... -4 mA
Minimum input pulse width, (t_{ui}) ..... 1 µs
Signaling rate ($1/t_{ui}$) ..... 0 to 1000 kbps
High level input voltage, (V_{IH}) (IN) (EN on all devices) ..... 2 V to VCC
Low level input voltage, (V_{IL}) (IN) (EN on all devices) ..... 0 V to 0.8 V
Maximum junction temperature ..... 150°C
Maximum external magnetic field-strength immunity
per IEC 61000-4-8 and IEC 61000-4-9 certification (H) ..... 1000 A/m
Maximum device power dissipation ..... 220 mW 5/

1.5 Thermal characteristics.

Parameter		TYP	Units
Junction to air θ_{JA}	Low K thermal resistance 6/	168	°C/W
	High K thermal resistance	96.1	
Junction to board thermal	resistance, θ_{JB}	61	
Junction to case thermal	resistance, θ_{JC}	48	

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to network ground terminal and are peak voltage values.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
4/ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.
5/ $V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, Input a 50% duty cycle square wave.
6/ Tested in accordance with the Low-K or High-K thermal metric definition EIA/JESD51-3 for leaded surface mount packages.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD22	–	Qualification Testing for Plastic Encapsulated Solid State Devices – Electro Static Discharge (ESD) protection.
JESD51-3	–	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

(Copies of these documents are available online at https://www.jedec.org).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI/ESDS5.2 – Electrostatic Discharge Sensitivity Testing - Machine Model (MM) -

(Copies of these documents are available online at https:/www.ansi.org.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function diagram. The function diagram shall be as shown in figure 3.

3.5.4 Device I/O schematic. The device I/O schematic shall be as shown in figure 4.

3.5.5 Device function table. The device function table shall be as shown in figure 5.

3.5.6 Switching characteristic test circuit and voltage waveforms. The switching characteristic test circuit and voltage waveforms shall be as shown in figure 6.

3.5.7 Enable/Disenable propagation delay time test circuit and waveform. The Enable/Disenable propagation delay time test circuit and waveform shall be as shown in figure 7.

3.5.8 Failsafe delay time test circuit and voltage waveforms. The failsafe delay time test circuit and voltage waveforms shall be as shown in figure 8.

3.5.9 Common mode transient immunity test circuit and voltage waveforms. The common mode transient immunity test circuit and voltage waveforms shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
ELECTRICAL CHRACTERISTIC: V_{CC1} and V_{CC2} at 5-V 3/ OPERATION						
Supply current						
Quiescent 1 Mbps	I_{CC1}	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
Quiescent 1 Mbps	I_{CC2}	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
Electrical characteristics						
Sleep mode output current	I_{OFF}	EN at 0 V, Single channel		0		µA
High level output voltage	V_{OH}	I_{OH} = -4 mA, See FIGURE 6	V_{CC} – 0.8			V
		I_{OH} = -20 µA, See FIGURE 6	V_{CC} – 0.1			
Low level output voltage	V_{OL}	I_{OL} = 4 mA, See FIGURE 6			0.4	
		I_{OL} = 20 µA, See FIGURE 6			0.1	
Input voltage hysteresis	$V_{I(HYS)}$			150		mV
High level input current	I_{IH}	IN from 0 V to V_{CC}			10	µA
Low level input current	I_{IL}		-10			
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, See FIGURE 9	25	50		kV/µs
SWITCHING CHRACTERISTIC: V_{CC1} and V_{CC2} at 5-V OPERATION						
Propagation delay	t_{PLH}, t_{PHL}	See FIGURE 6	40		95	ns
Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ 4/	PWD				10	
Channel to channel output skew	$t_{sk(o)}$				2	
Output signal rise time	t_r	See FIGURE 6		2		
Output signal fall time	t_f			2		
Propagation delay, high level to high impedance output	t_{PHZ}			15	20	
Propagation delay, high impedance to high level output	t_{PZH}	See FIGURE 7		15	20	
Propagation delay, low level to high impedance output	t_{PLZ}			15	20	
Propagation delay, high impedance to low level output	t_{PZL}			15	20	
Fail safe output delay time from input power loss	t_{fs}	See FIGURE 8		12		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
ELECTRICAL CHRACTERISTIC: V_{CC1} at 5 V, V_{CC2} at 3.3-V 3/ OPERATION						
Supply current						
Quiescent	I_{CC1}	V_I = V_{CC} or 0 V, All channels, no load,		6.5	11	mA
1 Mbps		EN_1 at 3 V, EN_2 at 3 V				
Quiescent	I_{CC2}	V_I = V_{CC} or 0 V, All channels, no load,		8	13	mA
1 Mbps		EN_1 at 3 V, EN_2 at 3 V		8	13	
Electrical characteristics						
Sleep mode output current	I_{OFF}	EN at 0 V, Single channel		0		µA
High level output voltage	V_{OH}	I_{OH} = -4 mA, See FIGURE 6 (5-V side)	V_{CC} – 0.8			V
		I_{OH} = -20 µA, See FIGURE 6	V_{CC} – 0.1			
Low level output voltage	V_{OL}	I_{OL} = 4 mA, See FIGURE 6			0.4	
		I_{OL} = 20 µA, See FIGURE 6			0.1	
Input voltage hysteresis	$V_{I(HYS)}$			150		mV
High level input current	I_{IH}	IN from 0 V to V_{CC}			10	µA
Low level input current	I_{IL}		-10			
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, See FIGURE 9	25	50		kV/µs
SWITCHING CHRACTERISTIC: V_{CC1} at 5 V, V_{CC2} at 3.3-V OPERATION						
Propagation delay	t_{PLH}, t_{PHL}	See FIGURE 6	40		100	ns
Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ 4/	PWD				11	
Channel to channel output skew	$t_{sk(o)}$				3	
Output signal rise time	t_r	See FIGURE 6		2		
Output signal fall time	t_f			2		
Propagation delay, high level to high impedance output	t_{PHZ}	See FIGURE 7		15	20	
Propagation delay, high impedance to high level output	t_{PZH}			15	20	
Propagation delay, low level to high impedance output	t_{PLZ}			15	20	
Propagation delay, high impedance to low level output	t_{PZL}			15	20	
Fail safe output delay time from input power loss	t_{fs}	See FIGURE 8		18		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
ELECTRICAL CHRACTERISTIC: V_{CC1} at 3.3 V, V_{CC2} at 5-V 3/ OPERATION						
Supply current						
Quiescent	I_{CC1}	V_I = V_{CC} or 0 V, All channels, no load,		4	7	mA
1 Mbps		EN_1 at 3 V, EN_2 at 3 V		4	7	
Quiescent	I_{CC2}	V_I = V_{CC} or 0 V, All channels, no load,		13	20	mA
1 Mbps		EN_1 at 3 V, EN_2 at 3 V		13	20	
Electrical characteristics						
Sleep mode output current	I_{OFF}	EN at 0 V, Single channel		0		µA
High level output voltage	V_{OH}	I_{OH} = -4 mA, See FIGURE 6 (5-V side)	V_{CC} – 0.8			V
		I_{OH} = -20 µA, See FIGURE 6	V_{CC} – 0.1			
Low level output voltage	V_{OL}	I_{OL} = 4 mA, See FIGURE 6			0.4	
		I_{OL} = 20 µA, See FIGURE 6			0.1	
Input voltage hysteresis	$V_{I(HYS)}$			150		mV
High level input current	I_{IH}	IN from 0 V to V_{CC}			10	µA
Low level input current	I_{IL}		-10			
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, See FIGURE 9	25	50		kV/µs
SWITCHING CHRACTERISTIC: V_{CC1} at 3.3 V, V_{CC2} at 5-V OPERATION						
Propagation delay	t_{PLH}, t_{PHL}	See FIGURE 6	40		100	ns
Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ 4/	PWD				11	
Channel to channel output skew	$t_{sk(o)}$				2.5	
Output signal rise time	t_r	See FIGURE 6		2		
Output signal fall time	t_f			2		
Propagation delay, high level to high impedance output	t_{PHZ}	See FIGURE 7		15	20	
Propagation delay, high impedance to high level output	t_{PZH}			15	20	
Propagation delay, low level to high impedance output	t_{PLZ}			15	20	
Propagation delay, high impedance to low level output	t_{PZL}			15	20	
Fail safe output delay time from input power loss	t_{fs}	See FIGURE 8		12		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
ELECTRICAL CHRACTERISTIC: V_{CC1} and V_{CC2} at 3.3-V 3/ OPERATION						
Supply current						
Quiescent	I_{CC1}	V_I = V_{CC} or 0 V, All channels, no load,		4	7	mA
1 Mbps		EN_1 at 3 V, EN_2 at 3 V		4	7	
Quiescent	I_{CC2}	V_I = V_{CC} or 0 V, All channels, no load,		8	13	mA
1 Mbps		EN_1 at 3 V, EN_2 at 3 V		8	13	
Electrical characteristics						
Sleep mode output current	I_{OFF}	EN at 0 V, Single channel		0		µA
High level output voltage	V_{OH}	I_{OH} = -4 mA, See FIGURE 6	V_{CC} – 0.4			V
		I_{OH} = -20 µA, See FIGURE 6	V_{CC} – 0.1			
Low level output voltage	V_{OL}	I_{OL} = 4 mA, See FIGURE 6			0.4	
		I_{OL} = 20 µA, See FIGURE 6			0.1	
Input voltage hysteresis	$V_{I(HYS)}$			150		mV
High level input current	I_{IH}	IN from 0 V to V_{CC}			10	µA
Low level input current	I_{IL}		-10			
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		2		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, See FIGURE 9	25	50		kV/µs
SWITCHING CHRACTERISTIC: V_{CC1} and V_{CC2} at 3.3-V OPERATION						
Propagation delay	t_{PLH}, t_{PHL}	See FIGURE 6	45		110	ns
Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ 4/	PWD				12	
Channel to channel output skew	$t_{sk(o)}$				3.5	
Output signal rise time	t_r	See FIGURE 6		2		
Output signal fall time	t_f			2		
Propagation delay, high level to high impedance output	t_{PHZ}	See FIGURE 7		15	20	
Propagation delay, high impedance to high level output	t_{PZH}			15	20	
Propagation delay, low level to high impedance output	t_{PLZ}			15	20	
Propagation delay, high impedance to low level output	t_{PZL}			15	20	
Fail safe output delay time from input power loss	t_{fs}	See FIGURE 8		18		µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

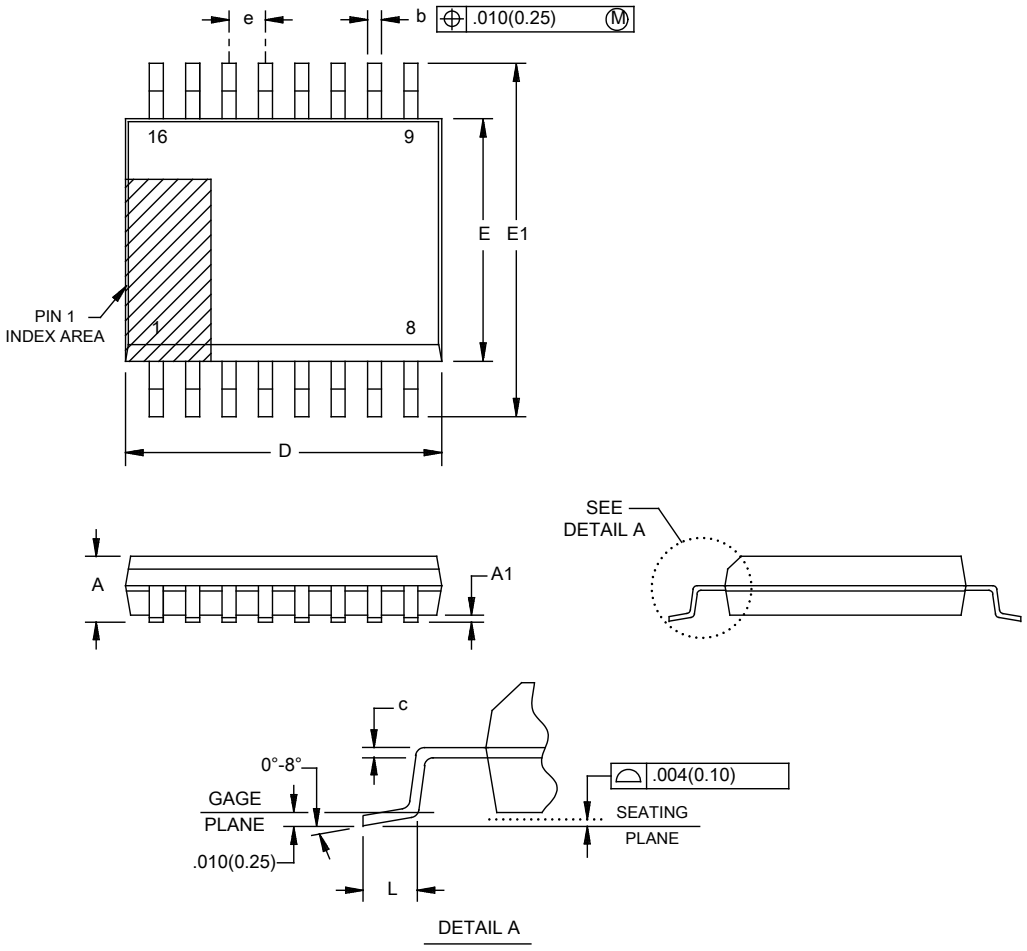
2/ Over recommended operating conditions (unless otherwise noted).

3/ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

4/ Also referred to as pulse skew.

5/ tsk(o) is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A		.104		2.65	E	.291	.299	7.40	7.60
A1	.004	.012	0.10	0.30	E1	.393	.419	9.97	10.63
b	.012	.020	0.31	0.51	e	.050	BSC	1.27	BSC
c	.008	.013	0.20	0.33	L	.016	.050	0.40	1.27
D	.398	.413	10.10	10.50					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed .006 (0.15)
4. Falls within JEDEC MO-13 variation AA.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VCC1	16	VCC2
2	GND1	15	GND2
3	IN_A	14	OUT_A
4	IN_B	13	OUT_B
5	IN_C	12	OUT_C
6	OUT_D	11	IN_D
7	EN_1	10	EN_2
8	GND1	9	GND2

FIGURE 2. Terminal connections.

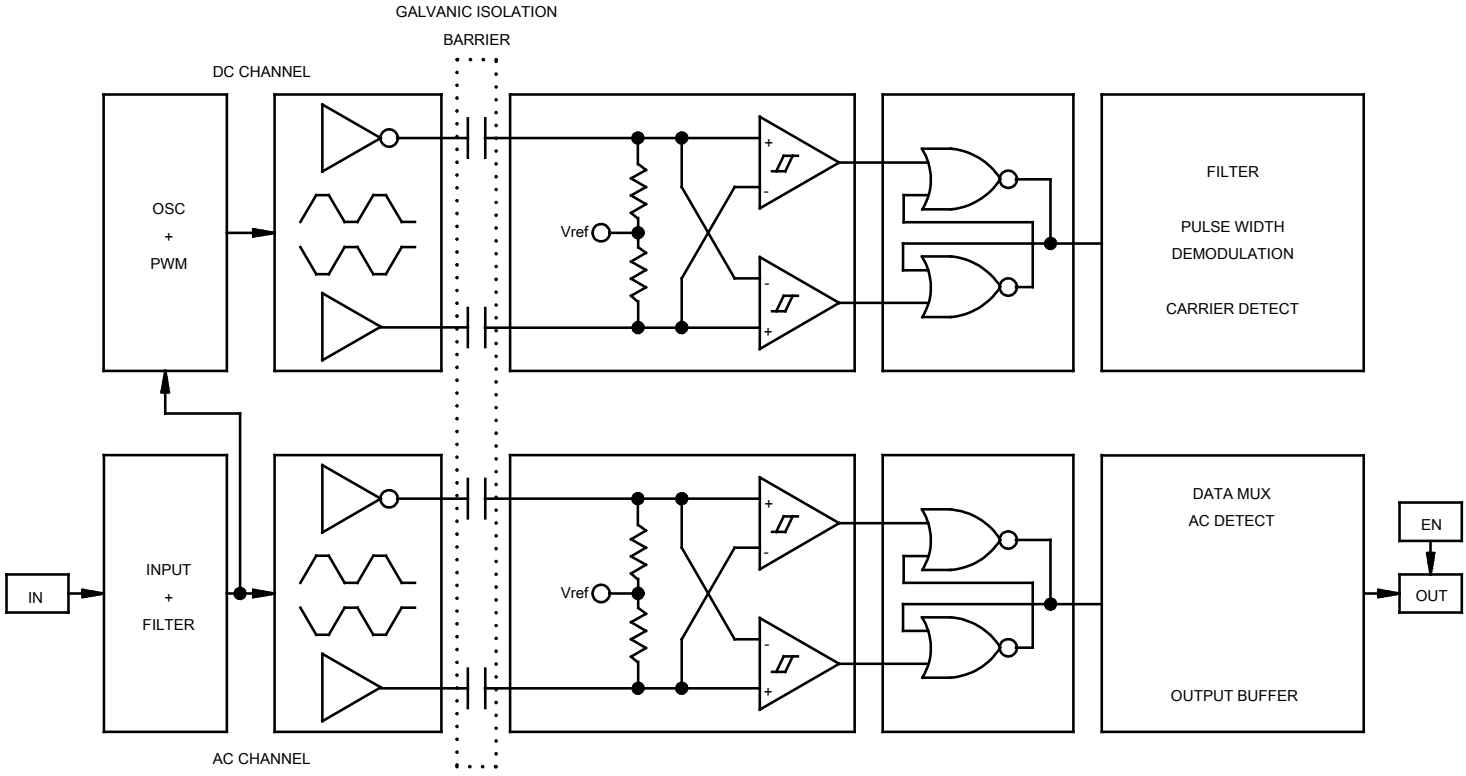


FIGURE 3. Function diagram.

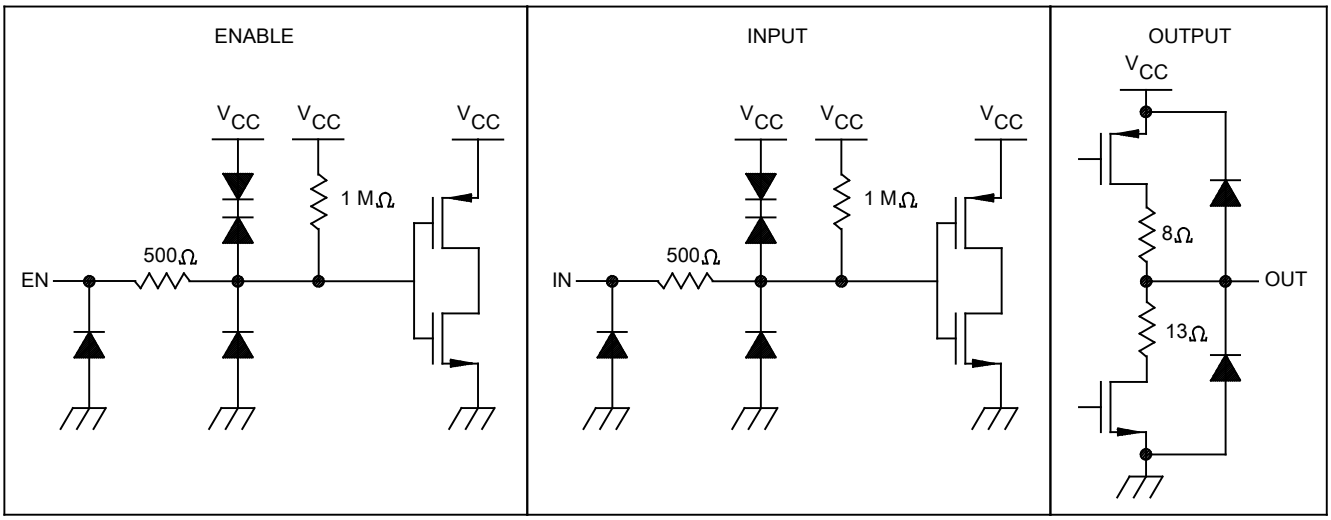


FIGURE 4. Device I/O schematics.

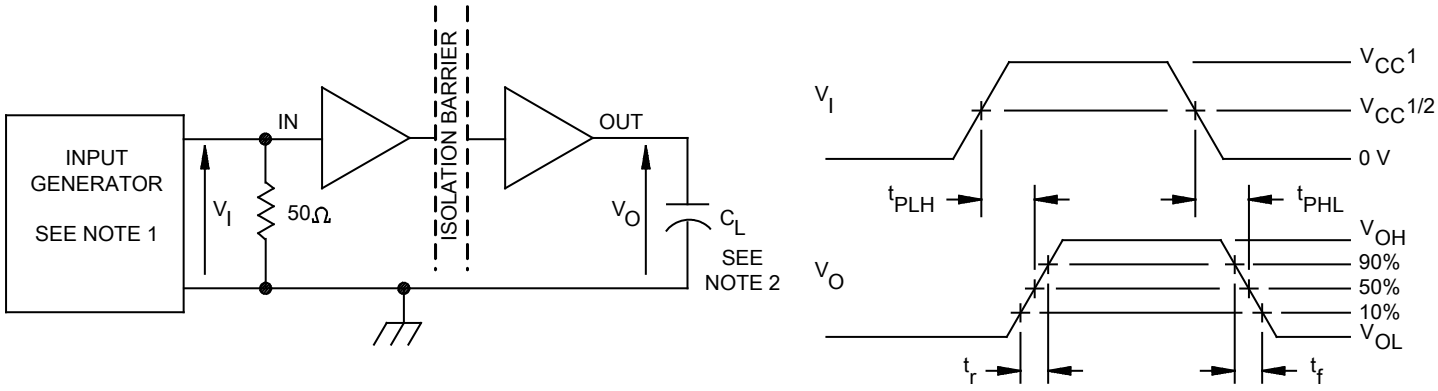
INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

PU = Powered Up PD = Powered Down

X = Irrelevant H = High level

L = Low level

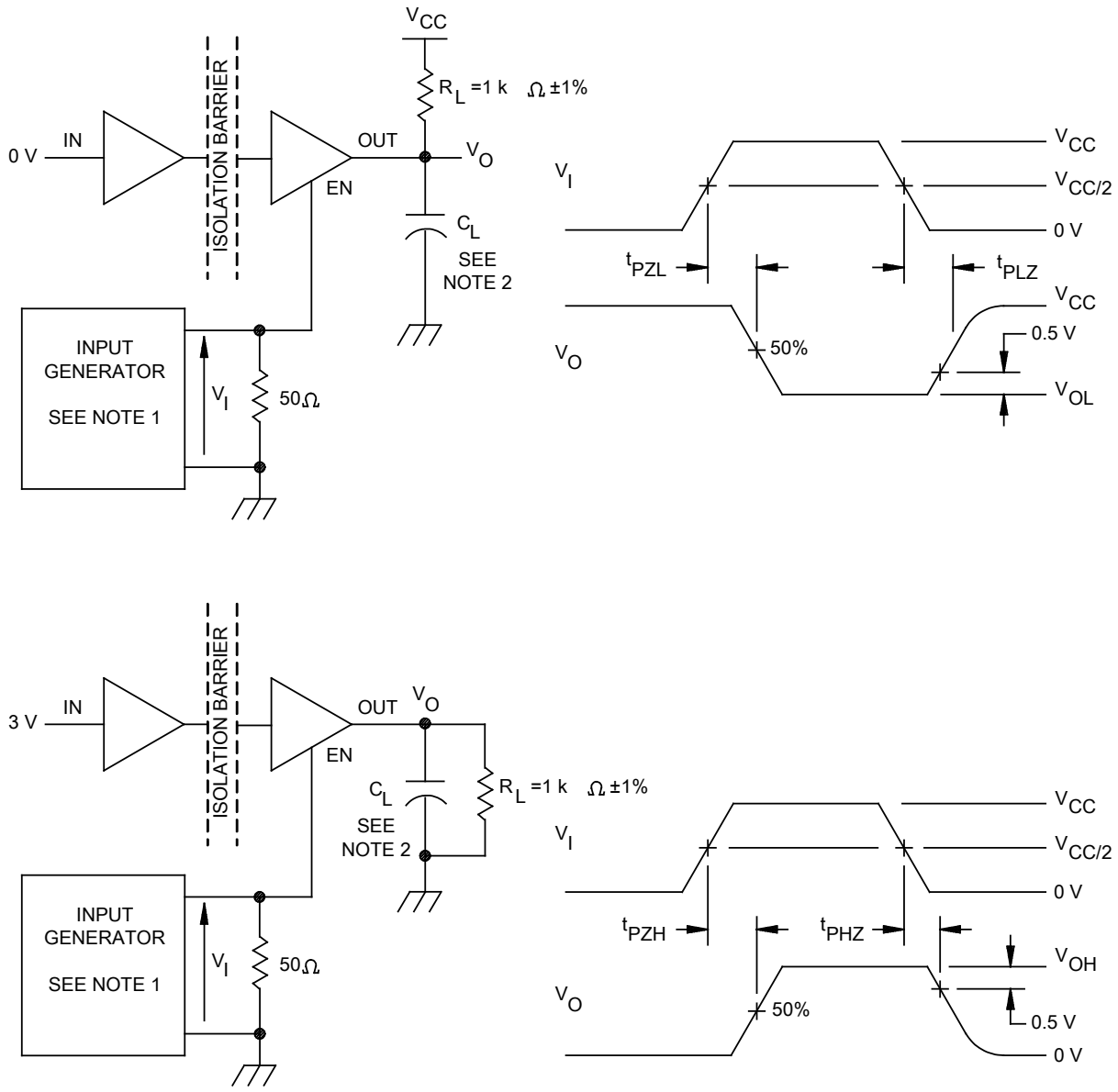
FIGURE 5. Device function table



NOTES:

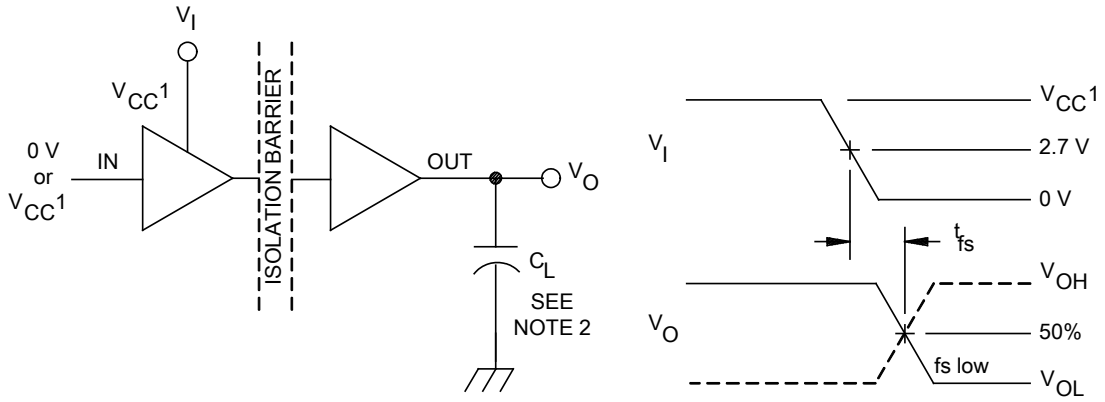
1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

FIGURE 6. Switching characteristic test circuit and voltage waveforms.



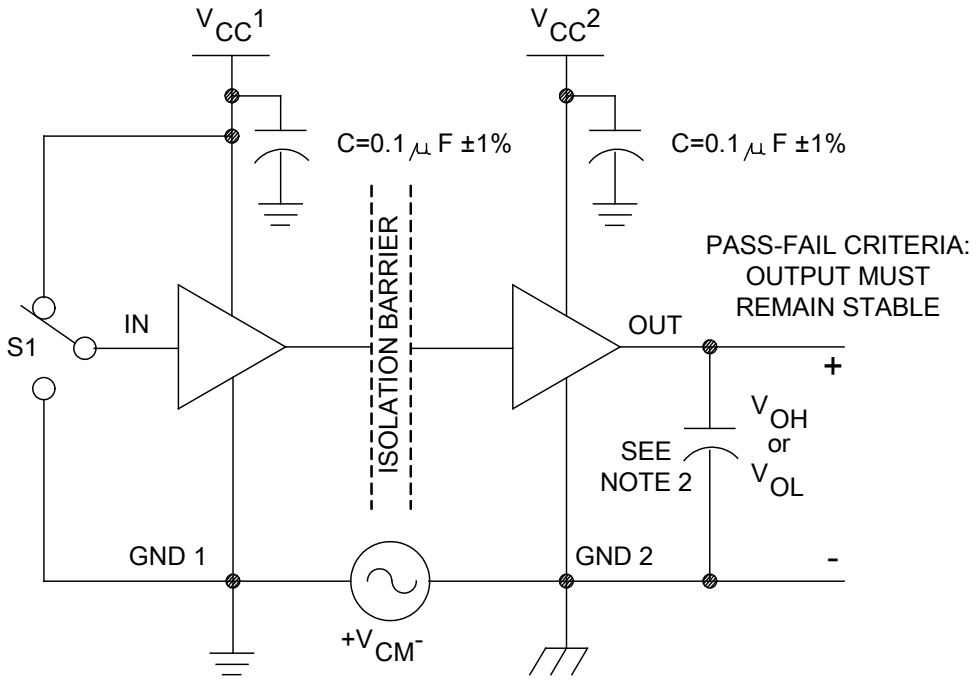
NOTES:
1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

FIGURE 7. Enable/Disenable propagation delay time test circuit and waveform.



NOTES:
1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
2. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

FIGURE 8. Failsafe delay time test circuit and voltage waveforms.



NOTES:
1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
2. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

FIGURE 9. Common mode transient immunity test circuit and voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/10606-01XE	01295	ISO7241AMDWREP	ISO7241AM

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243