REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add ESD information to paragraphs 1.3 and 2.0. Add paragraph 1.5. Make changes to Figure 1 terminal connections descriptions. Update document paragraphs to current requirements. - ro	16-04-04	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**	A	A	A	A	A	A	A	A	A	A	A	A						
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12						

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 10-08-11	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, LINEAR, PRECISION, LOW POWER INSTRUMENTATION AMPLIFIER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/10605**
	REV **A**	**PAGE** 1 **OF** 12

AMSC N/A

5962-V048-16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance precision, low power instrumentation amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/10605	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	INA129-EP	Precision, low power instrumentation amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S) ..... ±18 V
Analog input voltage range ..... ±40 V
Output short circuit (to ground) ..... Continuous
Power dissipation (P_D) ..... 166.6 mW
Junction temperature range (T_J) ..... 150°C
Storage temperature range (T_{STG}) ..... -55°C to +125°C
Lead temperature (soldering 10 seconds) ..... 300°C
Electrostatic discharge (ESD):
Human body model (HBM) ..... ±4000 V 2/
Charged device model (CDM) ..... ±200 V 3/

1.4 Recommended operating conditions. 4/

Supply voltage range (V_S) ..... ±15 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics. 5/

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	110	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	57	°C/W
Thermal resistance, junction-to-board	θ_{JB}	54	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	11	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	53	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

3/ JEDEC document JEP157 states that 250 V HBM allows safe manufacturing with a standard ESD control process.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ For more information about traditional and new thermal metrics, contact the manufacturer.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	-	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	-	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_S = ±15 V, R_L = 10 kΩ Unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input section							
Offset voltage, referred to input (RTI)							
Initial offset voltage			+25°C	01		±100 ±800/G	µV
			-55°C to +125°C			±150 ±2050/ G	
Offset voltage versus power supply		V_S = ±2.25 to ±18 V	+25°C	01		±1.6 ±175/G	µV/V
			-55°C to +125°C			±1.8 ±175/G	
Long term stability			+25°C	01	±1 ±3/G typical		µV/mo
Differential input 2/ impedance			+25°C	01	10^{10}||2 typical		Ω||pF
Common mode 2/ input impedance			+25°C	01	10^{11}||9 typical		Ω||pF
Common mode 3/ voltage range		V_O = 0 V	+25°C	01	(V+) - 2		V
					(V-) + 2		
Safe input voltage			+25°C	01		±40	V
Common mode rejection	CMR	G = 1, V_{CM} = ±13 V, ΔR_S = 1 kΩ	+25°C	01	75		dB
			-55°C to +125°C		67		
		G = 10, V_{CM} = ±13 V, ΔR_S = 1 kΩ	+25°C		93		
			-55°C to +125°C		84		
		G = 100, V_{CM} = ±13 V, ΔR_S = 1 kΩ	+25°C		113		
			-55°C to +125°C		98		
		G = 1000, V_{CM} = ±13 V, ΔR_S = 1 kΩ	+25°C		113		
			-55°C to +125°C		98		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = ±15 V, R_L = 10 kΩ Unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Current section							
Bias current	I_B		+25°C	01		±8	nA
			-55°C to +125°C			±16	
Offset current	I_{OS}		+25°C	01		±8	nA
			-55°C to +125°C			±16	
Noise section							
Noise voltage, referred to input (RTI)	V_N	f = 10 Hz, G = 1000, R_S = 0 Ω	+25°C	01	10 typical		nV / $\sqrt{Hz}$
		f = 100 Hz, G = 1000, R_S = 0 Ω			8 typical		
		f = 1 kHz, G = 1000, R_S = 0 Ω			8 typical		
		f_B = 0.1 Hz to 10 Hz, G = 1000, R_S = 0 Ω			0.2 typical		μVpp
Noise current		f = 10 Hz, G = 1000, R_S = 0 Ω	+25°C	01	0.9 typical		pA / $\sqrt{Hz}$
		f = 1 kHz, G = 1000, R_S = 0 Ω			0.3 typical		
		f_B = 0.1 Hz to 10 Hz, G = 1000, R_S = 0 Ω			30 typical		pApp
Gain section							
Gain equation			+25°C	01	1 + (49.4 kΩ/R_G) typical		V/V
Range gain			-55°C to +125°C	01	1	10000	V/V
Gain error		G = 1	+25°C	01		±0.1	%
			-55°C to +125°C			±0.15	
		G = 10	+25°C			±0.5	
			-55°C to +125°C			±0.65	
		G = 100	+25°C			±0.65	
			-55°C to +125°C			±1.1	
		G = 1000	+25°C			±2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = ±15 V, R_L = 10 kΩ Unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Gain section - continued.							
Gain versus temperature 4/		G = 1	+25°C	01		±10	ppm / °C
Gain 49.4 kΩ resistance 4/ 5/			+25°C	01		±100	ppm / °C
Nonlinearity		G = 1, V_O = ±13.6 V	+25°C	01		±0.0018	% of FSR
			-55°C to +125°C			±0.0035	
		G = 10	+25°C			±0.0035	
			-55°C to +125°C			±0.0055	
		G = 100	+25°C			±0.0035	
			-55°C to +125°C			±0.0055	
		G = 1000	+25°C			6/	
Output section							
Positive output voltage	$+V_{OUT}$	R_L = 10 kΩ	+25°C	01	(V+) - 1.4		V
Negative output voltage	$-V_{OUT}$	R_L = 10 kΩ	+25°C	01	(V-) + 1.4		V
Load capacitance stability	C_{LS}		+25°C	01	1000 typical		pF
Short circuit current	I_{SC}		+25°C	01	+6/-15 typical		mA
Frequency response section							
Bandwidth, -3 dB		G = 1	+25°C	01	1300 typical		kHz
		G = 10			700 typical		
		G = 100			200 typical		
		G = 1000			20 typical		
Slew rate	SR	V_O = ±10 V, G = 10	+25°C	01	4 typical		V/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_S = ±15 V, R_L = 10 kΩ Unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency response section - continued.							
Settling time, 0.01%	t_S	G = 1	+25°C	01	7 typical		µs
		G = 10			7 typical		
		G = 100			9 typical		
		G = 1000			80 typical		
Overload recovery		50% overdrive	+25°C	01	4 typical		µs
Power supply section							
Voltage range	V_R		+25°C	01	±2.25	±18	V
Current, total	I_T	V_{IN} = 0 V	+25°C	01		±750	µA
			-55°C to +125°C			±1200	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The || symbolizes that the input impedance is being represented as the resistance value is in parallel with the capacitance.

3/ Input common mode range varies with output voltage.

4/ Specified by wafer test.

5/ Temperature coefficient of the 49.9 kΩ term in the gain equation.

6/ Nonlinearity measurements in G = 1000 are dominated by noise. Typically nonlinearity is ±0.001%.

Case X

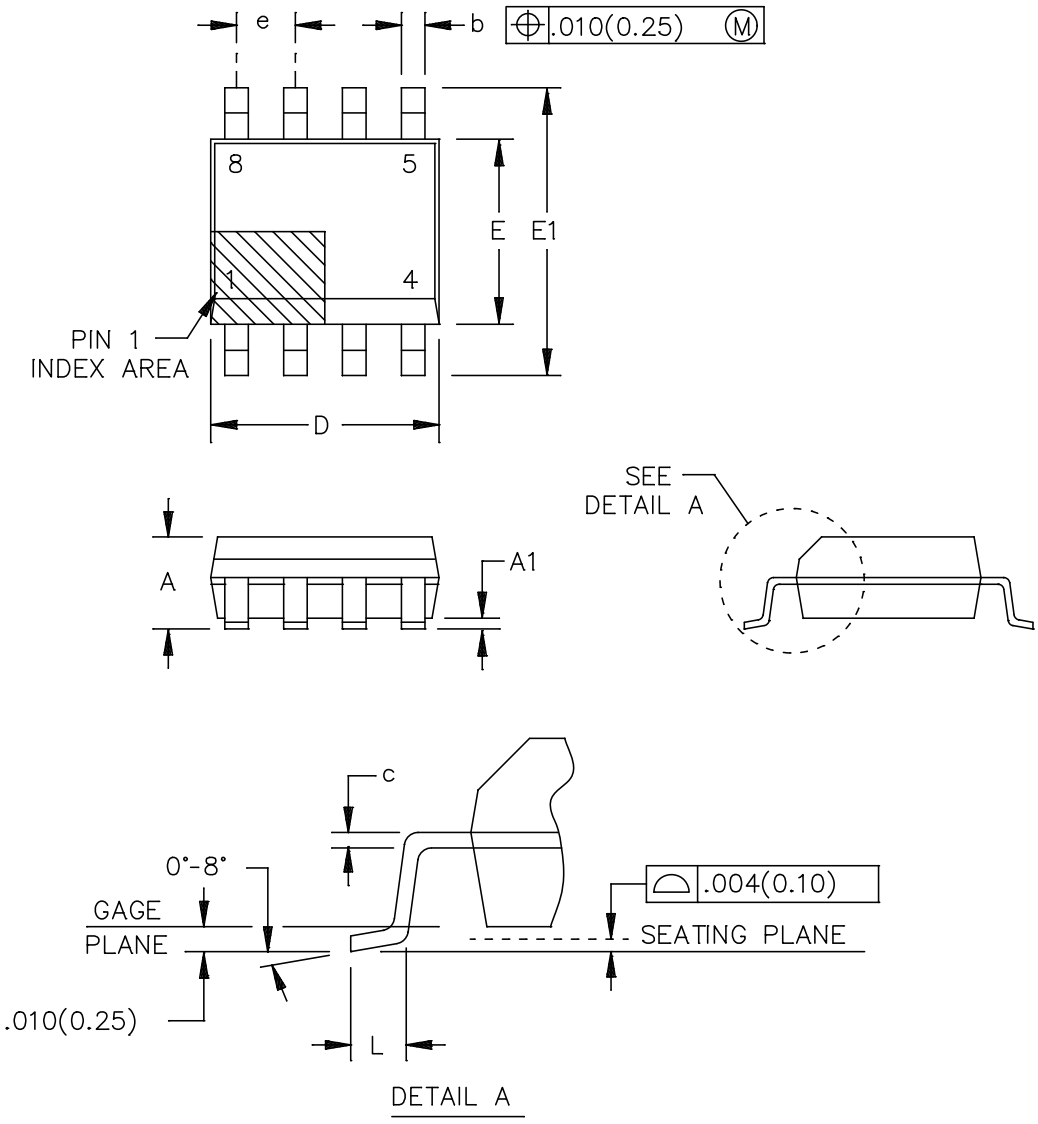

FIGURE 1. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.17	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within JEDEC MS-012-AA.

FIGURE 1. Case outline – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	R_G	O	Single external resistor used to set gain.
2	$-V_{IN}$	I	Negative input voltage.
3	$+V_{IN}$	I	Positive input voltage.
4	$-V_S$	Power	Negative power supply voltage from -2.25 to -18 V.
5	REF	I	Output voltage reference.
6	V_O	O	Output voltage.
7	$+V_S$	Power	Positive power supply voltage from 2.25 V to 18 V.
8	R_G	O	Single external resistor used to set gain.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking 2/ 3/	Vendor part number
V62/10605-01XE	01295	129EP	INA129MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet , or use website www.ti.com.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243