REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

PMIC N/A	PREPARED BY RAJESH PITHADIA		DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990
Original date of drawing YY-MM-DD 10-03-24	CHECKED BY RAJESH PITHADIA APPROVED BY CHARLES F. SAFFLE		TITLE MICROCIRCUIT, LINEAR, LOW POWER, RS-485/RS-422 TRANSMITTER, MONOLITHIC SILICON
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/10602
	REV		PAGE 1 OF 16

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance, low power, RS-485/RS-422 transmitter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/10602	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ISL3298E	Low power, RS-485/RS-422 transmitter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	See figure 1	Thin dual flat leadless plastic package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{CC} to GND	-0.3 V to 7 V
V_L to GND	-0.3 V to V_{CC} + 0.3 V
Input voltages:	
Pins DI, DE	-0.3 V to 7 V
Output voltages:	
Pins Y, Z ($V_{CC} \leq 3.6$ V)	-8 V to +13 V
Pins Y, Z ($V_{CC} > 3.6$ V)	-0.5 V to V_{CC} + 0.5 V
Short circuit duration:	
Pins Y, Z ($V_{CC} \leq 3.6$ V)	Continuous
Pins Y, Z ($V_{CC} > 3.6$ V) 2/	1 second at < 300 mA
ESD rating	See table I
Junction temperature range (TJ)	150°C
Storage temperature range (T_{STG})	-65°C to 150°C
Thermal resistance, junction to case (θ_{JC}): 3/ 4/	
X package	8°C/W
Thermal resistance, junction to ambient (θ_{JA}): 3/ 4/	
X package	65°C/W

1.4 Recommended operating conditions. 5/

Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Due to the high short circuit current at V_{CC} >3.6 V, the outputs must not be shorted outside the range of GND to V_{CC} or damage may occur. To prevent excessive power dissipation that may damage the output, the short circuit current should be limited to ≤ 300 mA during testing. It is best to use an external resistor for this purpose, since the current limiting on the V_O supply may respond too slowly to protect the output.

3/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See manufacturer's technical brief TB379.

4/ For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

IEC 61000-4-2 – Electromagnetic Compatibility (EMC) – Part 4-2
Testing and Measurement Techniques – Electrostatic Discharge Immunity Test

(Applications for copies should be addressed to the International Electrotechnical Commission Regional Centre for North America 446 Main Street, 16th Floor, Worcester, MA 01608 or online at http://www.iec.ch)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4, 5, 6, and 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/ 4/		Unit
					Min	Max	
DC characteristics							
Driver differential V_{OUT}	V_{OD}	R_L = 100 Ω (RS-422), V_{CC} ≥ 3.15 V, See figure 4 circuit A	-55°C to +125°C	01	2		V
		R_L = 100 Ω (RS-422), V_{CC} ≥ 4.5 V, See figure 4 circuit A			3		V
		R_L = 54 Ω (RS-485), V_{CC} ≥ 3.0 V, See figure 4 circuit A			1.5	V_{CC}	V
		R_L = 54 Ω (RS-485), V_{CC} ≥ 4.5 V, See figure 4 circuit A			2.5	V_{CC}	V
		No load				V_{CC}	V
		R_L = 60 Ω, -7 V ≤ V_{CM} ≤ 12 V, See figure 4 circuit B			1.5		V
Change in magnitude of driver differential V_{OUT} for complementary output states	ΔV_{OD}	R_L = 54 Ω or 100 Ω, See figure 4 circuit A	-55°C to +125°C	01		0.2	V
Driver common-mode V_{OUT}	V_{OC}	R_L = 54 Ω or 100 Ω, V_{CC} ≤ 3.6 V See figure 4 circuit A	-55°C to +125°C	01		3	V
		R_L = 54 Ω or 100 Ω, V_{CC} ≤ 5.5 V See figure 4 circuit A				3.2	
Change in magnitude of driver common-mode V_{OUT} for complementary output states	ΔV_{OC}	R_L = 54 Ω or 100 Ω, See figure 4 circuit A	-55°C to +125°C	01		0.2	V
Input high voltage (DI, DE)	V_{IH1}	V_L = V_{CC}, V_{CC} ≤ 3.6 V	-55°C to +125°C	01	2.2		V
	V_{IH2}	V_L = V_{CC}, V_{CC} ≤ 5.5 V			3		
	V_{IH3}	2.7 V ≤ V_L < 3.0 V			2		
	V_{IH4}	2.3 V ≤ V_L < 2.7 V			1.65		
	V_{IH5}	1.6 V ≤ V_L < 2.3 V			0.7*V_L		
	V_{IH6}	1.35 V ≤ V_L < 1.6 V	+25°C		0.5*V_L typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/ 4/ Min	Max	Unit
DC characteristics – continued.							
Input low voltage (DI, DE)	V_{IL1}	$V_L = V_{CC}$	-55°C to +125°C	01		0.8	V
	V_{IL2}	$V_L \geq 2.7$ V				0.8	
	V_{IL3}	2.3 V ≤ V_L < 2.7 V				0.65	
	V_{IL4}	1.6 V ≤ V_L < 2.3 V				0.22*V_L	
	V_{IL5}	1.35 V ≤ V_L < 1.6 V	+25°C		0.3*V_L typical		
Logic input current	I_{IN}	DI = DE = 0 V or V_{CC} 5/	-55°C to +125°C	01	-2	2	µA
Output leakage current (Y, Z) 5/	I_{OZ}	DE = 0 V, V_{CC} = 0 V, 3.6 V, or 5.5 V, V_{IN} = 12 V	-55°C to +125°C	01		40	µA
		DE = 0 V, V_{CC} = 0 V, 3.6 V, or 5.5 V, V_{IN} = -7 V			-40		
Driver short circuit current, V_O = High or Low 6/	I_{OSD1}	DE = V_{CC}, -7 V ≤ V_O ≤ 12 V, V_{CC} ≤ 3.6 V	-55°C to +125°C	01		±250	mA
		DE = V_{CC}, 0 V ≤ V_O ≤ V_{CC}, V_{CC} > 3.6 V 7/				±450	
Thermal shutdown threshold	T_{SD}		-55°C to +125°C	01	160 typical		°C
Supply current							
No load supply current	I_{CC}	DI = 0 V or V_{CC}, DE = V_{CC}	-55°C to +125°C	01		150	µA
Shutdown supply current	I_{SHDN}	DE = O V, DI = 0 V or V_{CC}	-55°C to +125°C			1	µA
ESD performance							
RS-485 pins (Y, Z)		Human body model, from bus pins to GND	+25°C	01	±16.5 typical		kV
		IEC61000 contact, from bus pins to GND			±7 typical		
All pins		Human body model, per MIL-STD-883 method 3015			±8 typical		
		Machine model			±400 typical		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/ 4/ Min	Limits 3/ 4/ Max	Unit
Driver switching characteristics							
Maximum data rate	f_{MAX}	V_{OD} = ±1.5 V, C_D = 360 pF, See figure 5	-55°C to +125°C	01	16		Mbps
Driver single ended output delay	t_{SD}	R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = V_{CC}, see figure 6	-55°C to +125°C	01	15	42	ns
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L ≥ 1.8 V, see figure 6	+25°C		32 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.5 V, see figure 6			36 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.35 V, see figure 6			40 typical		
Part-to-part output delay skew	t_{SKPP}	R_{DIFF} = 54 Ω, C_D = 50 pF, see figure 6 8/	-55°C to +125°C	01		25	ns
Driver single ended output skew	t_{SSK}	R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = V_{CC}, see figure 6	-55°C to +125°C	01		7	ns
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L ≥ 1.8 V, see figure 6	+25°C		3 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.5 V, see figure 6			4 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.35 V, see figure 6			5 typical		
Driver differential output delay	t_{DD}	R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = V_{CC}, see figure 6	-55°C to +125°C	01		42	ns
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L ≥ 1.8 V, see figure 6	+25°C		32 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.5 V, see figure 6			36 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.35 V, see figure 6			42 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits 3/ 4/ Min	Limits 3/ 4/ Max	Unit
Driver switching characteristics – continued.							
Driver differential output skew	t_{DSK}	R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L = V_{CC} \le 3.6$ V, see figure 6	-55°C to +125°C	01		3	ns
		R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L = V_{CC}$ = 5 V, see figure 6	+25°C		2 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L \ge 1.8$ V, V_{CC} = 3.3 V, see figure 6			0.5 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L \ge 1.8$ V, V_{CC} = 5 V, see figure 6			1 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L \ge 1.5$ V, V_{CC} = 3.3 V, see figure 6			1 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L \ge 1.5$ V, V_{CC} = 5 V, see figure 6			2 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.35 V, V_{CC} = 3.3 V, see figure 6			2 typical		
		R_{DIFF} = 54 Ω, C_D = 50 pF, V_L = 1.35 V, V_{CC} = 5 V, see figure 6			4 typical		
Driver differential rise or fall time	t_R, t_F	R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L = V_{CC}$, see figure 6	-55°C to +125°C	01		15	ns
		R_{DIFF} = 54 Ω, C_D = 50 pF, $V_L \ge 1.35$ V, see figure 6	+25°C		9 typical		
Driver enable to output high	t_{ZH}	R_L = 500 Ω, C_L = 50 pF, SW = GND, see figure 7	-55°C to +125°C	01		250	ns
Driver enable to output low	t_{ZL}	R_L = 500 Ω, C_L = 50 pF, SW = V_{CC}, see figure 7	-55°C to +125°C	01		250	ns
Driver disable from output high	t_{HZ}	R_L = 500 Ω, C_L = 50 pF, SW = GND, see figure 7	-55°C to +125°C	01		60	ns
Driver disable from output low	t_{LZ}	R_L = 500 Ω, C_L = 50 pF, SW = V_{CC}, see figure 7	-55°C to +125°C	01		60	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{CC} = 3.0 V to 5.5 V, $V_L = V_{CC}$. Typical values are at T_A = +25°C. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground.

3/ Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

4/ Typicals are measured at V_{CC} = 3.3 V for parameters specified with 3 V ≤ V_{CC} ≤ 3.6 V, and are measured at V_{CC} = 5 V for parameters specified with 4.5 V ≤ V_{CC} ≤ 5.5 V. If V_{CC} isn't specified, then a single "typical" entry applies to both V_{CC} = 3.3 V and 5 V.

5/ If the driver enable function isn't needed, connect DE to V_{CC} (or V_L) through a 1 kΩ to 3 kΩ resistor.

6/ Applies to peak current.

7/ Due to the high short circuit current at V_{CC} >3.6 V, the outputs must not be shorted outside the range of GND to V_{CC} or damage may occur. To prevent excessive power dissipation that may damage the output, the short circuit current should be limited to ≤ 300 mA during testing. It is best to use an external resistor for this purpose, since the current limiting on the V_O supply may respond too slowly to protect the output.

8/ t_{SKPP} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (V_{CC}, temperature, etc.).

Case X

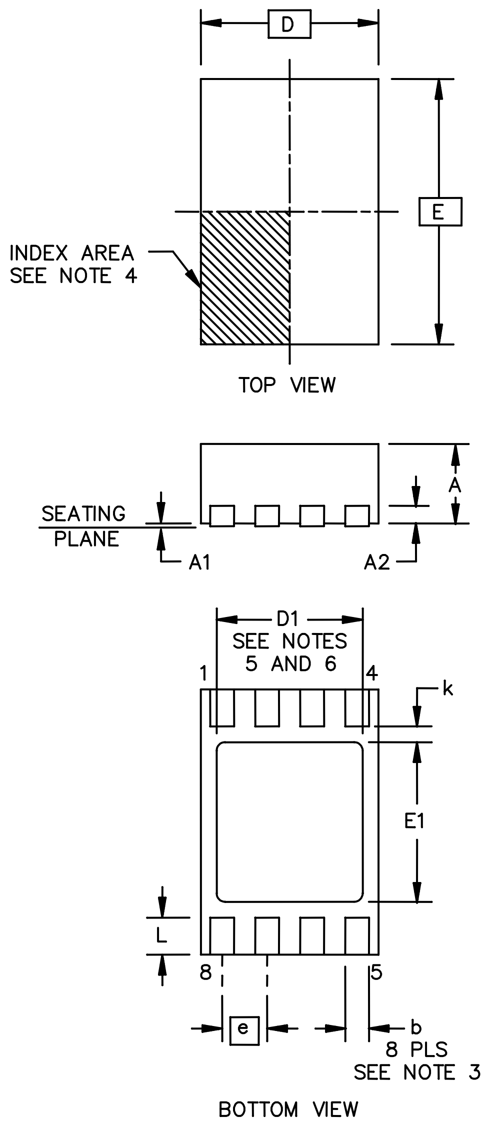


FIGURE 1. Case outlines.

Case X

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.027	.031	0.70	0.80	----
A1	----	.001	----	0.05	----
A2	.007 REF		0.20 REF		----
b	.007	.012	0.20	0.32	3, 6
D	.078 BSC		2.00 BSC		----
D1	.059	.068	1.50	1.75	5, 6
E	.118 BSC		3.00 BSC		----
E1	.064	.074	1.65	1.90	5, 6
e	.019 BSC		0.50 BSC		----
k	.007	----	0.20	----	----
L	.011	.019	0.30	0.50	6
N	8		8		7

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5-1994.
3. Dimension b applies to the metalized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
4. The configuration of the pin number 1 identifier is optional, but must be located within the zone indicated.
   the pin number 1 identifier may be either a mold or mark feature.
5. Dimesions D1 and E1 are for the exposed pads which provide improved electrical and thermal performance.
6. Nominal dimensions are provided to assist with printed circuit board land pattern design efforts, see manufacturer's technical brief TB389.
7. N is the number of terminals.

FIGURE 1. Case outlines – Continued.

Device type	01
Case outlines	X
Terminal number	Terminal symbol
1	V_L
2	DE
3	DI
4	GND
5	GND
6	Y
7	Z
8	V_{CC}

Terminal symbol	Description
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the driver enable function isn't needed, connect DE to V_{CC} (or V_L) through a 1 kΩ to 3 kΩ resistor.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection. This is also the potential of the thin dual flat leadless package thermal pad.
Y	±15 kV human body model, ±7 kV IEC61000 (contact method) ESD Protected RS-485/422 level, noninverting transmitter output.
Z	±15 kV human body model, ±7 kV IEC61000 (contact method) ESD Protected RS-485/422 level, inverting transmitter output.
V_{CC}	System power supply input (3.0 V to 5.5 V). On devices with a V_L pin, power-up V_{CC} first.
V_L	Logic-level supply which sets the V_{IL}/V_{IH} levels for the DI and DE pins. Power-up this supply after V_{CC}, and keep $V_L \leq V_{CC}$.

FIGURE 2. Terminal connections.

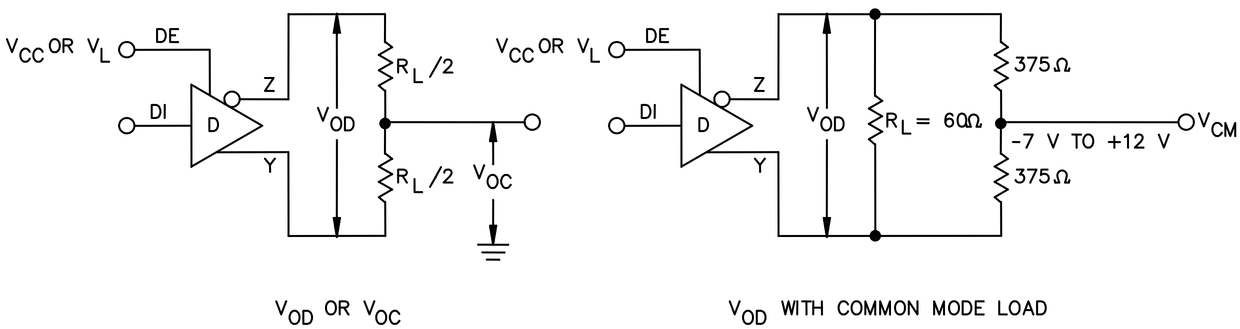
Inputs		Output	
DE (see note 1)	DI	Z	Y
1	1	0	1
1	0	1	0
0	X	High-Z (see note 2)	High-Z (see note 2)

X = Don't care

NOTES:

1. If the driver enable function isn't needed, connect DE to V_{CC} (or V_L) through a 1 kΩ to 3 kΩ resistor.
2. Shutdown mode.

FIGURE 3. Truth table.



Circuit A

Circuit B

FIGURE 4. DC driver test circuits.

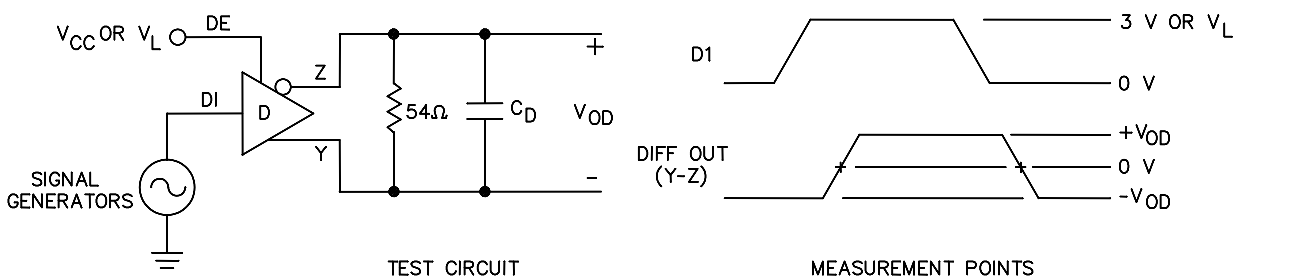


FIGURE 5. Driver data rate.

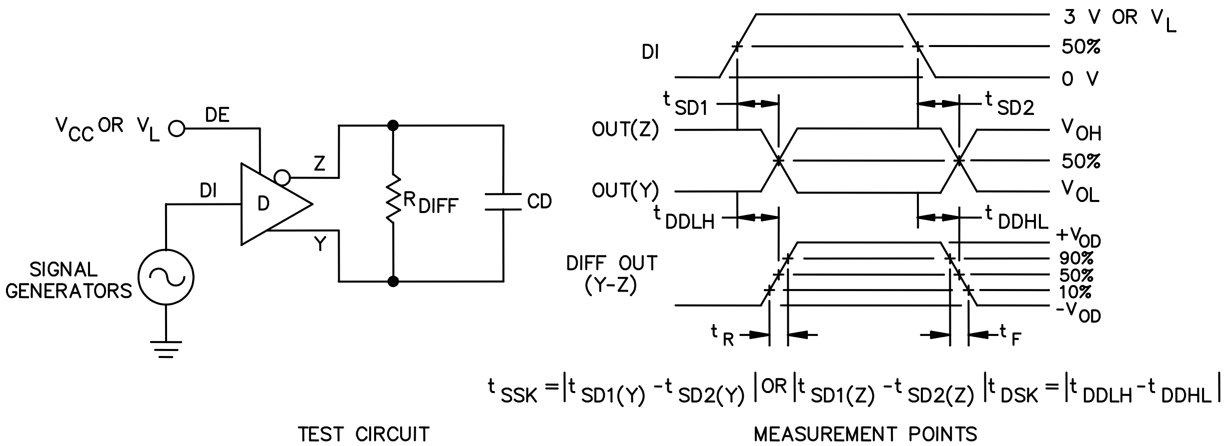
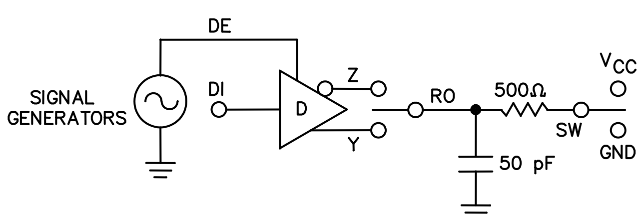
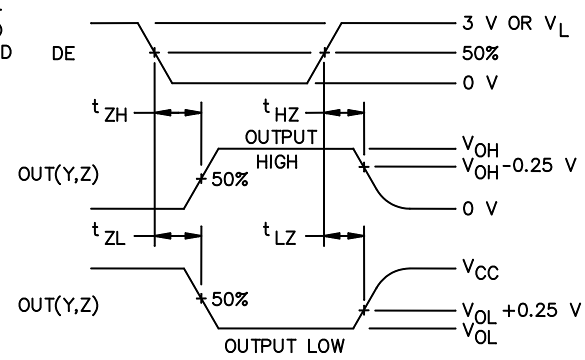


FIGURE 6. Driver propagation delay and differential transition times.



PARAMETER	OUTPUT	DI	SW
t_{HZ}	Y/Z	1/0	GND
t_{LZ}	Y/Z	0/1	V_{CC}
t_{ZH}	Y/Z	1/0	GND
t_{ZL}	Y/Z	0/1	V_{CC}

TEST CIRCUIT



MEASUREMENT POINTS

FIGURE 7. Driver enable and disable times.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number 2/
V62/10602-01XB	34371	298	ISL3298EMRTEP-T/-TK

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Add suffix –T for 6 thousand pieces per reel. Add suffix –TK for 1 thousand pieces per reel.

CAGE code	Source of supply
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035-6803 Point of contact: 1650 Robert J. Conlan Blvd. Palm Bay, FL 32905